RK3358J
Hardware Design Guide

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Author：	
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Preface

Overview

This document mainly introduces the key points of hardware design for RK3358J, aiming at helping customers to shorten product design period, improve stability and reduce bugs. Please follow this guide strictly for the hardware design, and use the relative core board released by RK. If need to change in special cases, please get confirmation from RK engineer first.

Chipset model

The chipset model described in this document is RK3358J

Relevant product versions are shown as below:

Product Name	Product Version
RK3358J MINI EVB	

Applicable object

- This document is mainly suitable for the following engineers:
- 1. Hardware development & PCB layout engineers
- 2. Field application engineers
- 3. Test engineers

Revision history

This revision history recorded description of each version, and any updates of previous versions are included in the latest one.

Revision Date	Version No.	Author	Revision Description
2019-05	V1.0	Hardware Group	Initial Release

Acronym

Acronyms used in the document are as below:

DDR	Double Data Rate	双倍速率同步动态随机存储器
eMMC	Embedded Multi Media Card	内嵌式多媒体存储卡
HDMI	High Definition Multimedia Interface	高清晰度多媒体接口
I²C	Inter-Integrated Circuit	内部整合电路(两线式串行通讯总线)
JTAG	Joint Test Action Group	联合测试行为组织定义的一种国际标准测试协议（IEEE 1149.1兼容）
LDO	Low Drop Out Linear Regulator	低压差线性稳压器
LVDS	Low-Voltage Differential Signaling	低电压差分信号
MAC	Media Access Control	以太网媒体接入控制器
MIPI	Mobile Industry Processor Interface	移动产业处理器接口
PMIC	Power Management IC	电源管理芯片
PMU	Power Management Unit	电源管理单元
RK	Rockchip Electronics Co.,Ltd.	瑞芯微电子股份有限公司
SD Card	Secure Digital Memory Card	安全数码卡
SDIO	Secure Digital Input and Output Card	安全数字输入输出卡
SDMMC	Secure Digital Multi Media Card	安全数字多媒体存储卡
SPI	Serial Peripheral Interface	串行外设接口
TF Card	Micro SD Card(Trans-flash Card)	外置记忆卡
USB	Universal Serial Bus	通用串行总线

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Chapter 1 Brief Introduction

1.1 Overview

RK3358J is a high-performance Quad-core application processor designed for personal mobile internet device and other digital multimedia applications, such as tablet, smart audio display products.

RK3358J embeds many powerful hardware engines, provides excellent performance for high-end application, supports almost full-format H.264 decoder by 1080p@60fps, H.265 decoder by 1080p@60fps, H.264 encoder by 1080p@30fps, and high-quality JPEG encoder/decoder.

Embedded 3D GPU makes RK3358J completely compatible with OpenGL ES 1.1/2.0/3.2, DirectX11.1, OpenCL 2.0 and Vulkan 1.0. Special MMU 2D hardware decoder will maximize display performance and provide smooth operation experience.

RK3358J supports various types of DDR memory interfaces such as DDR3/DDR3L/DDR4/LPDDR2/LPDDR3.

1.2 Block Diagram

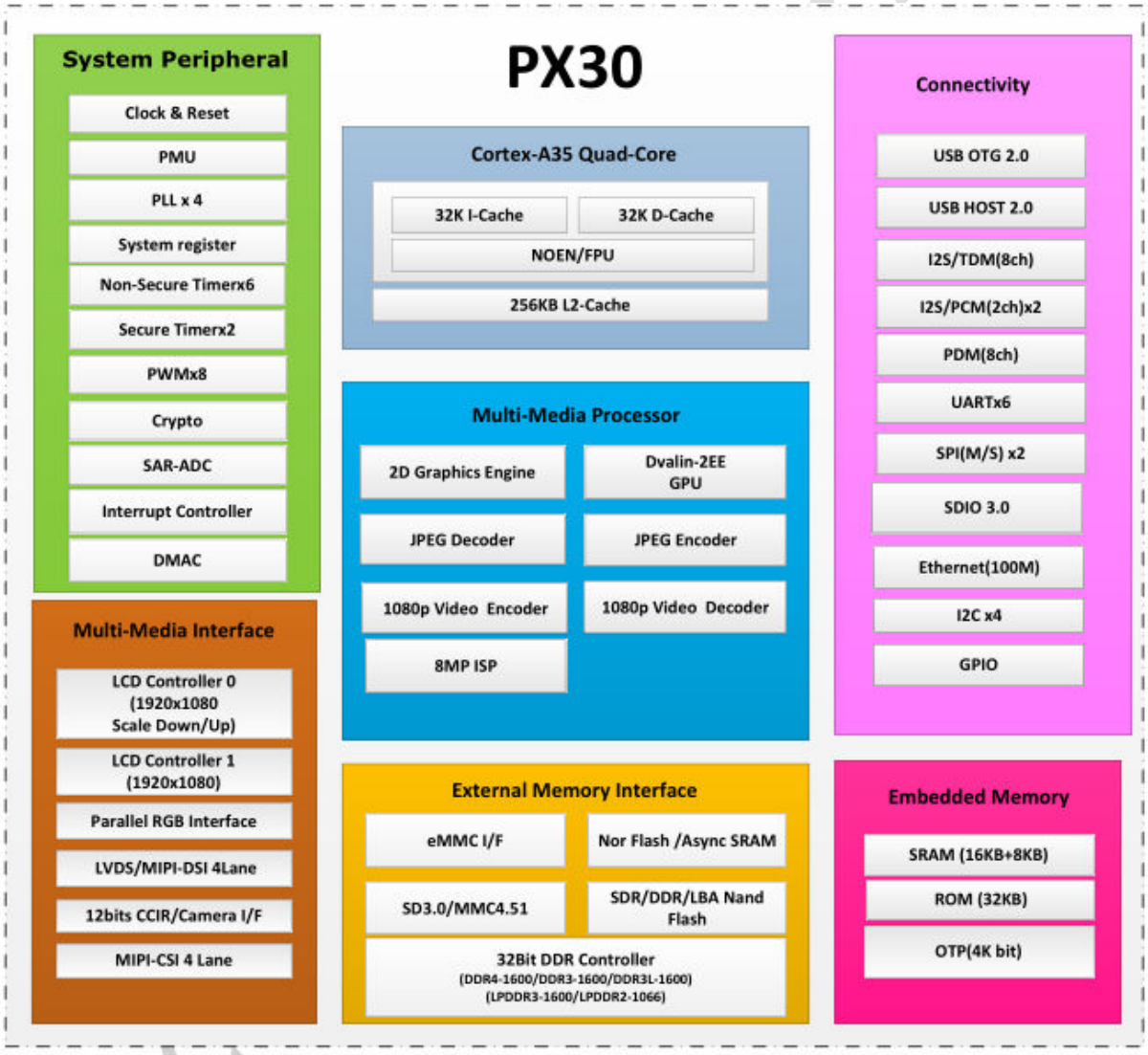


Figure 1-1 RK3358J block diagram

1.3 Application block diagram

1.3.1 Demo application block diagram

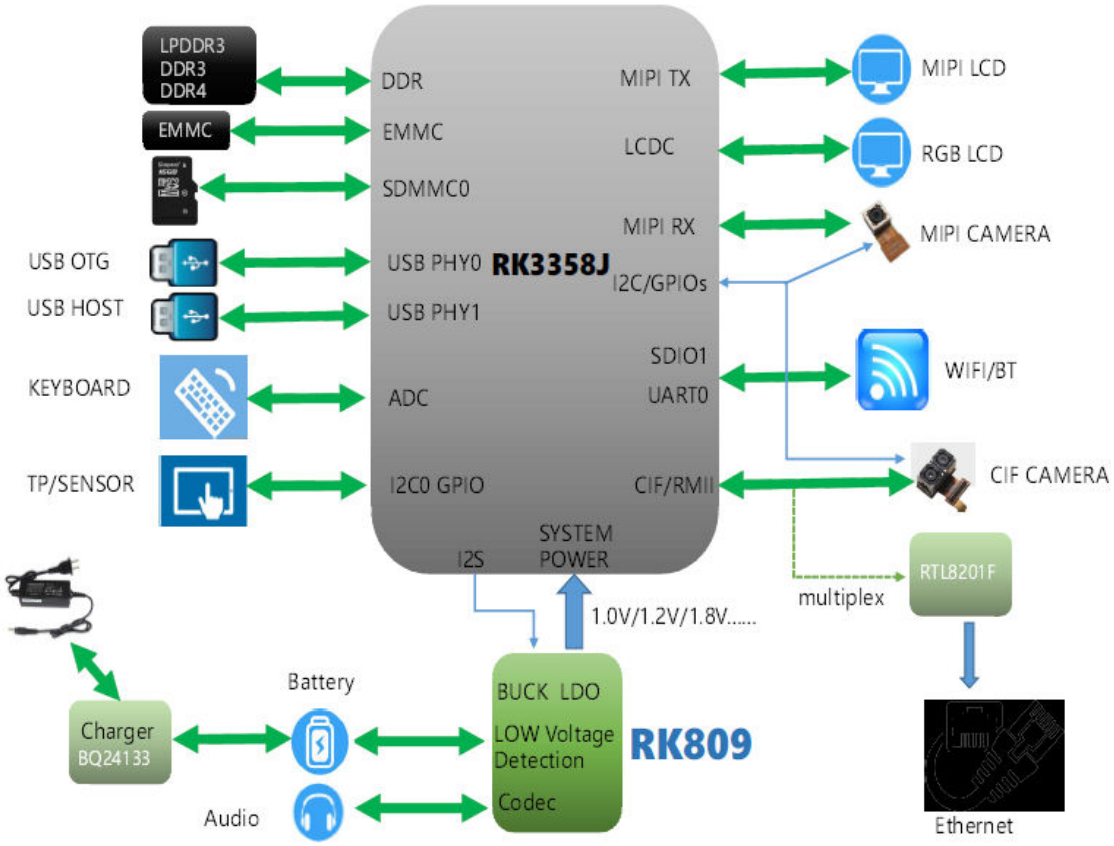


Figure 1-2 RK3358J Demo application block diagram

The above is the application block diagram of RK3358J. For more details, please refer to the reference design schematic released by RK.

2 Package and Pin

2.1 Package

2.1.1 Information

RK3358J encapsulation information is shown in table 2-1.

Table 2-1
RK3358J Package information

Orderable Device	RoHS Status	Package	Package Qty	Device special feature
RK3358J	RoHS	Bga418	1190	Quad-core ARM Cortex A35 CPU

2.1.2 Mark definition

RK3358J surface printing logo is shown as Picture 2-1：

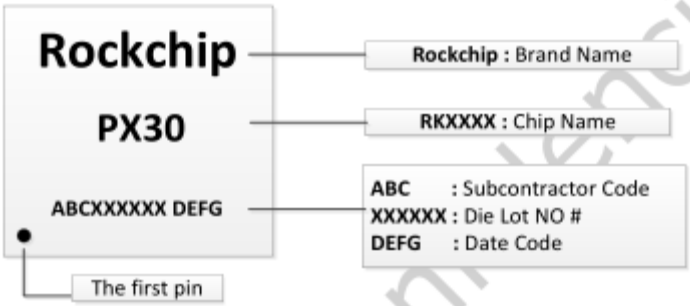


Figure 2-1 RK3358J Mark definition

2.1.3 Package Dimension

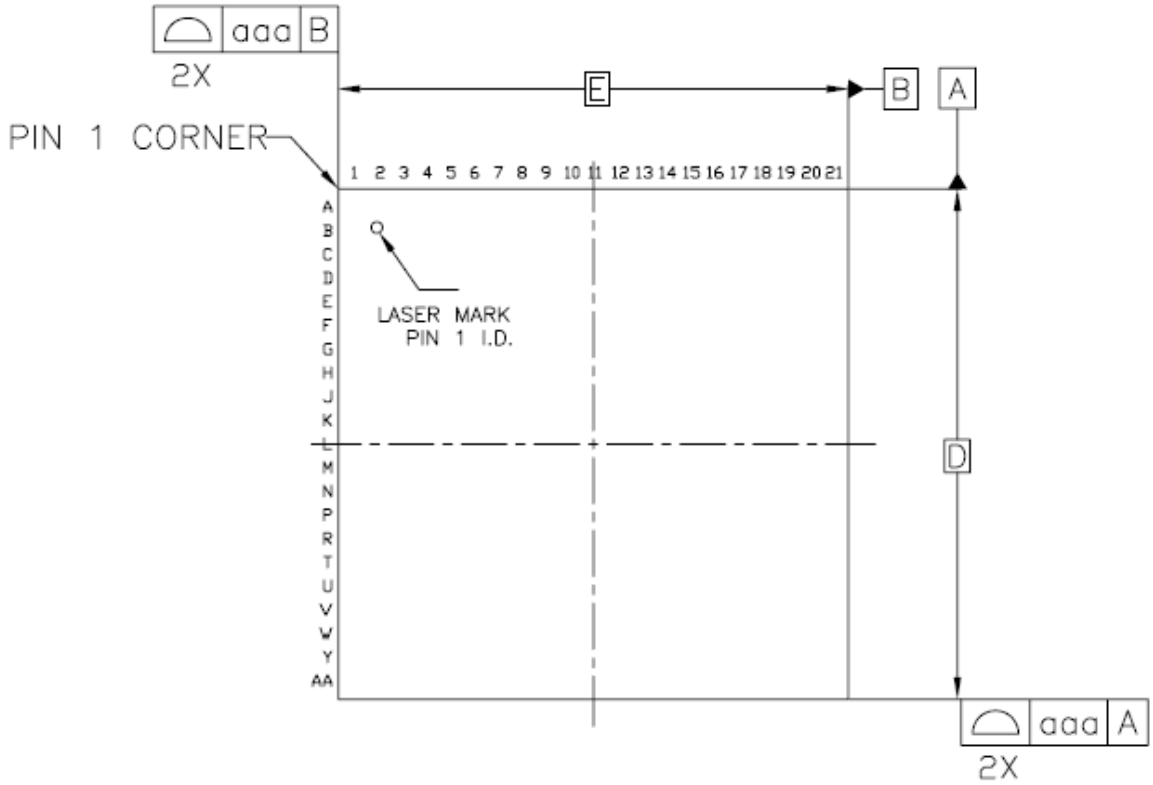


Figure 2-2 RK3358J Package dimension 1

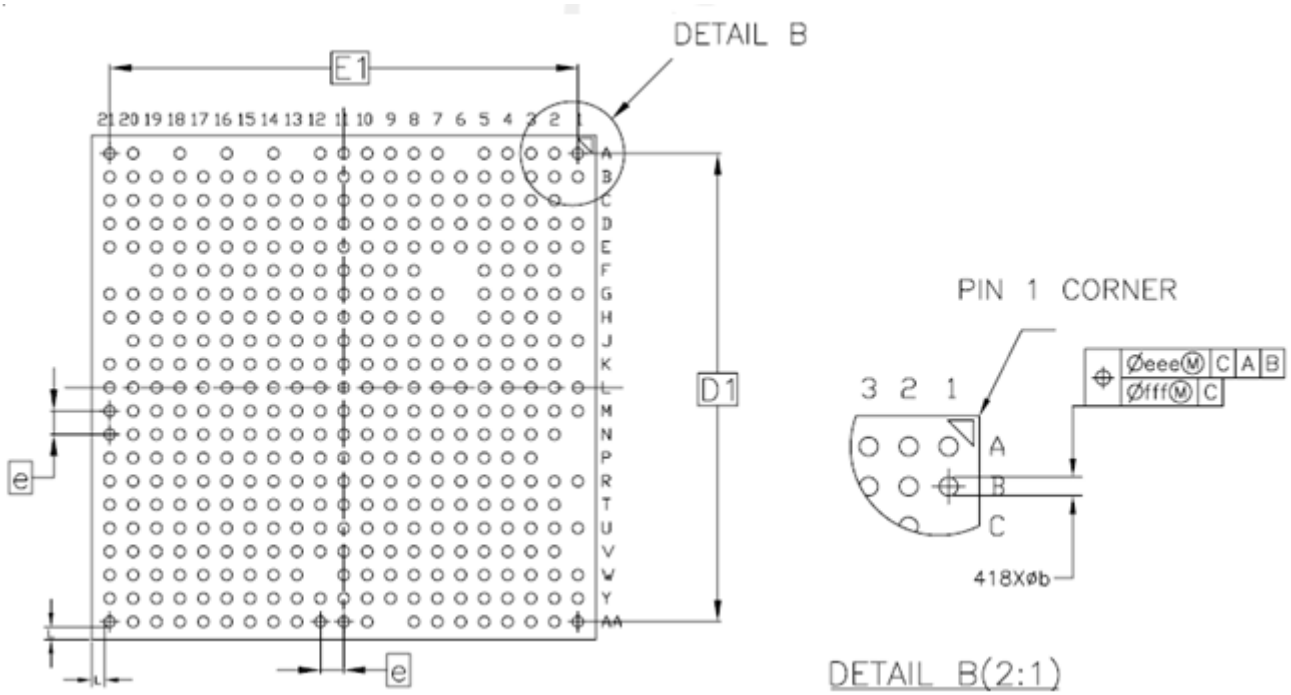


Figure 2-3 RK3358J package dimension 2

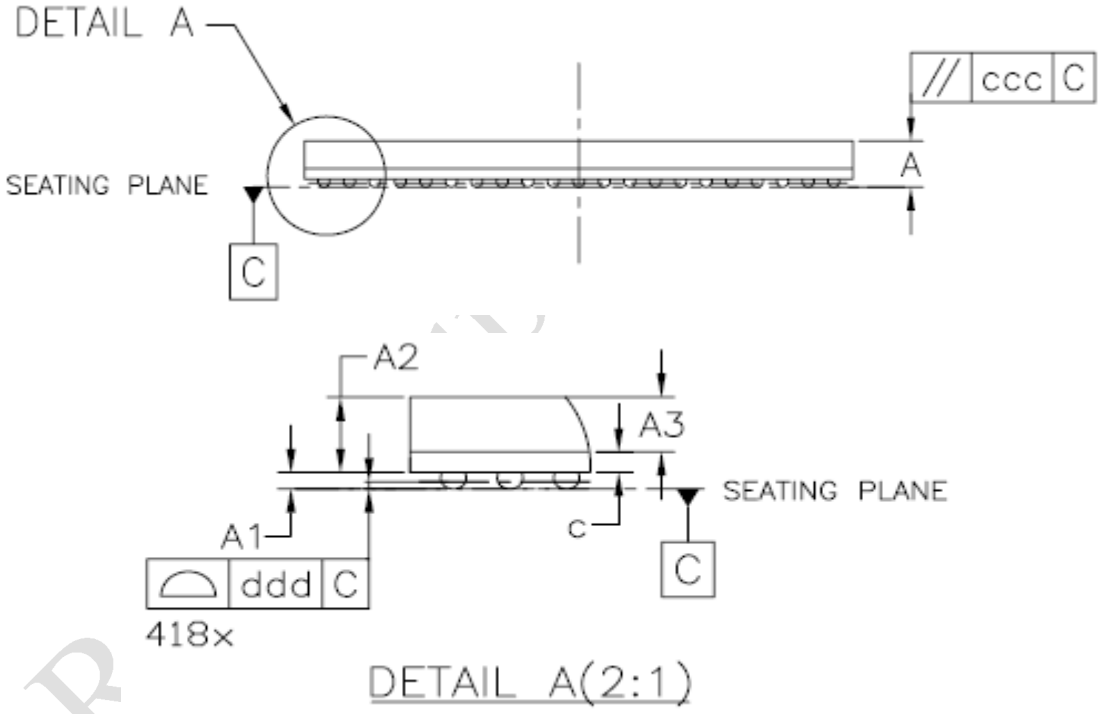


Figure 2-4 RK3358J package dimension 3

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	1.17	1.25
A1	0.16	0.21	0.26
A2	0.91	0.96	1.01
A3	0.70 BASIC		
c	0.22	0.26	0.30
D	13.90	14.00	14.10
D1	13.00 BASIC		
E	13.90	14.00	14.10
E1	13.00 BASIC		
e	0.65 BASIC		
b	0.25	0.30	0.35
L	0.35 REF		
aaa	0.15		
ccc	0.15		
ddd	0.10		
eee	0.15		
fff	0.08		

Figure 2-5 RK3358J package dimension 4

Note

Baseline C is defined by the spherical coronal of the solder ball.
Size b is measured according to the maximum diameter of the solder ball, parallel to baseline C.

2.2 GPIO type introduction

2.2.1 GPIO type

For RK3358J, GPIO type is 1.8V/3.3V, which can configure 1.8V and 3.3V voltage.

2.2.2 GPIO driver capacity

For RK3358J, GPIO provides 4 level driver strengths, which are 2mA, 4mA, 8mA and 12mA. The default driver strength is different for different GPIO type. Please refer to the datasheet to change the confirgure.

2.2.3 GPIO power

GPIO power pins are described as below:

Table 2-2 RK3358J GPIO power pin description

power domain	GPIO type	Pin name	description
PMUIO1	1.8V/3.3V	PMUIO_VDD_1V0	1.0V logic power for this GPIO domain (group).
		PMUIO1	1.8V or 3.3V IO supply for this GPIO domain (group).
PMUIO2	1.8V/3.3V	PMUIO2	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO1	1.8V/3.3V	VCCIO1	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO2	1.8V/3.3V	VCCIO2	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO3	1.8V/3.3V	VCCIO3	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO4	1.8V/3.3V	VCCIO4	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO5	1.8V/3.3V	VCCIO5	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO6	1.8V/3.3V	VCCIO6	1.8V or 3.3V IO supply for this GPIO domain (group).

2.2.4 GPIO M0 M1的定义

The suffix of M1 and MO in the pin name indicates that the signal is drawn to two different PIN pins and can not be used at the same time.

3 Schematic design suggestion

3.1 minimum system design

3.1.1 clock circuit

RK3358J system clock consists of the chipset internal oscillator circuit and the external 24MHz crystal, shown as picture 3-1.

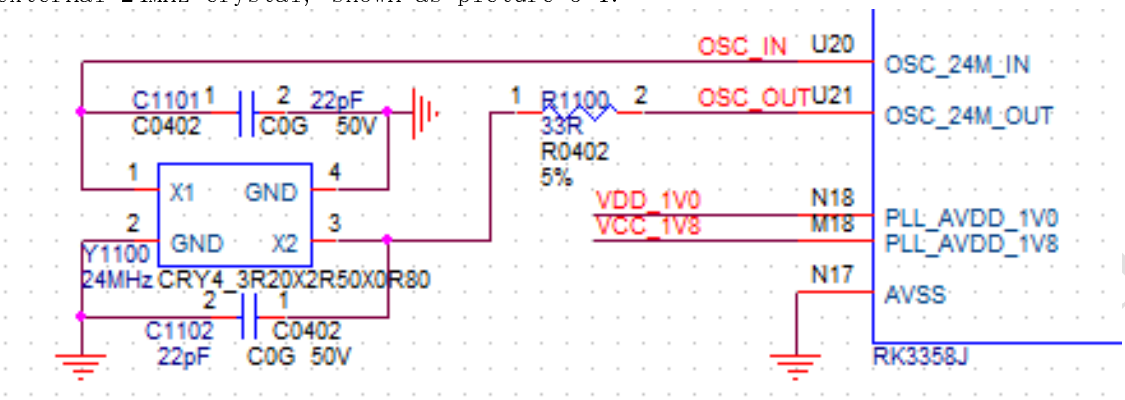


Figure 3-1 RK3358J crystal connection method and component parameter

注意Note

Need to choose the capacitor C1101, C1102 according to the crystal actual loading capacitance value. 22pF is just a sample, not the universal value.

Besides, the system clock can be provided by external active crystal oscillator, input through XIN_OSC pin, the clock parameter is shown as Table 3-1:

Table 3-1 RK3358J 24MHz clock requirement

parameter	standard			description
	min	max	unit	
frequency	24.000000		MHz	
frequency tolerance	+/-20		ppm	Frequency tolerance
working temp.	-20	70	℃	
ESR	/	40	Ohm	

RK3358J will switch the internal clock source to external 32.768KHz clock while in standby, in order to reduce the system power consumption by reducing the system clock frequency. The signal can be obtained from PMIC or external RTC clock ~~source~~circuit, shown as picture 3-2.

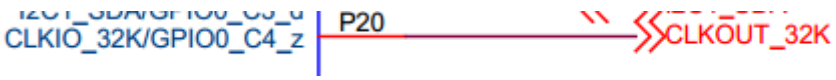


Figure 3-2 RK3358J clock input in standby

The external 32.768KHz RTC clock parameter is shown as table 3-2:

Table 3-2 RK3358J 32.768KHz clock requirement

parameter	standard			description
	min	max	unit	

frequency	32.768000		kHz	
frequency tolerance	+/-30		ppm	Frequency tolerance
working temp.	-20	70	℃	
duty ratio	50		%	

3.1.2 reset circuit

RK3358J internally integrates POR(power on reset) circuit, which is effective for low level. Capacitor C1100 is used to eliminate jitter. Please put it close to RK3358J in layout. The shortest reset time to ensure the chipset working stably and normally is 100 cycles 24MHz main clock period, that is 4us at least.

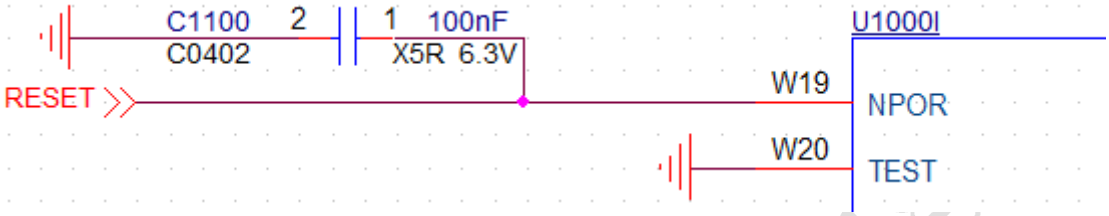


Figure 3-3 RK3358J reset input

3.1.3 system bootup sequence

RK3358J system bootup sequence priority from high to low is as below:

- Nand FLASH
- eMMC FLASH
- SFC/SPI FLASH
- SDMMC CARD
- USB OTG

So please remember for the product design, DO NOT connect the external memory device to the interface with higher priority than file system interface before the system bootup, or it will affect the system normal bootup.

3.1.4 system initialization config signal

RK3358J has two important signals, IO voltage of VCCIO6(FLASH) power domain and JTAG/SDMMC reused function control pin. They need to be configed by hardware before power on.

RK3358J VCCIO6 power domain's IO voltage mode needs to be configed as it belongs to FLASH power domain. It will be used during system bootup, so must specify default voltage mode through hardware config during system bootup instead of adjusting through register operation. The config is shown as table 3-3.

In order to reduce IO number, RK3358J reuses JTAG function and SDMMC function. Need to switch the output through the pin. The config is shown as table 3-3:

Table 3-3 RK3358J system initialization config signal description

signal name	pin	Internal pull up/down	description
FLASH_VOLSEL	R19	pull up	FLASH(VCCIO6)power domain driver strength choice, only effective when power on: 1: IO voltage mode is 1.8V; 0: IO voltage mode is 3.3V(default);
SDMMC0_DET	AA20	pull up	JTAG pin reuse choice control sig 0: rognized as sd inserted, SDMMC/JATG/UART pin reused as SDMMC output;

			1: recognized as sd card not inserted, SDMMC/JATG/UART pin reused as JTAG/UART output(default);

3.1.5 JTAG debug circuit

RK3358J chipset JTAG interface conforms to IEEE1149.1 standard. PC can connect DSTREAM simulator through SWD mode(two wire mode) to debug ARM core inside the chipset.

Before connecting simulator, need to ensure that SDMMC0_DET pin is with high voltage, otherwise cannot enter JTAG debug mode. Interface description is shown as table 3-4:

Table 3-4 JTAG debug interface signal

Signal name	pin	description
JTAG_TCK	AA19	AP JTAG clock input
JTAG_TMS	AA16	AP JTAG mode choice input

3.1.6 DDR circuit

- **3.1.6.1 DDR controller introduction**

RK3358J DDR controller interface supports JEDEC SDRAM standard interface. The controller has below features:

- Support DDR3/DDR3L/DDR4/LPDDR2/LPDDR3;
- Provide one 32 bit DDR controller interface, support data bus bitwidth 32 bit/16 bit configurable, address bus support up to 16bit max.
- Support DDR 4GB max.
- Support power down, self refresh etc. low power consumption mode;

- **3.1.6.2 DDR topology structure and connection method**

RK3358J SDRAM topology structure is shown as picture 3-4, taking DDR3 as an exemple:

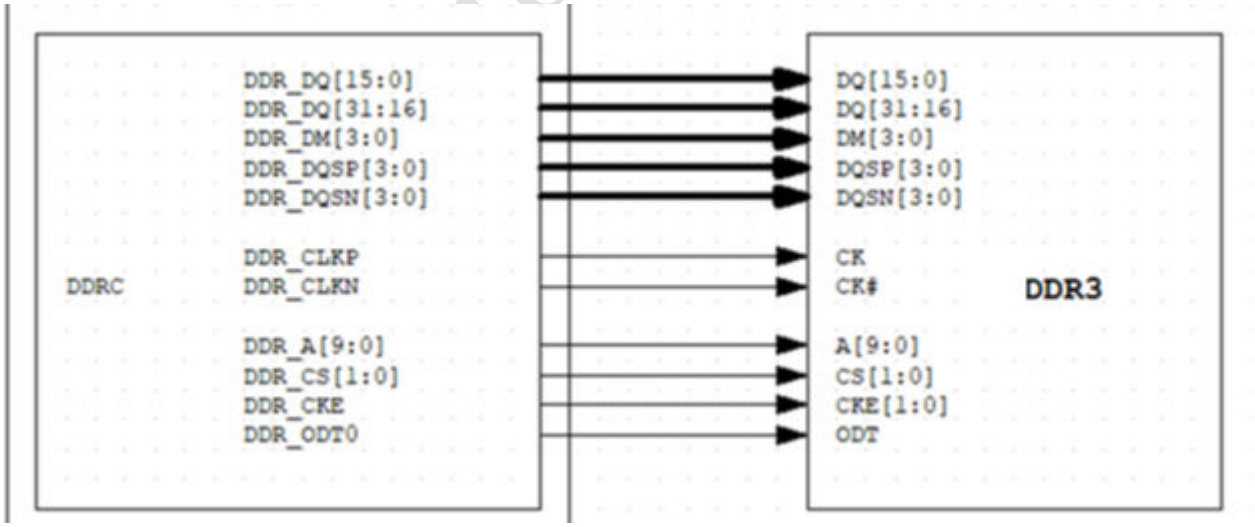


Figure 3-4 SDRAM topology structure picture

- **3.1.6.3 DDR power up sequence requirement**

RK3358J DDR controller only includes one set of power, so there is no power up sequence:

- DDRIO_VDD: DDR controller core power supply, interface I/O power supply and buffer power

DRAM power up sequence refers to JEDEC standard, taking DDR3 DRAM power up sequence

as an exemple shown as below:

After...	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2}—200mV
	V_{DD1} and V_{DD2} must be greater than V_{DDCA}—200mV
	V_{DD1} and V_{DD2} must be greater than V_{DDQ}—200mV
	V_{Ref} must always be less than all other supply voltages

Figure 3-5 DDR3 DRAM power up sequence

- **3.1.6.4 DDR support list**

RK3358J DDR interface supports DDR3/DDR3L/DDR4/LPDDR2/LPDDR3 and the max working frequency up to 800MHz. Please refer to 《RK DDR Support List》 for details.

3.1.7 emmc circuit

- **3.1.7.1 emmc controller introduction**

RK3358J emmc interface supports 5.0 and 5.1 protocol and is also compatible with 4.41 and 4.51 components. The controller has below features:

- Support SFC FLASH, nand flash and emmc flash;
- Support 1-bit, 4-bit and 8-bit three kinds of data bus width;
- Support HS200 mode but not support CMD Queue;

- **3.1.7.2 emmc topology structure and connection method**

Emmc interface supports interface pull up/down and matching design is recommended as below table 3-5:

Table 3-5 RK3358J eMMC接口设计

signal	internal pull up/down	connection	Description(chipset)
eMMC_DQ[7:0]	pull up	direct connection	emmc data sending/receiving
eMMC_CLK	pull up	Series connection 22ohm resistor	emmc clock sending
eMMC_CMD	pull up	Direct connection	emmc command sending/receiving

- **3.1.7.3 emmc power up sequence requirement**

RK3358J emmc controller only includes one set of power, so there is no special requirement:

- VCCIO0: emmc controller I/O power;
  emmc component power up sequence refers to JEDEC standard:
- VCC and VCCQ have no power up sequence requirement;
- VCC and VCCQ must be powered up and keep stale working voltage befor RK3358J sending out CMD command;

- After the component enters sleep mode, RK3358J can cut off VCC power to lower power consumption
- Before the component is waken up from sleep mode, VCC power must be on and keep stable working voltage;

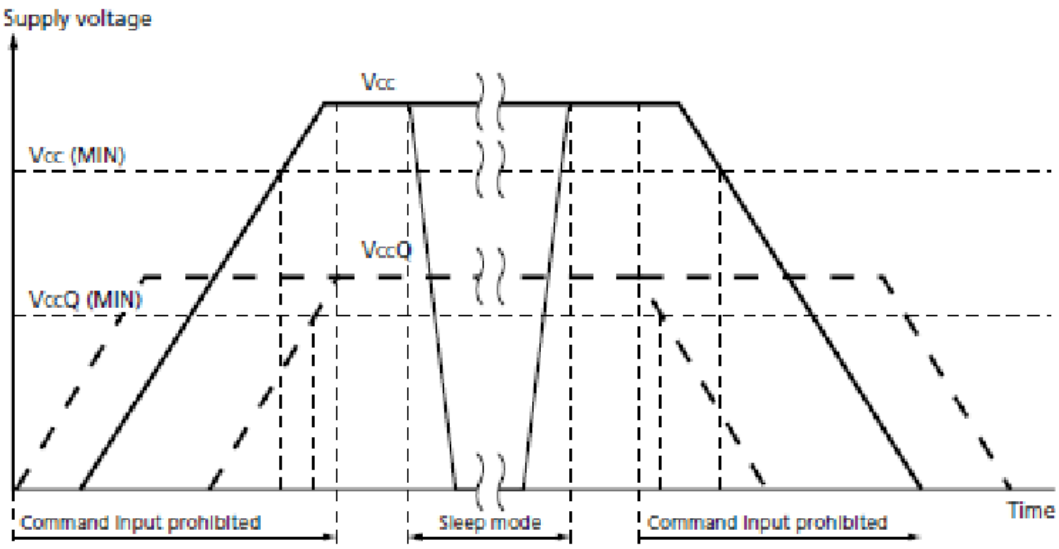


Figure 3-6 emmc component power up/down sequence

- **3.1.7.4 emmc support list**

RK3358J emmc interface support component refers to the document《RK eMMCSupportList》.

3.1.8 SPI circuit

- **3.1.8.1 SPI controller introduction**

RK3358J has two SPI controllers to connect SPI devices and SPI0 can be used as boot.

- **3.1.8.2 SPI topology and connection**

SPI interface pull up/down and matching design recommendation are shown as table 3-6

Table 3-6 RK3358J SPI interface design

signal	Internel pull up/down	Connection method	Description(chipset)
SPI0_MOSI	pull down	direct connection	SPI data sending
SPI0_MISO	pull up	Direct connection	SPI data receiving
SPI0_CLK	pull up	Series connection 22ohm resistor	SPI clock sending
SPI0_CSN	pull up	Direct connection	SPI chip select signal

- **3.1.8.3 SPI power up sequence requirement**

SPI controller power up requirement complies with GPIO power domain's power up requirement.

SPI flash only has one set of power, so there is no requirement for power up

sequence.

3.1.9 nand flash circuit

RK3358J supports flash memory device, such as nand, inand etc.

If using nand, shown as below picture: when use Toshiba and sandisk ddr mode nand flash, need to connect U4000 pin28 and pin45 to VCCIO_FLASH for power supply, which means R4001 and R4005 should use 0R resistor.

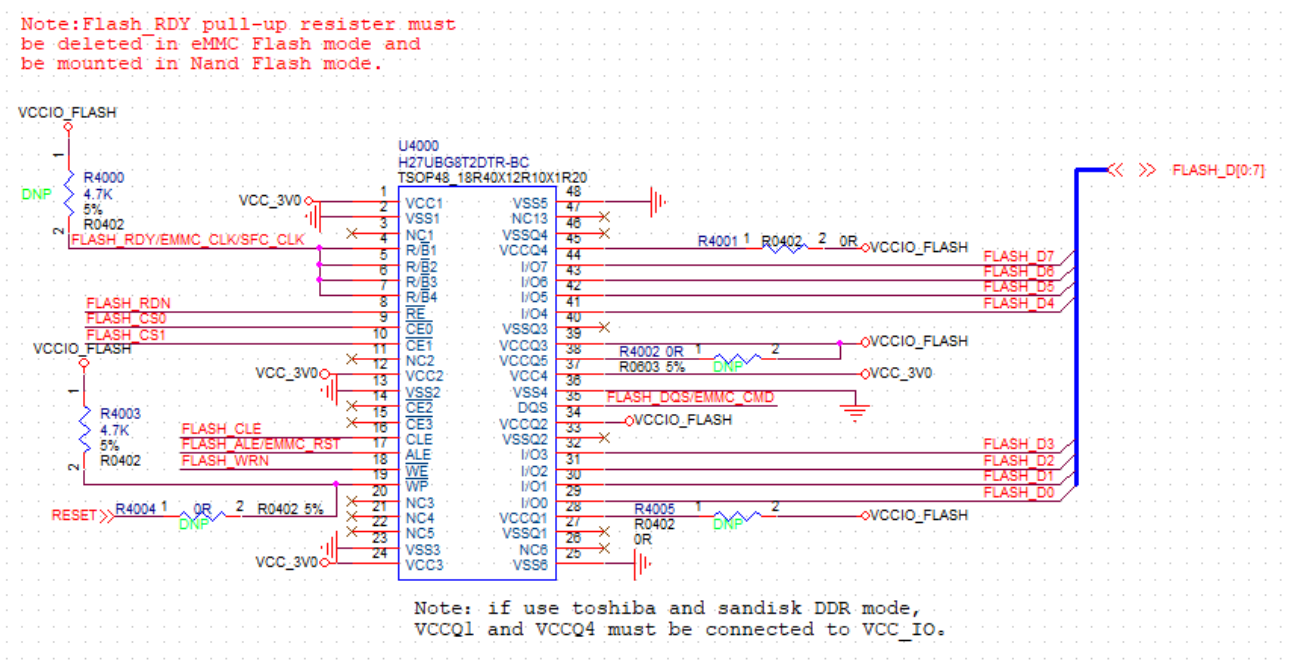


Figure 3-7 nand flash circuit

Note: RK3358J FLASH WP function pin is not pull out. You can use reset signal to get WP function.

3.2 power design

3.2.1 minimal system power introduction

- **3.2.1.1 power requirement**
  - PLL: PLL_AVDD_1V0、PLL_AVDD_1V8
  - CPU: VDD_ARM
  - LOGIC&GPU: VDD_LOG
  - DDR: VCC_DDR
  - GPIO: PMUIO_VDD_1V0、PMUIO1、PMUIO2

- **3.2.1.2 power up sequence**

Theoretically comply with the principle: for the same module, power up from low voltage to high voltage, and the same voltages power up at the same time. There is no power up requirement among different modules.

reference power up sequence is recommended as below:

PLL_AVDD_1V0&PMUIO_VDD_1V0&VDD_LOG->VDD_CPU->PLL_AVDD_1V8->VCC_DDR->PMUIO1&PMUIO2

Need to make sure VDD_LOG voltage is powered up first.

3.2.2 power design suggestion

- **3.2.2.1 standby circuit solution**

RK3358J board consists of constantly power supply area and power off in standby area which are powered separately as shown in picture 3-9.

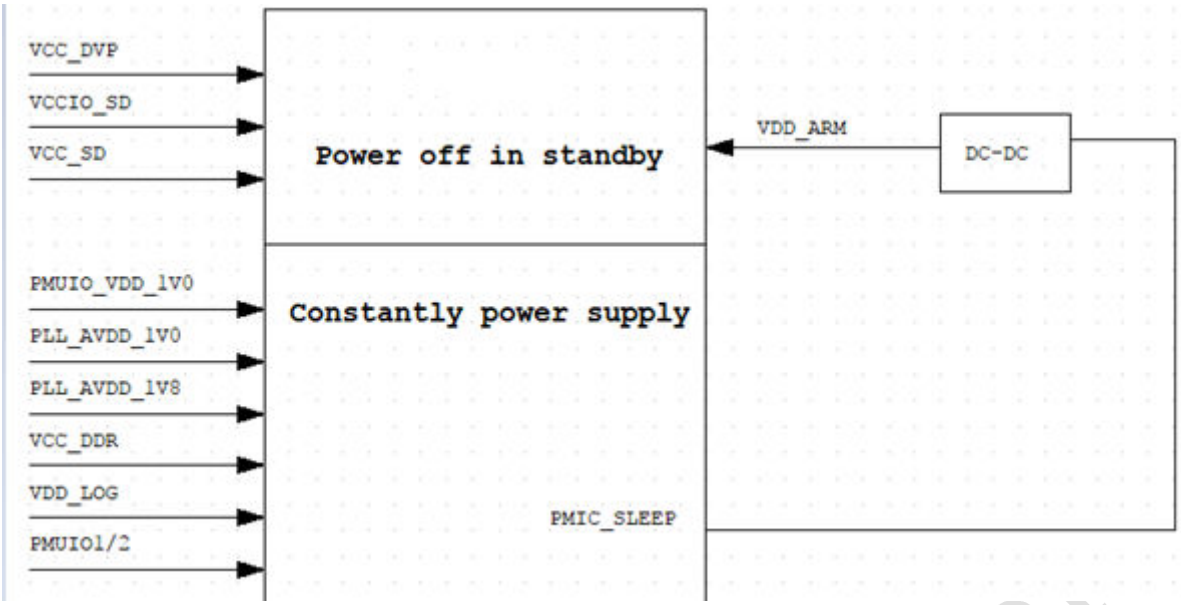


Figure 3-8 RK3358J standby circuit solution

For power off in stanby area, it is controlled by PMIC to cut off each independent power supply and through PMIC_SLEEP_H to control MOS switch circuit to cut off power supply in standby mode.

For constantly power supply area, the power is supplied directly by power chip. Need to keep below four set of power on at least in standby mode:

- supply power for DDR self refresh
- supply power for PMUIO1 & PMUIO2 power domain to keep output status and interrupt response
- supply power for logic core of PMUIO1 & PMUIO2 power domain
- supply power for PLL and CPU OSC working

- **3.2.2.2 PLL power**

RK3358J has 6 PLL inside the chip allocated as below:

Table 3-7 RK3358J internal PLL introduction

	quantity	power	standby status
PMU/OSC	1	PMU_VDD_1V0、PMUIO1	Do not power off
modules inside the chip	5	PLL_AVDD_1V0，PLL_AVDD_1V8	Do not power off

Recommend to use LDO to supply power for PLL. Specifically because DDR working frequency is relatively high, stable PLL power is helpful to improve the working stability with high frequency and the decoupling capacitor should be put close to the pin.

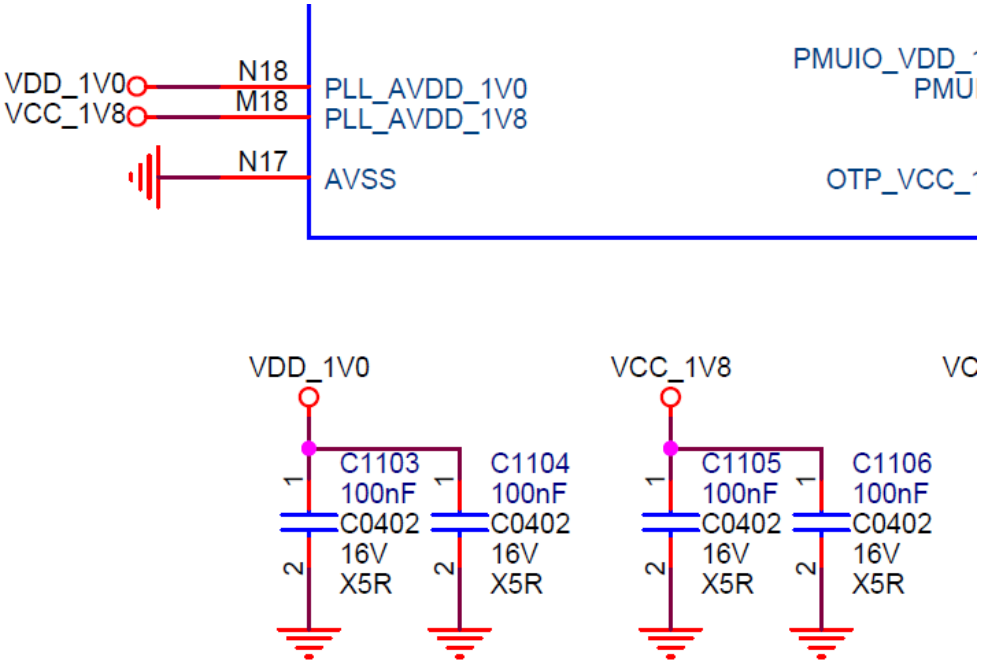


Figure 3-9 RK3358J chip PLL power

- **3.2.2.3 CPU power**

RK3358J uses independent power domain to supply power for CPU. VDD_ARM supply power for Cortex-A53 core shown as below picture. Support DVFS dynamic voltage and frequency scaling fuction, use DC-DC to supply power independently, the peak current can reach up to 1.2A separately, so please do not delete or reduce the capacitors in the RK3358J reference design schematic. For layout, put the big capacitor in the back side of RK3358J chip (put it close to the chip if only one side) to ensure the power ripple within 100mV in case the power ripple becomes too big with heavy loading. The capacitor is shown as picture 3-11.

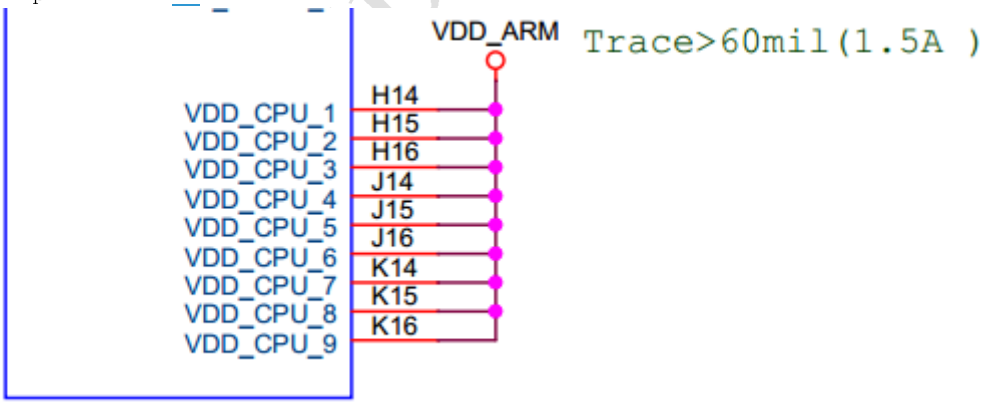


Figure 3-10 RK3358J VDD_CPU power

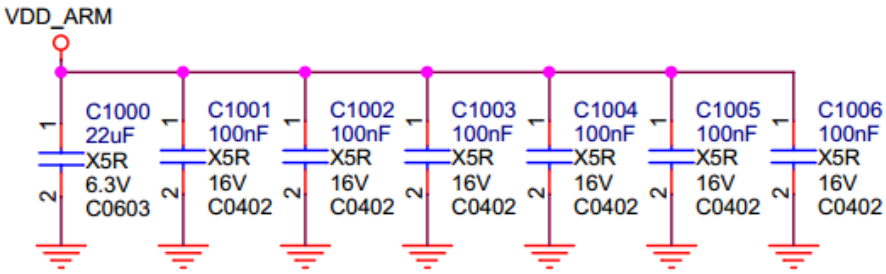


Figure 3-11 RK3358J VCC_CPU power decoupling

- **3.2.2.4 GPU & LOGIC power**

RK3358J uses DC-DC to supply power for GPU & LOGIC separately, VDD_LOG as shown in below picture, supports DVFS dynamic voltage and frequency scaling function, the peak current can reach up to 1.1A, so please DO NOT delete or decrease the capacitors required in the reference design schematic. For layout, put the big capacitor in the back side of RK3358J chip (put it close to the chip if only one side) to ensure the power ripple within 100mV in case the power ripple becomes too big with heavy loading. The capacitor is shown as picture 3-13.

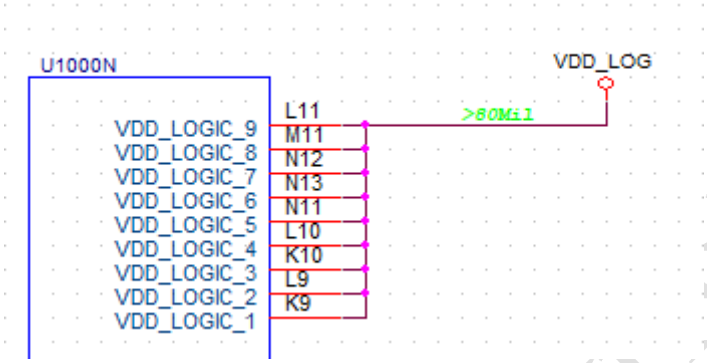


Figure 3-12 RK3358J VDD_GPU power

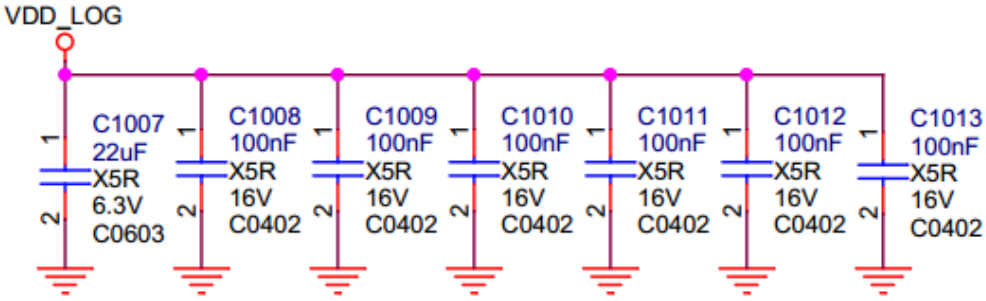
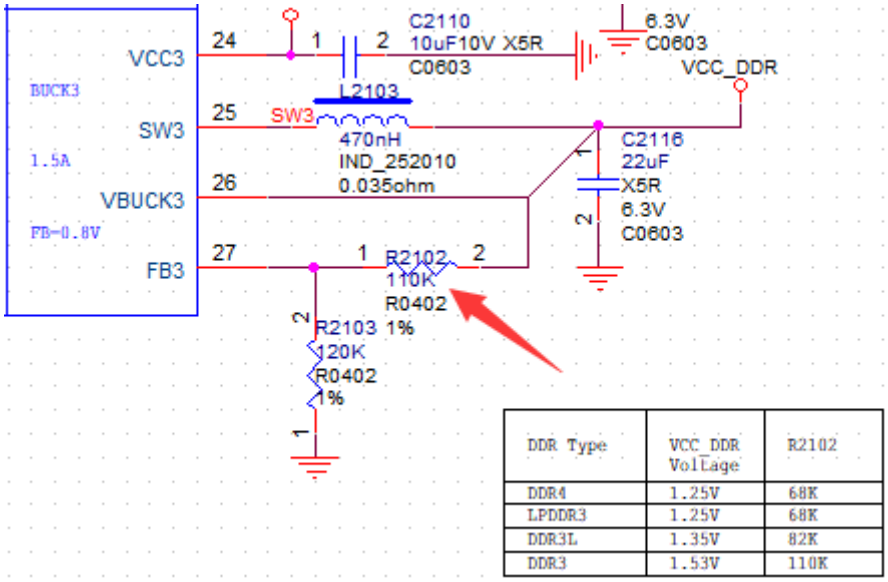


Figure 3-13 RK3358J VDD_GPU power decoupling

- **3.2.2.5 DDR power**

RK3358J DDR controller supports various types of DDR, such as DDR3/DDR3L/DDR4/LPDDR2/LPDDR3. For product design, adjust divider resistance and confirm RK809 BUCK3 output voltage according to the actual use case.



DDR Type	VCC_DDR Voltage	R2102
DDR4	1.25V	68K
LPDDR3	1.25V	68K
DDR3L	1.35V	82K
DDR3	1.53V	110K

Figure 3-14 RK3358J DDR controller power

DDR controller internally integrates Vref circuit and generates reference voltage for controller: VCC_DDR/2. In DDR/LPDDR3 DRAM side Vref_CA=VCC_DDR/2, but Vref_DQ is adjusted by ODT strategy, the corresponding Vref voltage can be adjusted according to driver strength and ODT value.

For example: using LPDDR3, with 800MHz, RK3358J chip side driver strength is 34.3ohm, DRAM side ODT is 240ohm, so when ODT is enabled, DRAM Vref=0.56*VCC_DDR calculated by the formula.

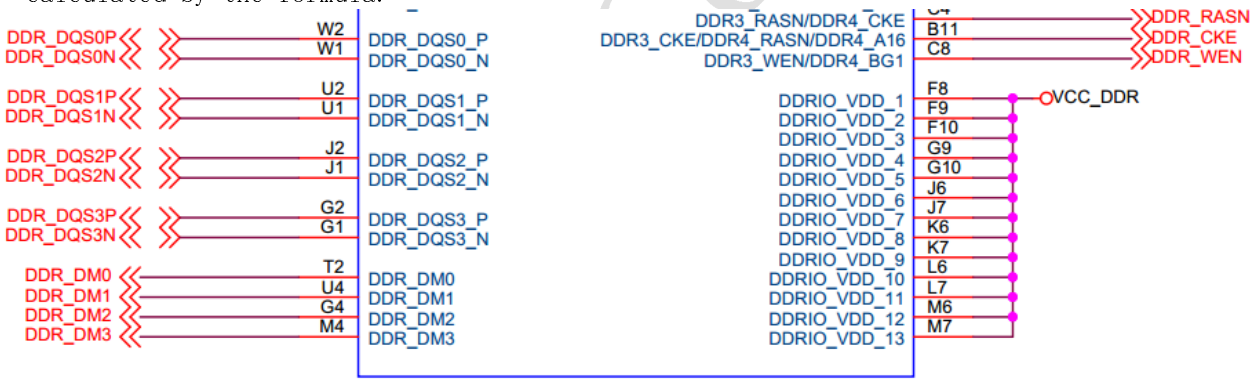


Figure 3-15 RK3358J DDR controller power

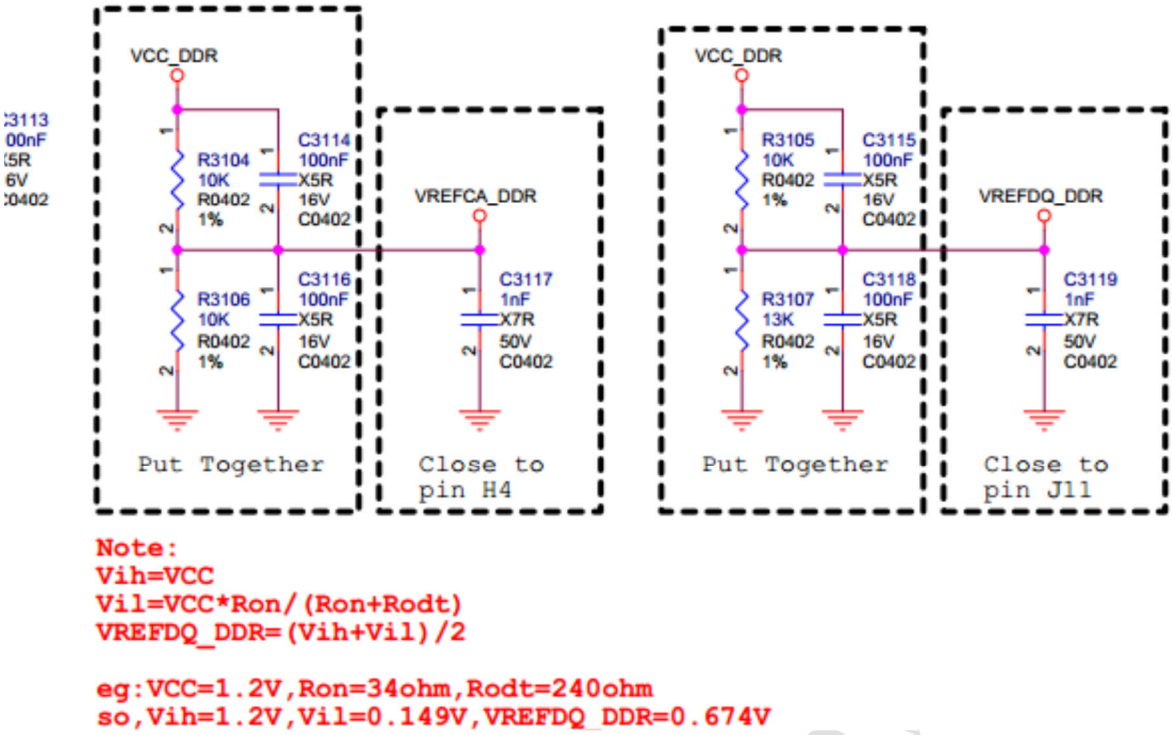


Figure 3-16 RK3358J LPDDR3 DRAM VREF power design

Note

Vref_DQ design for various types of DDR components:

LPDDR2 doesnot support ODT function; DDR4 Vref_DQ is adjusted inside the DDR parts; while DDR3/DDR3L ODT function is enabled, it will pull up/down simultaneously internally, Vref_DQ=Vref_CA=VCC_DDR/2; Only LPDDR3 needs to adjuct Vref_DQ externally.

- **3.2.2.6 GPIO power**

GPIO power refers to chapter 2.3.1. Suggest put a 100nF decoupling capacitor for every pin and put it close to the power supply pin. For more details please refer to RK3358J chip reference design schematic.

3.2.3 RK809-1 solution introduction

- **3.2.3.1 RK809-1 block diagram**
-

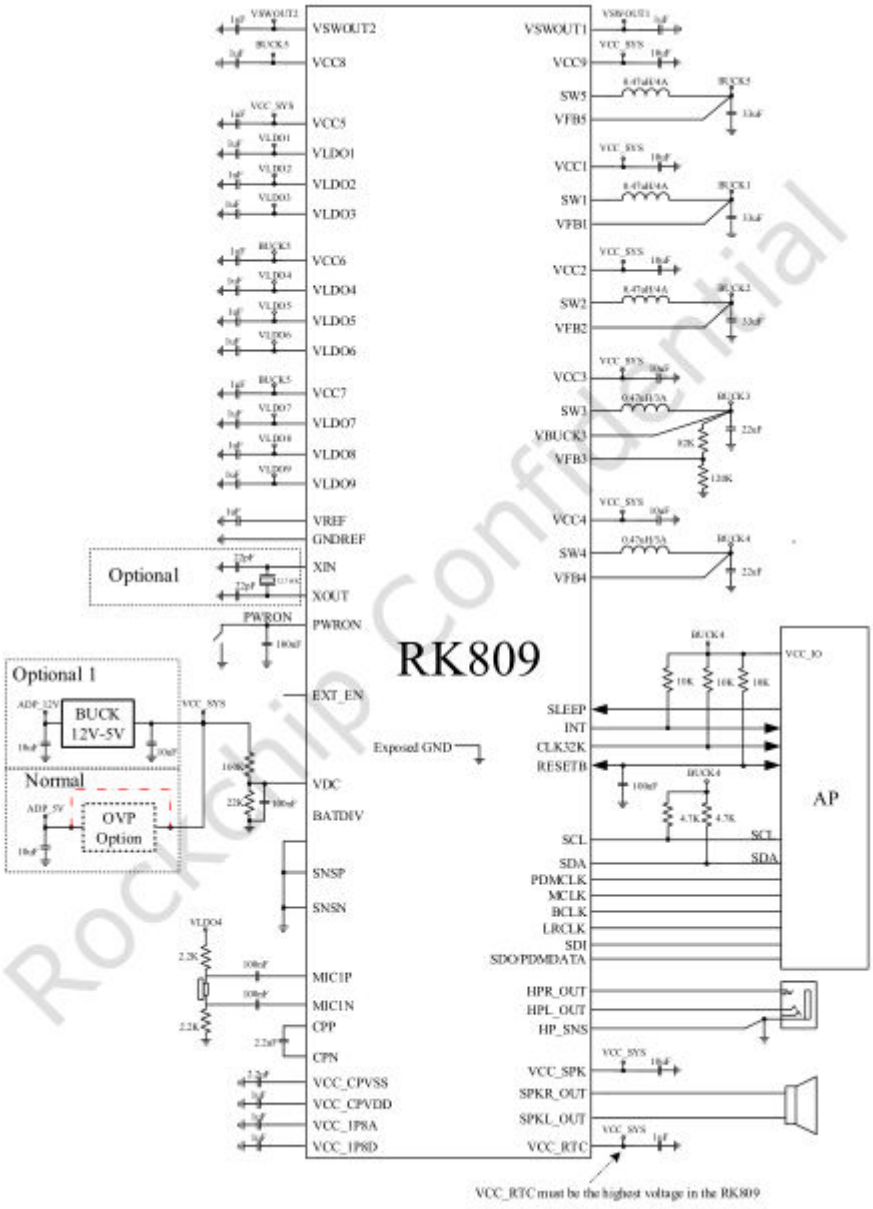


Figure 3-17 RK809-1 block diagram

- 3.2.3.2 RK809-1 characteristics
  - input range: 3.8V-5.5V
  - built-in precise fuel gauge
  - (RTC) built-in real time clock
  - 16uA very low standby current(with 32kHz clock frequency)
  - field ear driver
  - 1.3W Class D amplifier without filtering inductance
  - fixed and programmable choosable power bootup sequence control
  - built-in high performance audio encoder and decoder
    - buit-in independent PLL
    - support microphone input
    - support programmable digital and analog gain
    - support 16bits-32bits bit rate
    - sampling rate up to 192kHz
    - firmware supports master and slave working mode config
    - support 3 kinds of I2S format(standard, align left, align right)
    - support PDM mode(external input PCLK)

- power supply
  - Channel 1: synchronous step-down DC-DC converter, 2.5A max
  - Channel 2: synchronous step-down DC-DC converter, 2.5A max
  - Channel 3: synchronous step-down DC-DC converter, 1.5A max
  - Channel 4: synchronous step-down DC-DC converter, 1.5A max
  - Channel 5: synchronous step-down DC-DC converter, 1.5A max
  - Channel 6-7, 9-14: low dropout linear regulator, 400mA max
  - Channel 8: low dropout linear regulator with low noise and high power supply rejection ratio ,100mA max
  - Channel 15: OTG switch, 1.5A max
- 封装：Package: 7mmx7mm QFN68

- 3.2.3.3 RK3358J+RK809-1 Power Tree

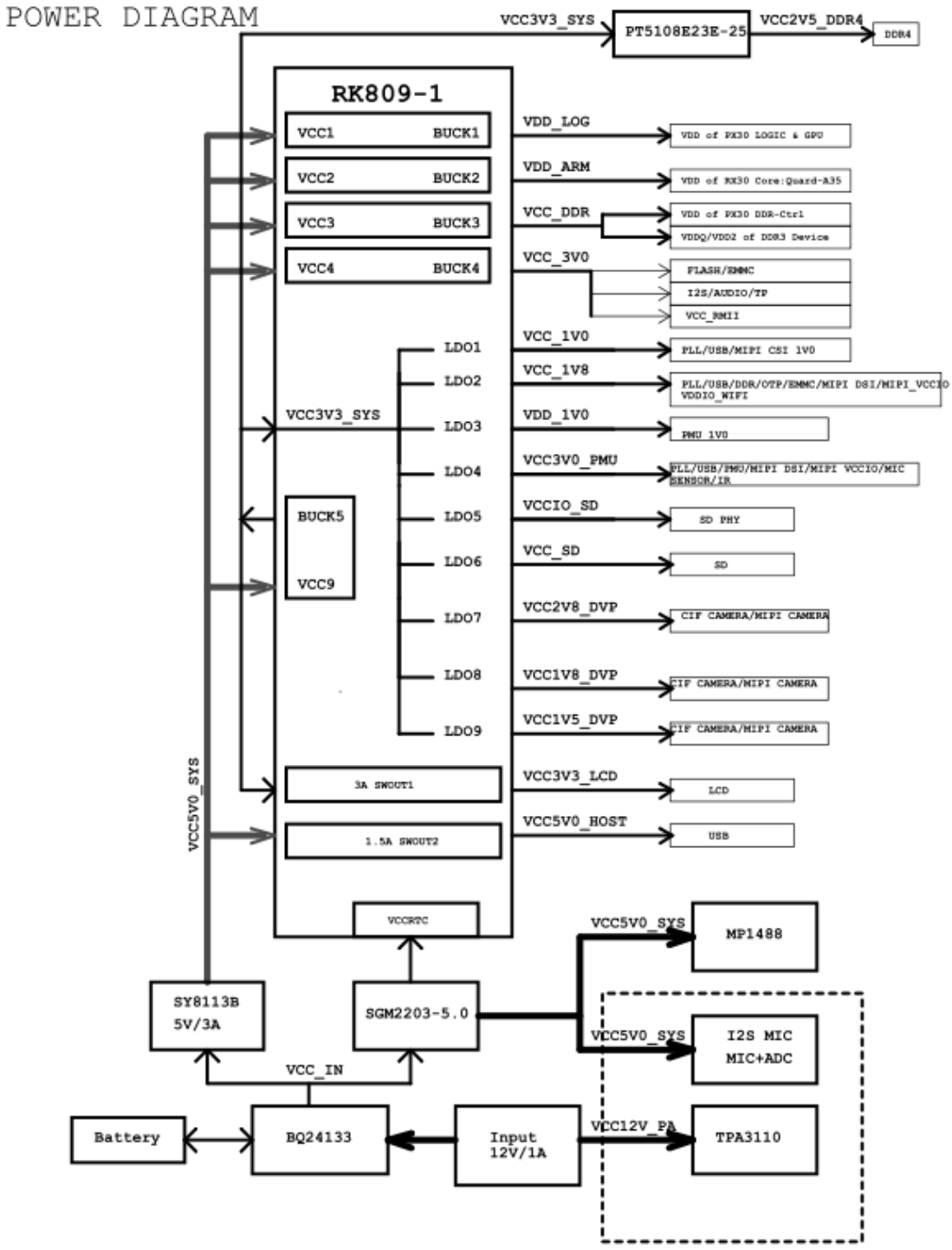


Figure 3-18 RK809-1 power structure

- **3.2.3.4 RK809-1 default power up sequence chart**

			RK809-1	
	Range of output voltage	Maximum output current	Default voltage	Start up sequence
BUCK1	0.5V-2.4V	2.5A	1.0V	2
BUCK2	0.5V-2.4V	2.5A	1.0V	2
BUCK3	X(external divided resistor) Or 0.5V-2.4v(internal divided resistor)	1.5A	x	4
BUCK4	0.5V-3.4V	1.5A	3.0V	5
LDO1	0.6V-3.4V	400mA	2.5V	3
LDO2	0.6V-3.4V	400mA	1.8V	3
LDO3	0.6V-3.4V	400mA	1.0V	2
LDO4	0.6V-3.4V	100mA	3.0V	5
LDO5	0.6V-3.4V	400mA	3.0V	5
LDO6	0.6V-3.4V	400mA	3.0V	5
LDO7	0.6V-3.4V	400mA	2.8V	OFF
LDO8	0.6V-3.4V	400mA	1.8V	OFF
LDO9	0.6V-3.4V	400mA	1.5V	OFF
BUCK5	1.5V-3.6V	2.5A	3.3V	1
SWOUT1				OFF
SWOUT2				OFF

Figure 3-19 RK809-1 default power up sequence chart

BUCK4 and LDO4, LDO5, LDO6 default output values are all 3.0V and can be adjusted to 3.3V by program after system bootup if needed.

- **3.2.3.5 RK809-1 notice**

- ■ VCC_RTC power must be supplied and the voltage must be the highest among the RK809-1 other power supply;
  - ■ The 32.768 crystal matching capacitor value recommend to use 22pF. User can fine tune the parameter according to the crystal specification.

Note

In otder to reduce the consumption PMIC RTC crystal oscillation usually is weak, it is not able to measure the oscillation signal in XOUT or XIN pin using normal oscilloscope, or the oscillation will stop once the probe touch it. Please use CLK32K pin if need to measure 32.768k signal.

  - ■ BUCK1 and BUCK2 output capacitor must be over 30uF to guarantee the good decoupling effect, especially in high current and heavy loading cases, it is better to increase the output decoupling capacitor value.
  - ■ RK809-1 supports built-in USB OTG power supply function, short circuit protection function and 1.0-1.5A configurable output current limitted;
  - ■ PWRON pin built in a pull up resistance which pull up to VCCRTC, when the low

level time is detected over 500ms, will power up automatically; If PWRON pin is pull down over 6s after power up, will force to power off(usually used to forcely power off and then power on after system crash); During standby and wake up operation, PWRON pin should keep low level for more than 20ms.

- RK809-1 basic working condition
  - VSYS bigger than 3.3V;
  - RK809-1 will power up automatically when detecting any one of below two cases: PWRON pin keeps low voltage for 500ms; Internl RTC Alarm power up is enabled and the time is up.
  - Start power up process, every timing interval is 2ms, the next timing will continue only after the former one voltage output meets the requirement, until all the timings power up, release reset, and then finish the process.

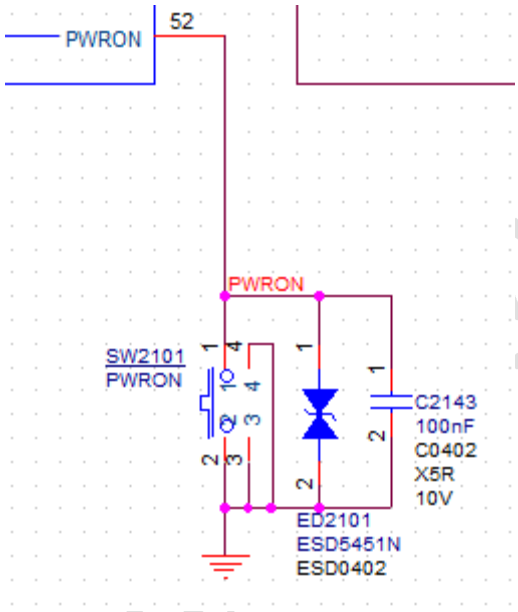


Figure 3-20 RK809-1 PWRON pin

- RK809-1 will power off automatically if detect any of below two cases:
  - I2C write DEVICE_OFF=1;
  - PWRON pin keeps low level over 6s
- when RK809-1 starts power off process, it will pull down reset in one RTC clock cycle, then cut off all power output simultaneously in 2ms, and then finish the process.

3.2.3.6 RK809-1 design introduction

RK809-1具体设计说明，请参考RK PMIC相关设计文档《RK809 应用指南》For RK809-1 design details, please refer to RK PMIC relative design document<RK809 application guide>

3.2.4 others

3.2.4.1 over temperature protection circuit

When RK3358J chip`s temperature is too high, crash or in other abornal situations, TSADC_SHUT pin will output low level, reset RK809-1, control the power to down and clear the whole registers, and then restart,

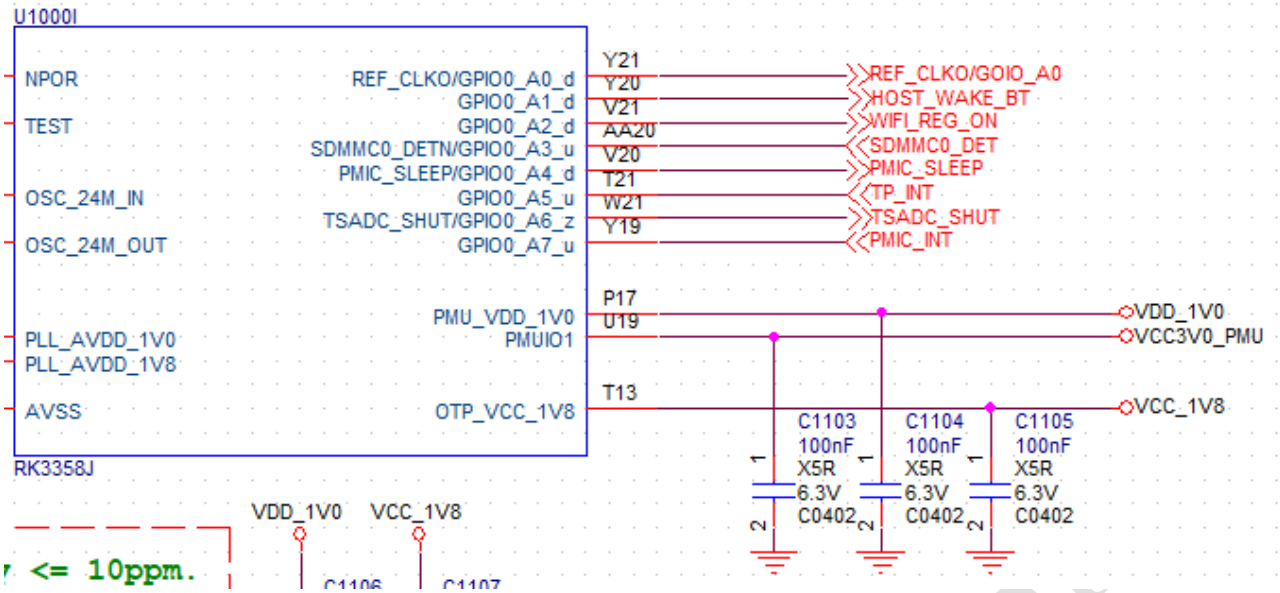


Figure 3-21 RK3358J OTP_OUT over temperature protection output

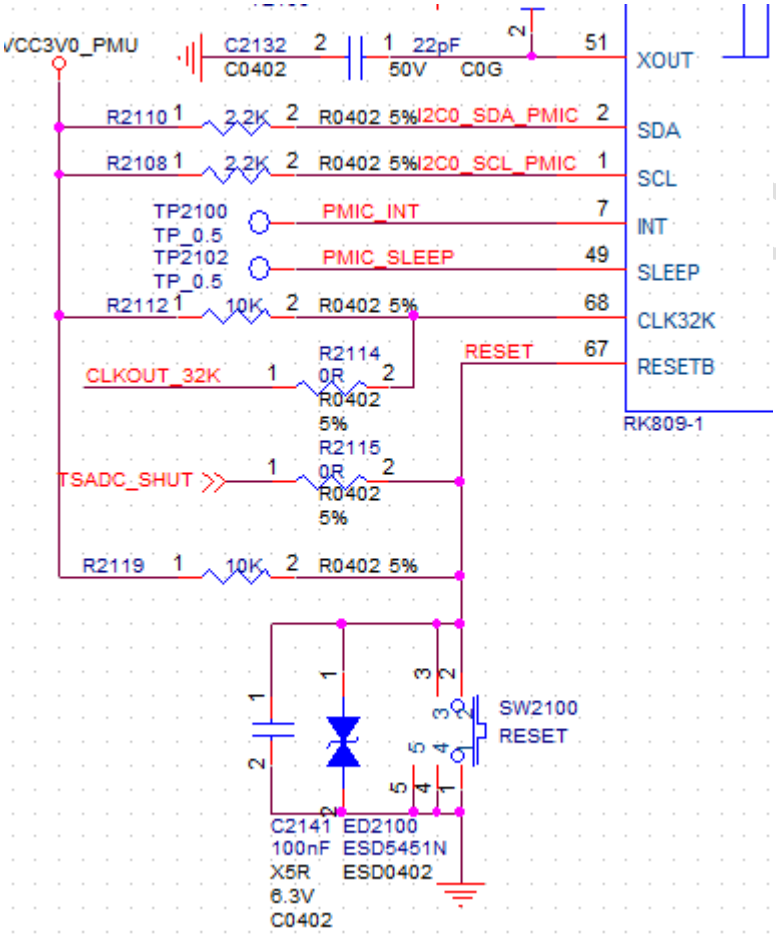


Figure 3-22 PMIC OTP_OUT over temperature protection input

- **3.2.4.2 PMIC SLEEP circuit**

When RK3358J is in normal working mode, the status pin PMIC_SLEEP will keep low level output.

When system enters standby mode, PMIC_SLEEP pin will output high level sleep indicator signal and at the moment PMIC will enter the standby mode as controlled by the signal. As configured in firmware dts file, some power will be cut off and some will set

down the voltage.

When system is waken up from the standby mode, PMIC_SLEEP pin will output low level first, and then PMIC will restore back to the previous working status and recover all power outputs.

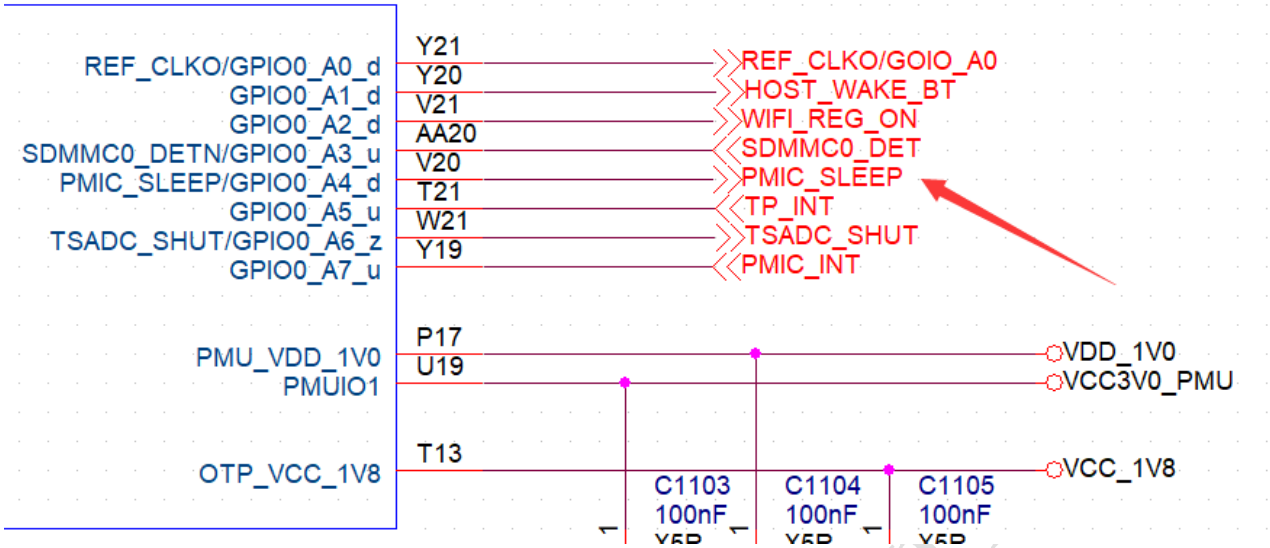


Figure 3-23 RK3358J PMIC_SLEEP output

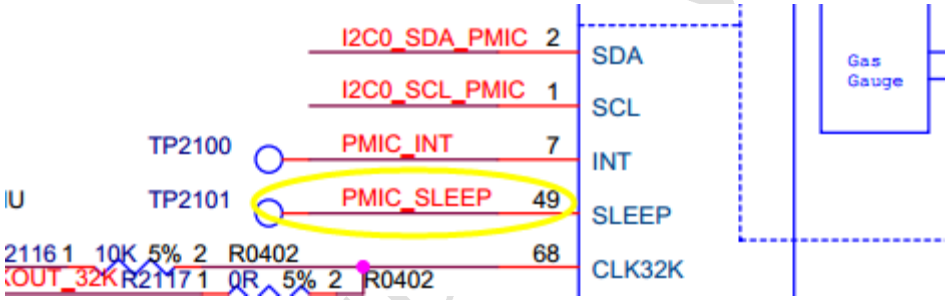


Figure 3-24 PMIC PMIC_SLEEP input

3.2.5 power peak current table

Below table shows the peak current test result in Antutu mode based on RK3358J DEMO device for reference. Test condition is as below:

- CPU max frequency: 1.512GHz
- GPU max frequency: 550MHz
- DDR max frequency: 4x16bit DDR3 K4B4G1646E, 800MHz;
- Oscilloscope enables 20HMz bandwidth limit;

Table 3-8 RK3358J peak current table

PowerName	Voltage (V)	Peak Current(mA)
VCC_SYS	5.16V	1146.00
VDD_ARM	1.35V	894.80
VDD_LOG	1.12V	718.20
VCC_DDR	1.52V	577.70
VCC_3V0	2.94V	75.50
VCC1V0	1.01V	/
VCC_1V8	1.81V	185.80
VDD_1V0	1.0V	12.7
VCC3V0_PMU	3.0V	9.2
VCCIO_SD	3.0V	TBD
VCC_SD	3.0V	TBD

3.3 function interface circuit design guide

3.3.1 memory card circuit

RK3358J provides one SDMMC interface controller which can support SD v3.0 and MMC v4.51 protocol, as shown in picture 3-25:

- SDMMC controller has a standalone power domain;
- SDMMC reuses with UART2, JTAG etc. Choose the function through SDMMC0_DET. Please refer to 3.1.4 for details;
- SDMMC0_VDD is IO power, and the power supply should be 3.3V from external(SD 2.0 mode) or 3.3V/1.8V adjustable(SD 3.0 mode);

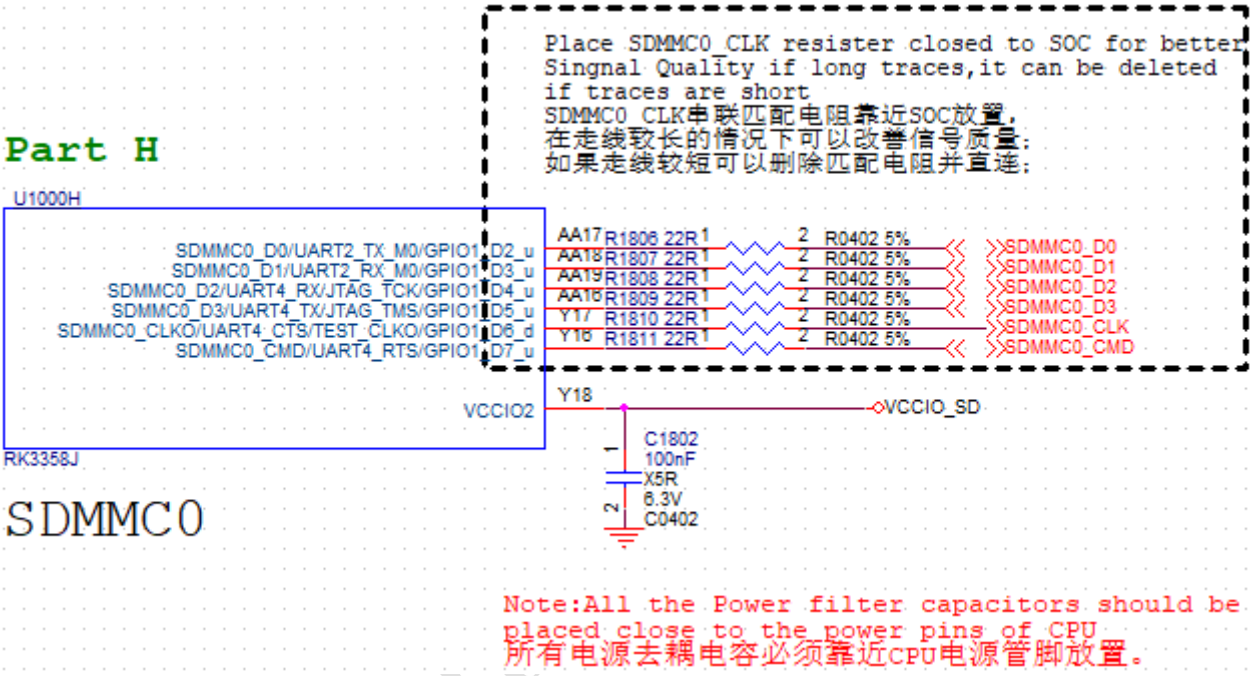


Figure 3-25 RK3358J SDMMC module circuit

SDMMC interface pull up/down and matching design recommendation are shown as below table 3-9.

Table 3-9 RK3358J SDMMC interface design

signal	internal pull up/down	connection method (SDR104 high speed mode)	description(chip side)
SDMMC_DQ[3:0]	pull up	Series 22ohm resisto Can delete if the line is short	SD data sending/receiving
SDMMC_CLK	pull down	series 22ohm resistor	SD clock sending
SDMMC_CMD	pull up	series 22ohm	

		resistor can delete if the line is short	SD command sending/receiving

3.3.2 USB circuit

RK3358J has two set of USB 2.0 interface, one supports OTG mode, and the other is HOST.

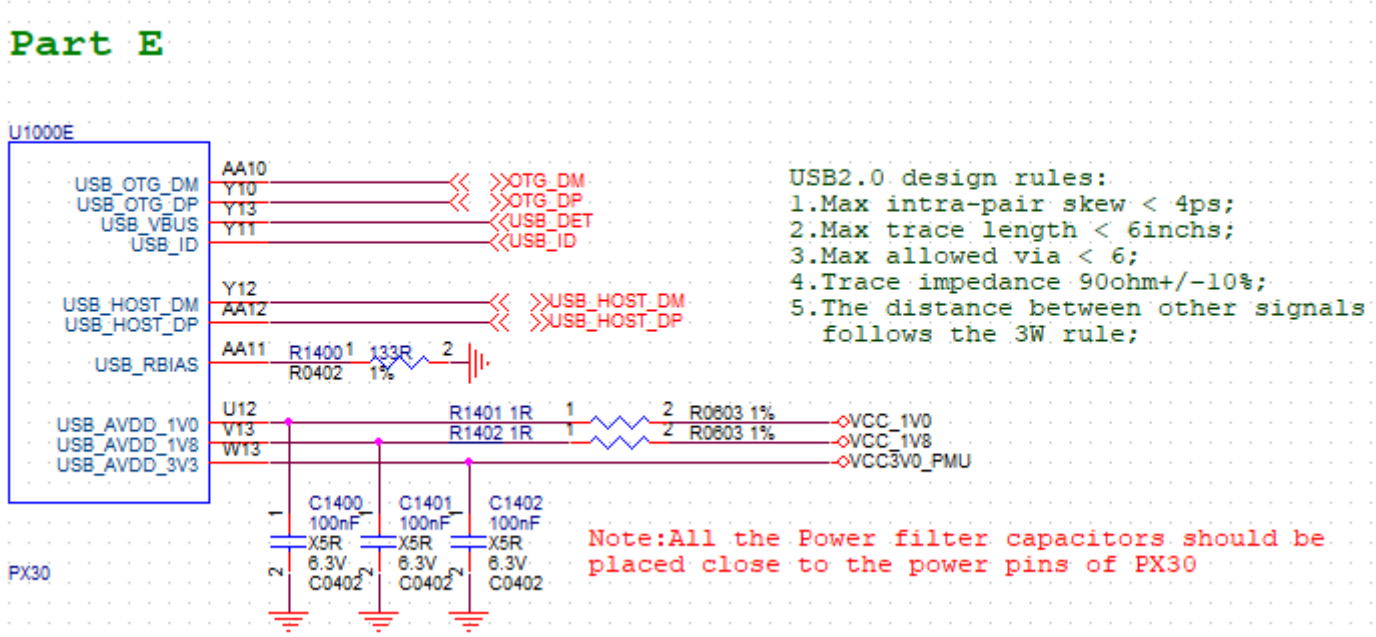
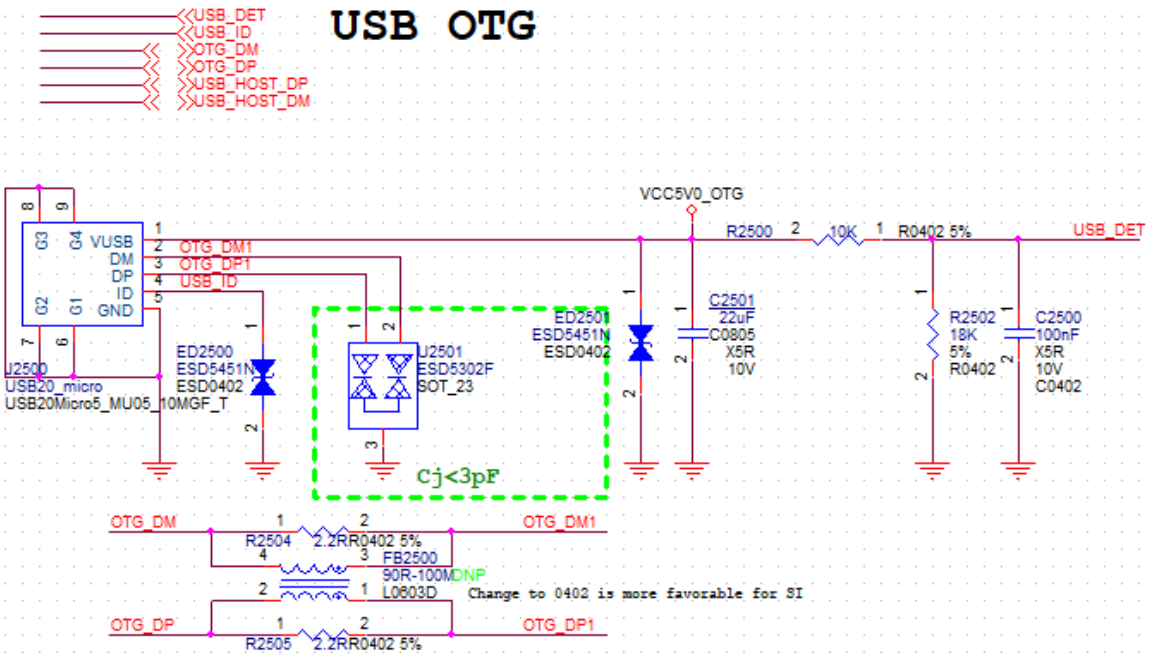


Figure 3-26 RK3358J USB 2.0 module

Design notice:

- USB OTG interface is used as system image flashing port by default, so must reserve interface during design;



-

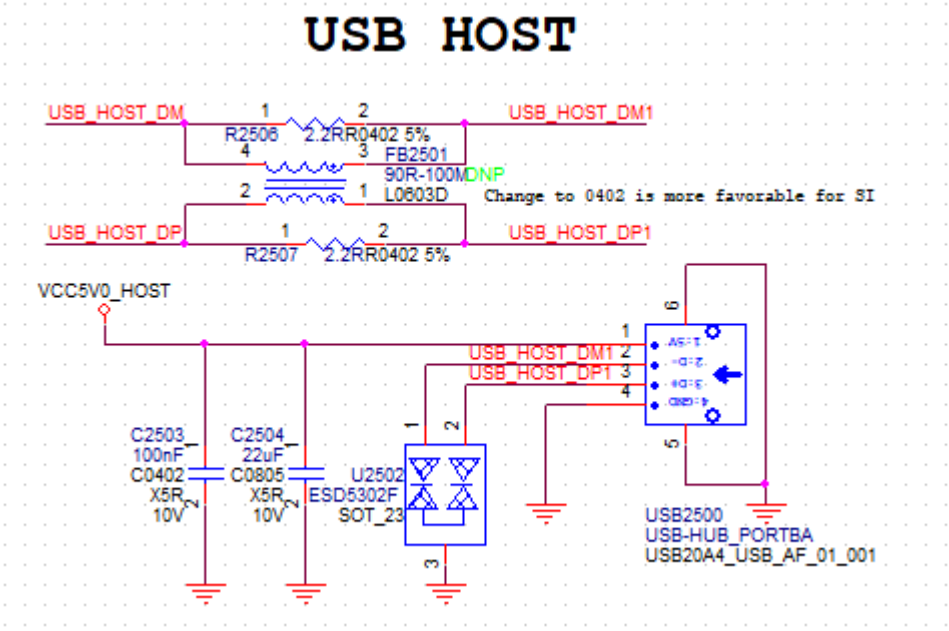


Figure 3-27 RK3358J USB connecting socket

- USB_ID internal has a 200k pull up resistance which pull up to USB_AVDD_1V8, so OTG is used as Device mode by default;
- USB_VBUS(USB_DET) is used to detect USB insertion. If a high ~~voltage~~ level is detected, it means there is USB inserted;

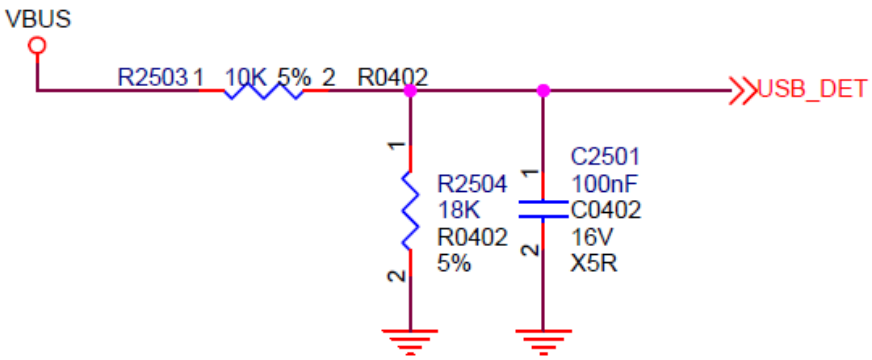


Figure 3-28 RK3358J USB insert detection

- USB controller config reference resistor tolerance should be within 1% because the resistor will affect USB amplitude and the eye diagram.

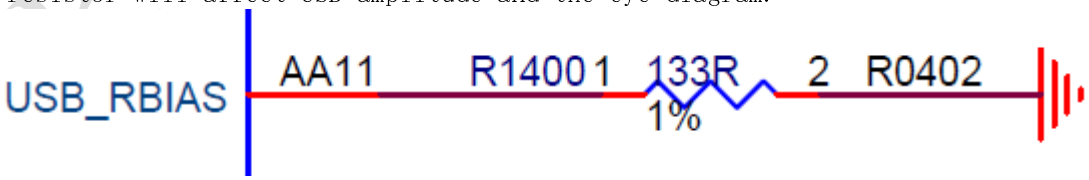


Figure 3-29 RK3358J USB controller reference resistor

- In order to avoid capacitor charge-discharge surging shock to the chip, need to series connect 1ohm resistor with controller 1.0V/1.8V power.

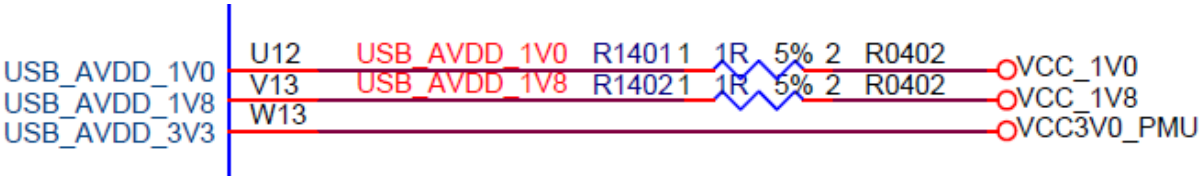


Figure 3-30 RK3358J USB controller power surge protection

- Please put the controller power decoupling capacitor close to the pin to ensure the USB performance.
- Consider to reserve a common mode choke in the signal line in order to restrain electromagnetic radiation. Choose to use the resistor or the common mode choke according to the actual situation during debugging.

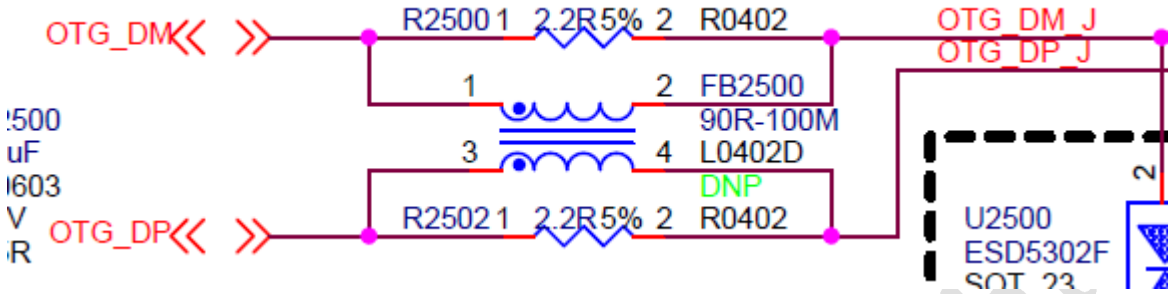


Figure 3-31 RK3358J USB reserved common mode choke

USB 2.0 interface pull up/down and matching design recommendation is shown as table 3-10.

Table 3-10 RK3358J USB2.0 interface design

signal	connection method	description
USB_OTG_DP/DM	direct connection	USB OTG input/output
USB_ID	direct connection(internal with 1.8V pull up)	USB OTG ID recognition, Micro-B interface needs to use
USB_VBUS		USB OTG insert detection
USB_RBIAS		USB PHY config reference resistor, 133ohm groud connection

3.3.3 audio circuit

RK3358J provides 3 set of standard I2S interface. They all support master and slave mode, max sampling rate up to 192kHz and the bit rate from 16bits to 32bits.

- **3.3.3.1 I2S0**

As shown in the picture, I2S0 interface includes independent 8 channels output and 8 channels input. To meet with the asynchronous sampling rate requirement of playback and recording, bit clock and frame clock also provide 2 set (SCLKTX\LRCKTX,SCLKRX\LRCKRX) correspondingly. Need to notice that, in the case when SDOx and SDIx only refer to one set of bit/frame clock, prefer to use SCLKTX\LRCKTX as their common clock.

Need to notice that, the set of I2S interface belongs to VCCIO4 power domain, default set as 1.8V power supply. If I2S peripheral IO voltage is 3.3V, need to adjust the power supply and notice to match the voltage with relative IO in the same power domain.

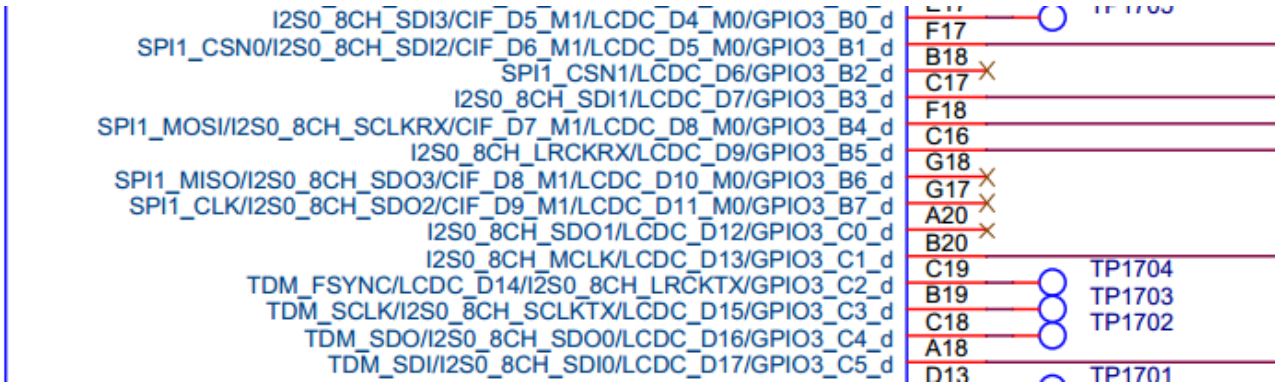


Figure 3-32 RK3358J I2S0 module

I2S0 interface pull up/down and the matching design recommendation is shown as table 3-11.

Table 3-11 RK3358J I2S0 interface design

signal	internal pull up/down	connection method	description(chip side)
I2S0_8CH_MCLK	pull down	series connection 22ohm resistor	I2S0 system clock output
I2S0_8CH_SCLKTX	pull down	series connection 22ohm resistor	I2S0 bit clock(tx, associated with SDOx)
I2S0_8CH_LRCKTX	pull down	series connection 22ohm resistor	I2S0 frame clock, used for audio channel selection(TX, associated with SDOx)
I2S0_8CH_SDO0	pull down	series connection 22ohm resistor	I2S0 data output channel 0
I2S0_8CH_SDO1	pull down	series connection 22ohm resistor	I2S0 data output channel 1
I2S0_8CH_SDO2	pull down	series connection 22ohm resistor	I2S0 data output channel 2
I2S0_8CH_SDO3	pull down	series connection 22ohm resistor	I2S0 data output channel 3
I2S0_8CH_SCLKRX	pull down	series connection 22ohm resistor	I2S0 bit clock(RX, associated with SDIx)
I2S0_8CH_LRCKRX	下拉pull down	series connection 22ohm resistor	I2S0 frame clock, used for audio channel selection(RX, associated with SDIx)
I2S0_8CH_SDI0	下拉pull down	series connection 22ohm resistor	I2S0 data input channel 0
I2S0_8CH_SDI1	下拉pull down	series connection 22ohm resistor	I2S0 data input channel 1

I2S0_8CH_SDI2	pull down	series connection 22ohm resistor	I2S0 data input channel 2
I2S0_8CH_SDI3	pull down	series connection 22ohm resistor	I2S0 data input channel 3

- **3.3.3.2 I2S1**

I2S1 supports 2 channels input and 2 channels output.

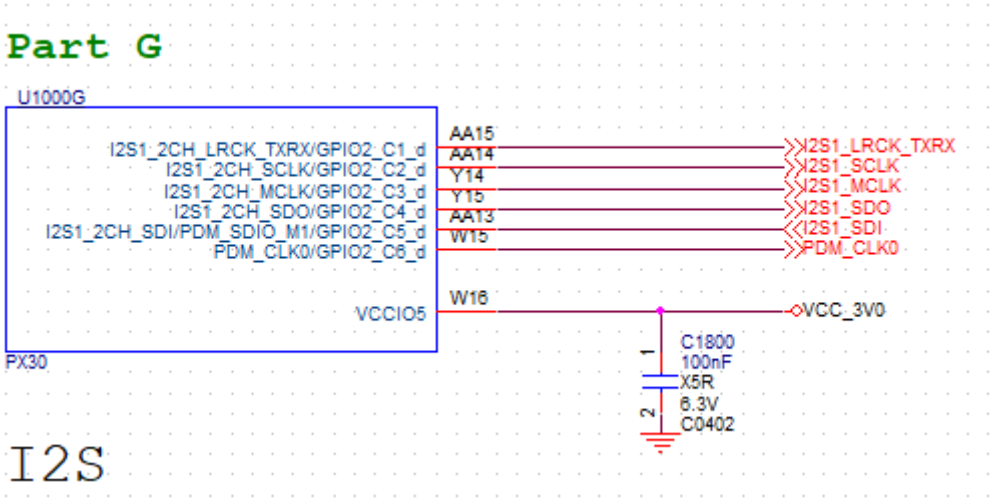


Figure 3-33 RK3358J I2S1 module

I2S1接口上下拉和匹配设计推荐如表3-12所示。I2S1 interface pull up/down and the matching design recommendation is shown as table 3-12.

Table 3-12 RK3358J I2S1 interface design

signal	internal pull up/down	connection method	description(chip side)
I2S1_MCLK	pull down	series connection 22ohm resistor	I2S1 system clock output
I2S1_SCLK	下拉pull down	connection 22ohm resistor	I2S1 bit clock
I2S1_LRCK_TXRX	下拉pull down	connection 22ohm resistor	I2S1 frame clock, used for audio channel to select clock
I2S1_SDO	下拉pull down	connection 22ohm resistor	I2S1 data output channel
I2S1_SDI	下拉pull down	series connection 22ohm resistor	I2S1 data input channel

- **3.3.3.3 I2S2**

I2S2 supports 2 channels output and 2 channels input. The PCM interface used to connect BT module is default as communication port of Bt call with HFP protocol.

Need to notice that, this set of I2S interface belongs to VCCIO4 power domain. When WIFI/BT module is in SDIO3.0 mode, it is set as 1.8V power supply by default. If the power domain is set as 3.3V power supply, PCM IO relative voltage conversion circuit

needs to be soldered to meet with the voltage matching requirement.

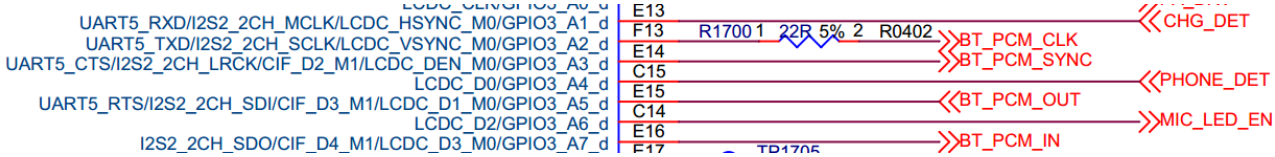


Figure 3-34 RK3358J I2S2 module

I2S2 interface pull up/down and matching design recommendation is shown as table 3-13.

Table 3-13 RK3358J I2S2 interface design

signal	internal pull up/down	connection method	description(chip side)
I2S2_2CH_MCLK	pull down	connection 22ohm resistor	I2S2 system clock output Not reused as PCM, can be used as normal GPIO
I2S2_2CH_SCLK PCM_CLK	pull down	connection 22ohm resistor	I2S2 bit clock PCM clock
I2S2_2CH_LRCK PCM_SYNC	pull down	connection 22ohm resistor	I2S2 frame clock, used for audio channel to select clock PCM data frame sync
I2S2_2CH_SDO PCM_OUT	pull down	connection 22ohm resistor	I2S2 data output channel PCM data output
I2S2_2CH_SDI PCM_IN	pull down	connection 22ohm resistor	I2S2 data input channel PCM data input

RK3358J provides one set of PDM digital audio interface, which supports 8 channels PDM format audio input at most, max sampling rate up to 192kHz and bit rate from 16bits to 32bits.

The IO reuse is relatively flexible in order to cooperate with RK809-1 to implement audio loop back input. Need to avoid the same signal being used repeatedly in different reuse locations.

When use PDM MIC to capture audio, to simplify the firmware processing on the audio recording data, also suggest use PDM interface for loop back. Therefore in the normal cases with 6 PDM MIC audio recording and 2 loop back channels at most, just one whole 8-channel audio recording is enough to complete input, no need for firmware to do the additional splicing processing.

If need to connect 8 channel PDM MIC input, need to use I2S interface as loop back channel capture and firmware needs to do the additional audio splicing processing to meet with the algorithm requirement on the data synchronization.

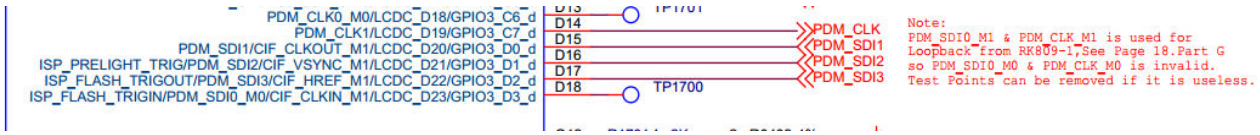


Figure 3-35 RK3358J I2S2 module PDM

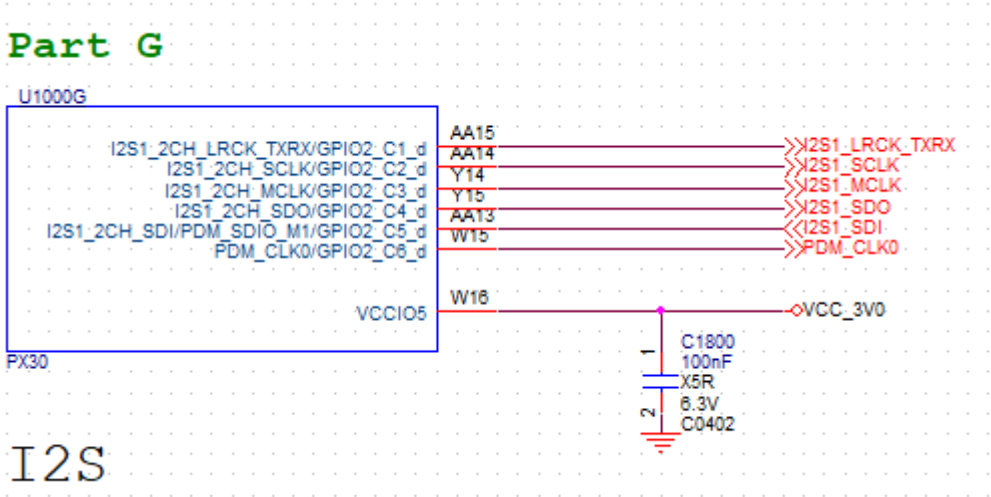


Figure 3-36 RK3358J PDM interface

- **3.3.3.4 Codec**

RK809-1 built in codec, connecting with RK3358J through I2S interface.

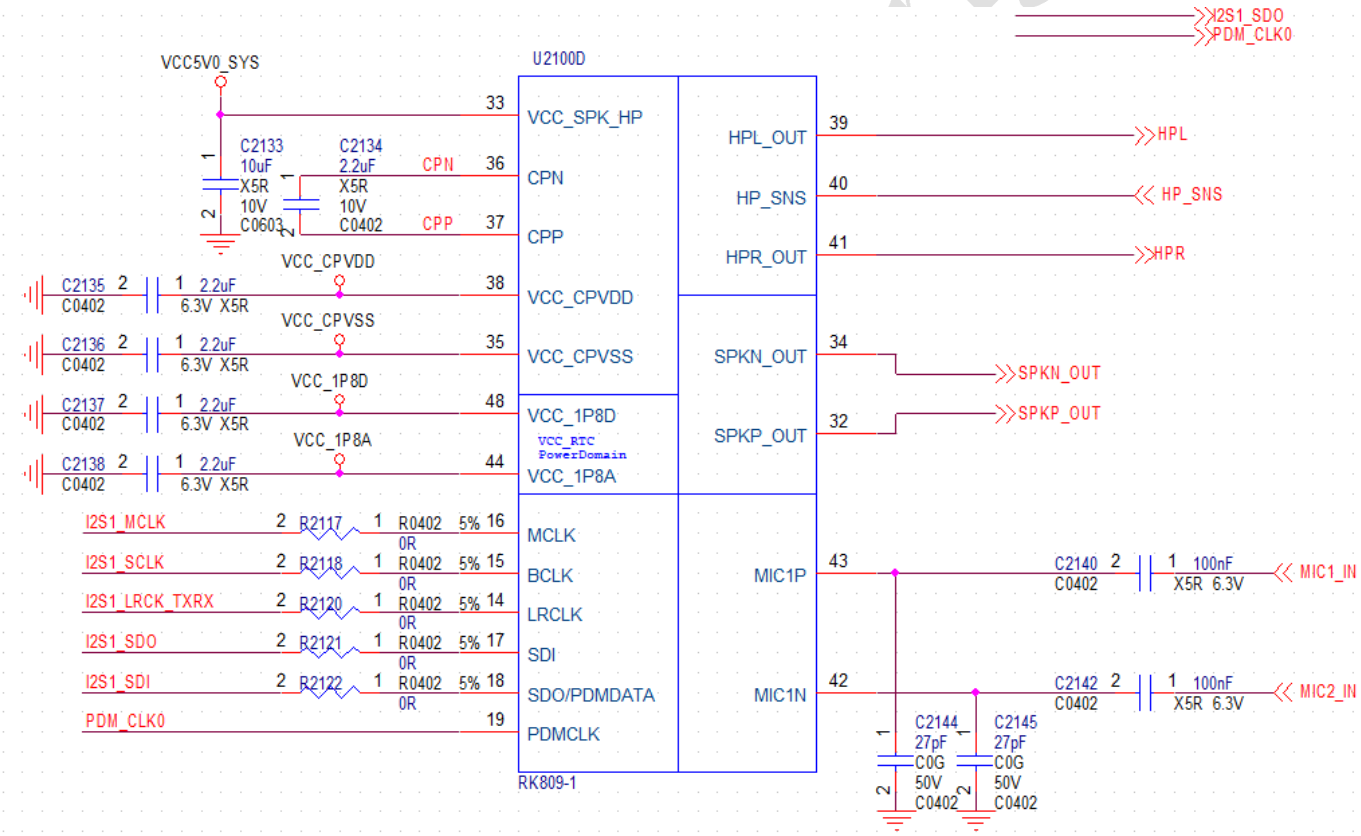


Figure 3-37 RK809-1 codec circuit

Codec outputs HPSNS as internal offset reference and needs to connect with GND on the headphone socket in layout to reduce the voltage difference from headphone GND. If codec GND and headphone GNS are on the same whole GND plane and components layout are close, then can directly connect to GND plane.

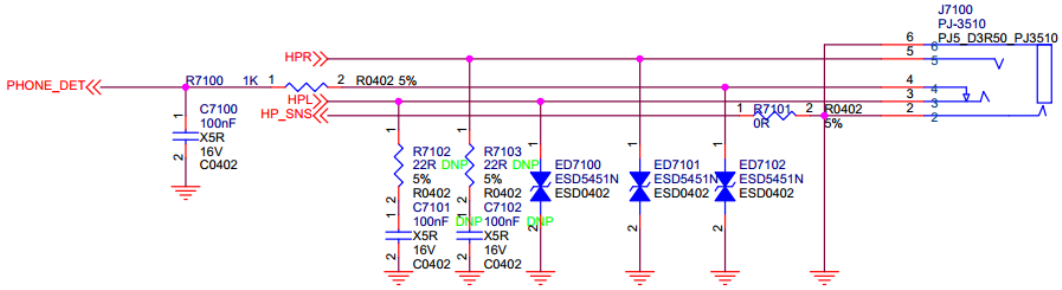


Figure 3-38 RK3358J headphone circuit

Codec builds in a mono filterless speaker driving circuit which can provide 1.3W@8ohm driver strength for low power single audio channel to save the cost. When using the built-in amplifier, suggest loop back circuit as below, output differential loop back signal after voltage dividing and filtering to RK809-1 audio ADC interface and then transfer back to RK3358J through PDM/I2S interface after RK809-1 completes A/D conversion.

Here RK809-1 is default set as PDM interface communicating with RK3358J based on the case of using PDM MIC as described in PDM interface part.

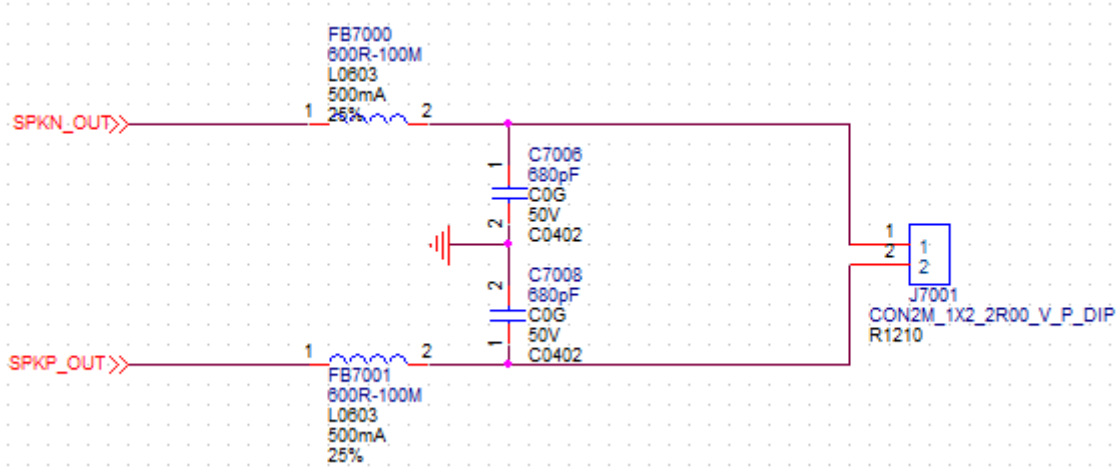


Figure 3-39 RK3358J speaker circuit

- **3.3.3.5 MIC**

MIC circuit is shown as picture 3-40. Please select appropriate divider resistance R7105 and R7106 according to the electret microphone specification.

If using analog interface MEMS MIC, please refer to detailed recommended design circuit.

If using digital interface MEMS MIC, as picture 3-41, directly connect to RK3358J I2S0.

Microphone

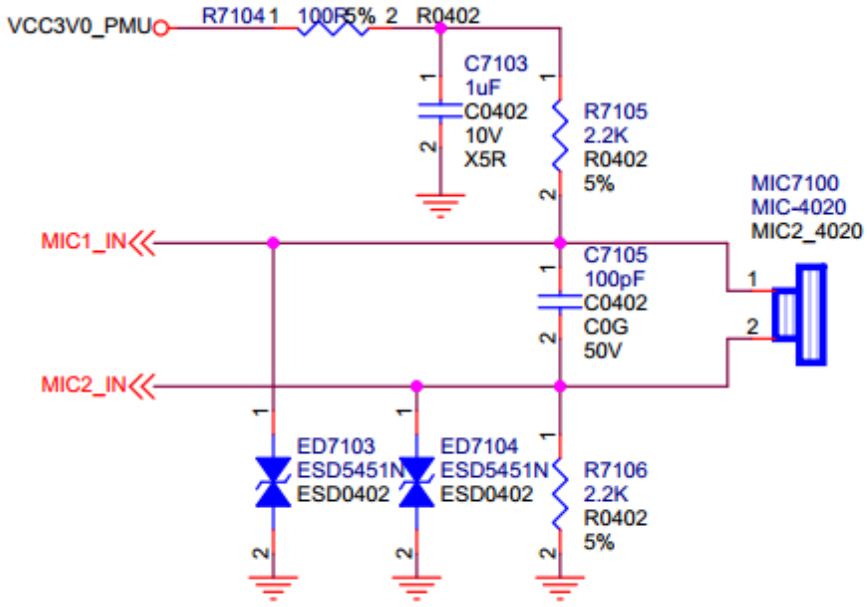


Figure 3-40 RK3358J MIC circuit

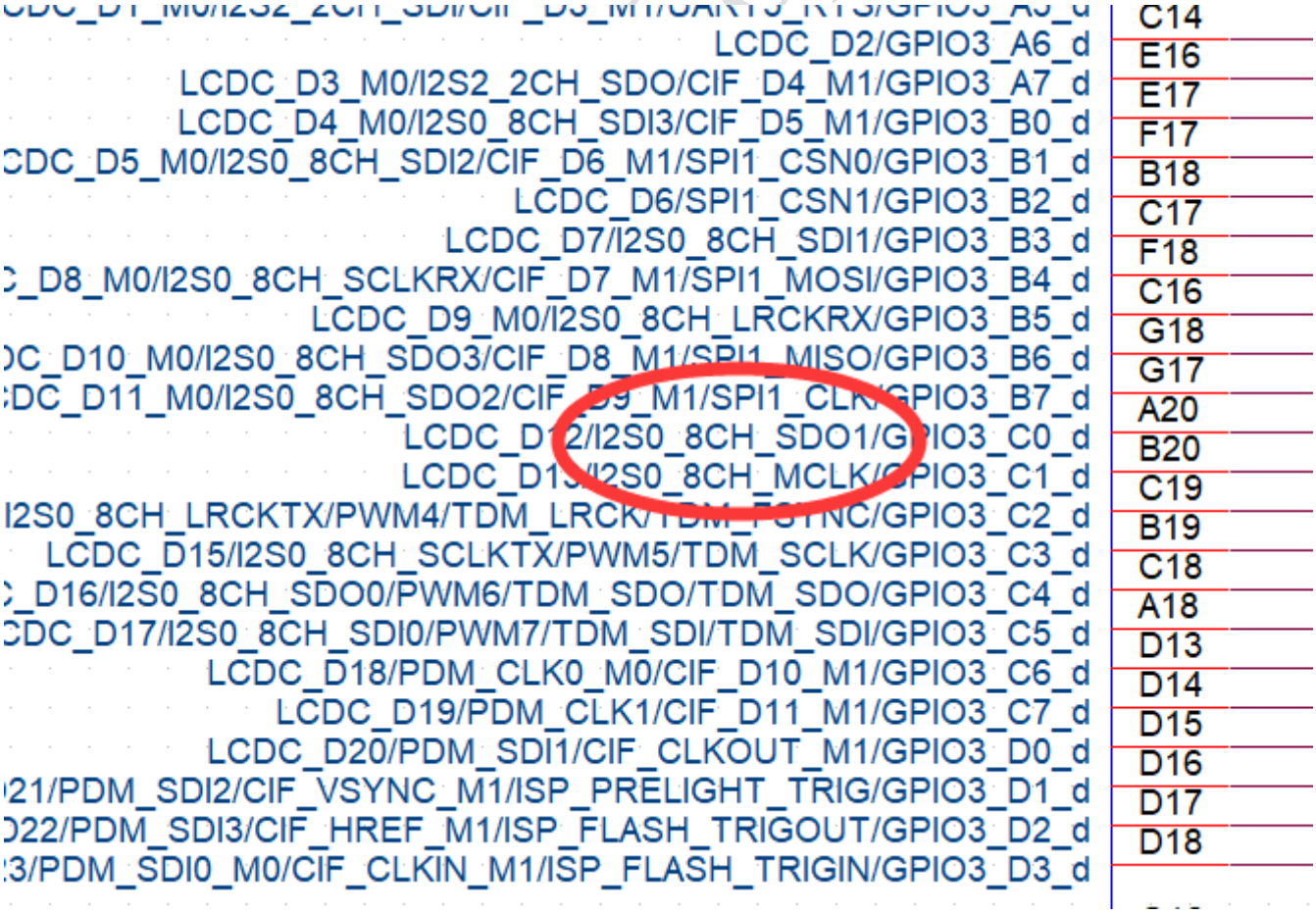


Figure 3-41 RK3358J I2S0

3.3.4 video circuit

RK3358J builds in a video controller which supports RGB/LVDS/MIPI DSI video output modes.

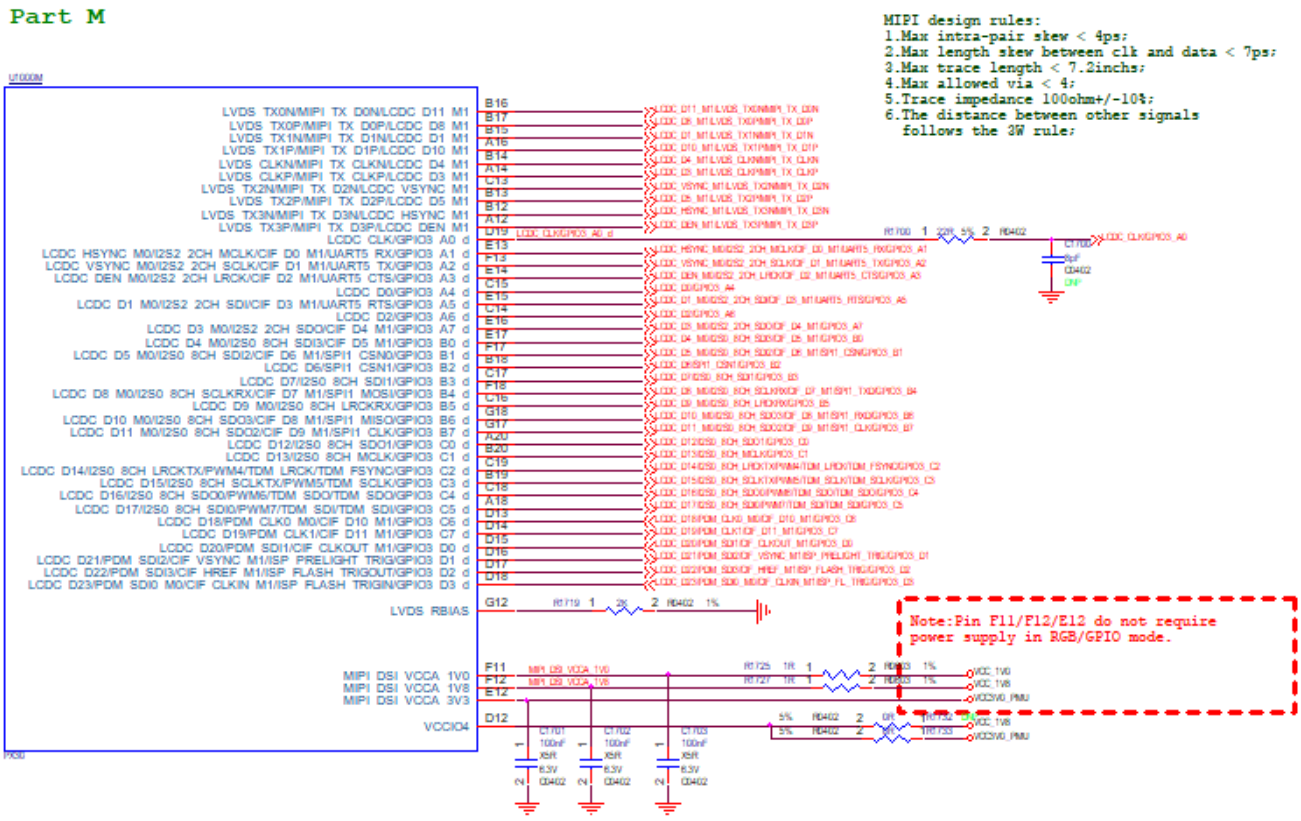


Figure 3-42 RK3358J video output interface

3.3.4.1 LVDS/MIPI mode

LVDS/MIPI uses the same controller which is reused with some of RGB pin. When use LVDS/MIPI output, firmware needs to config the corresponding output mode.

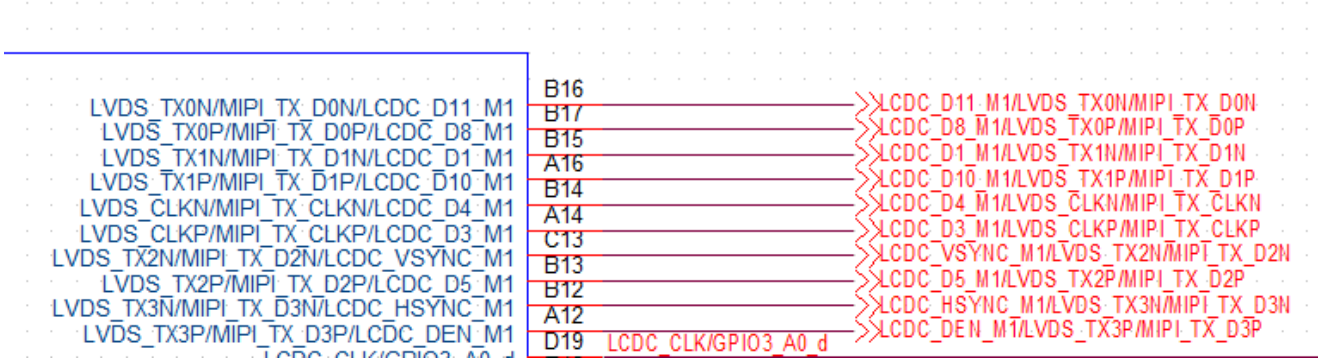


Figure 3-43 RK3358J LVDS/MIPI interface

Notices for design:

- LVDS controller reference resistor R1719 tolerance should be within 1% as the resister will affect the quality of eye diagram signal. The resistor is not needed in MIPI/RGB mode.

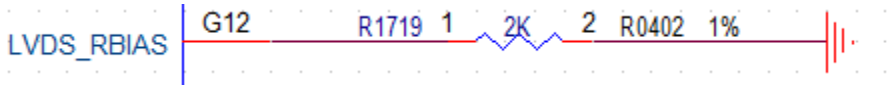


Figure 3-44 RK3358J LVDS controller reference resistor

- In order to avoid capacitor charge-discharge surging shock to the chip, need to

series connect 1ohm resistor with LVDS/MIPI controller 1.0V/1.8V power. No need to supply power for the 3 set of power in RGB mode.

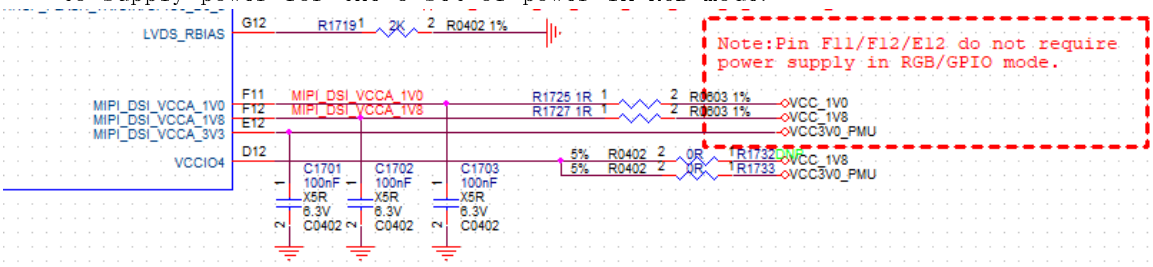


Figure 3-45 RK3358J video output interface

- Put the controller power decoupling capacitor close to the pin to ensure the working stability.

3.3.4.2 RGB mode

RK3358J supports 24 bit RGB output. When using RGB output, firmware needs to config the corresponding output mode.

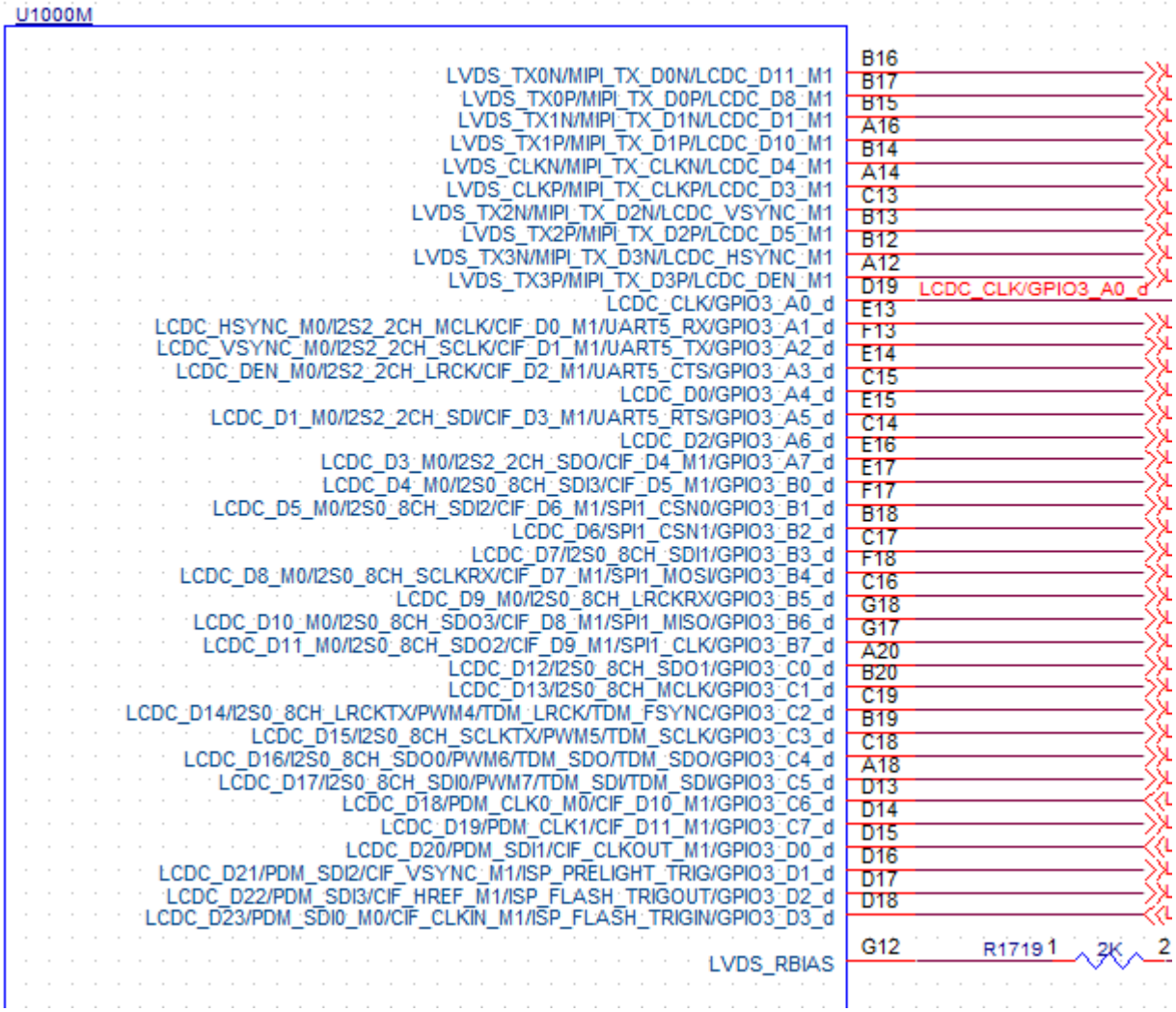


Figure 3-46 RK3358J MIPI DSI0 module

- When using RGB888 24 bit panel, the signal corresponding relationship is as below:

Correspondence between LCDC DATA and RGB			
LCDC_D0	B0	LCDC_D12	G4
LCDC_D1	B1	LCDC_D13	G5
LCDC_D2	B2	LCDC_D14	G6
LCDC_D3	B3	LCDC_D15	G7
LCDC_D4	B4	LCDC_D16	R0
LCDC_D5	B5	LCDC_D17	R1
LCDC_D6	B6	LCDC_D18	R2
LCDC_D7	B7	LCDC_D19	R3
LCDC_D8	G0	LCDC_D20	R4
LCDC_D9	G1	LCDC_D21	R5
LCDC_D10	G2	LCDC_D22	R6
LCDC_D11	G3	LCDC_D23	R7

Figure 3-47 RK3358J 24 bit connection method

- When using RGB666 18 bit panel, only needs to connect LCDC_D0-D17 data signal. The corresponding relationship is as below:

Correspondence between LCDC DATA and RGB			
LCDC_D0	B2	LCDC_D9	G5
LCDC_D1	B3	LCDC_D10	G6
LCDC_D2	B4	LCDC_D11	G7
LCDC_D3	B5	LCDC_D12	R2
LCDC_D4	B6	LCDC_D13	R3
LCDC_D5	B7	LCDC_D14	R4
LCDC_D6	G2	LCDC_D15	R5
LCDC_D7	G3	LCDC_D16	R6
LCDC_D8	G4	LCDC_D17	R7

Figure 3-48 RK3358J 18 bit connection method

- RGB signals including LCDC_D5/D8/D10 etc. have two reuse relationships M0 and M1 which can be configured flexibly. But for the actual product design, suggest use M1 pin. Because the pin is on the edge of the chip, it is convenient to layout no matter for double layers board or four layers board.

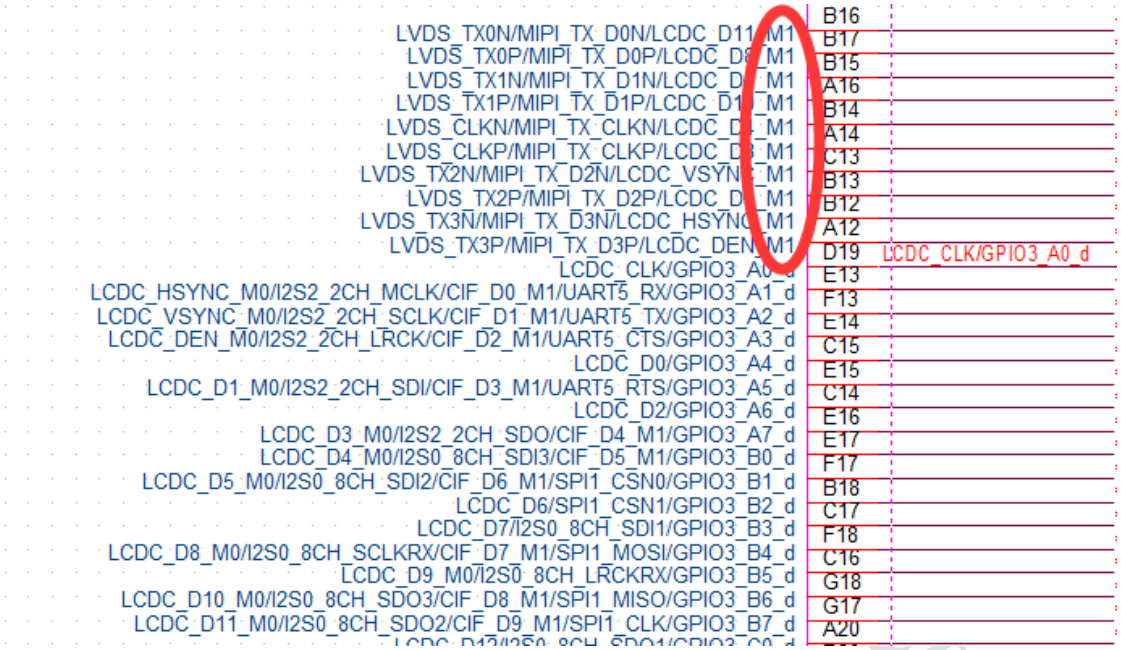


Figure 3-49 RK3358J LCDC M0&M1 reuse pin

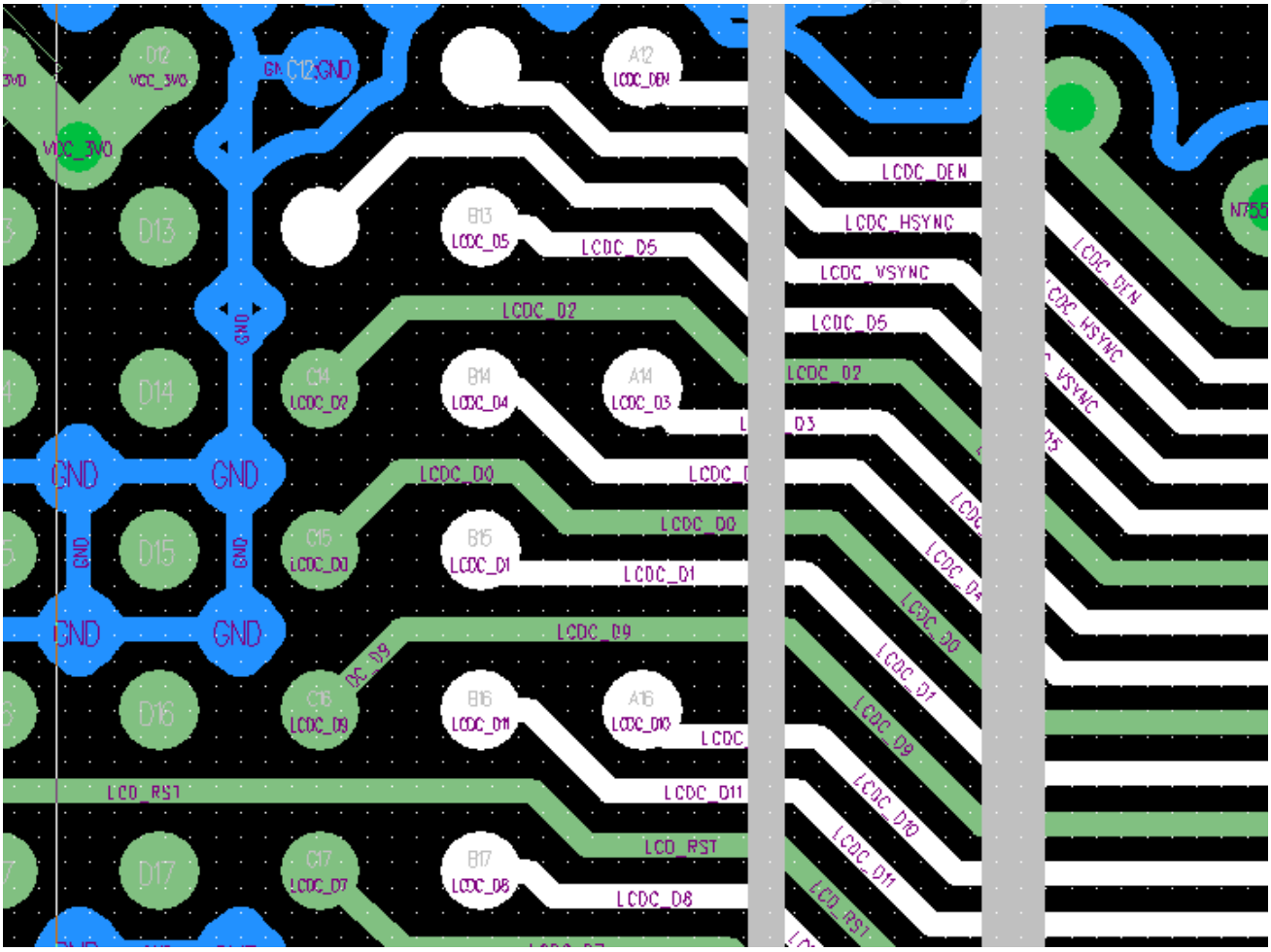


Figure 3-50 RK3358J LCDC M1 pin fan out

3.3.5 camera circuit

- **3.3.5.1 USB CAMERA**

  Please refer to chapter 3.3.2 USB design method for USB CAMERA.

- **3.3.5.2 MIPI CSI**

  RK3358J has one MIPI-CSI input interface with built-in ISP processor.

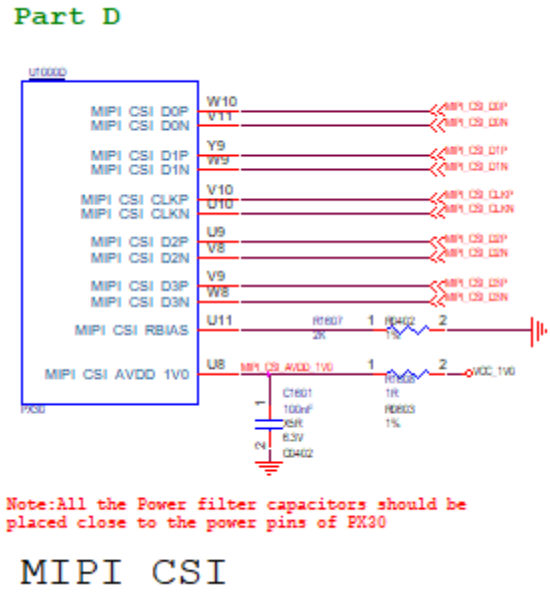


Figure 3-51 MIPI-CSI module

Notices for design:

- The controller reference resistor R1600 tolerance should be within 1% as the resistance will affect the quality of eye diagram signal.

Figure 3-52 RK3358J MIPI-CSI controller reference resistor

- In order to avoid capacitor charge-discharge surging shock to the chip, need to series connect 1ohm resistor with MIPI-CSI controller's power.

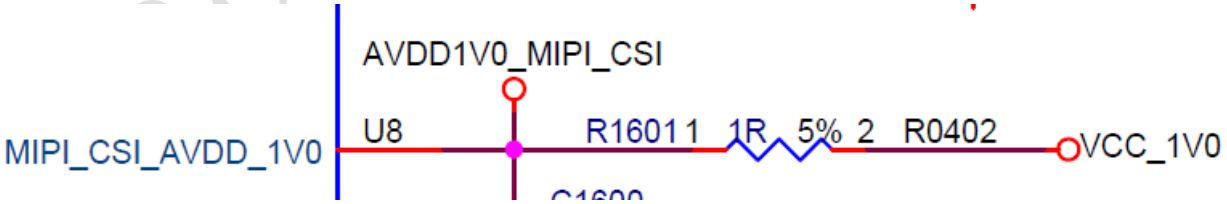


Figure 3-53 RK3358J video output interface

- Please put the controller power decoupling capacitor close to the pin to ensure the MIPI-CSI performance.

- **3.3.5.3 CIF CAMERA**

The CIF interface power domain is VCCIO3 power supply. In the actual product design, need to select the corresponding power supply according to the product camera actual IO power supply requirement (1.8V or 2.8V) and keep I2C pull up voltage level same as it, otherwise it will make camera working abnormally or can not work.

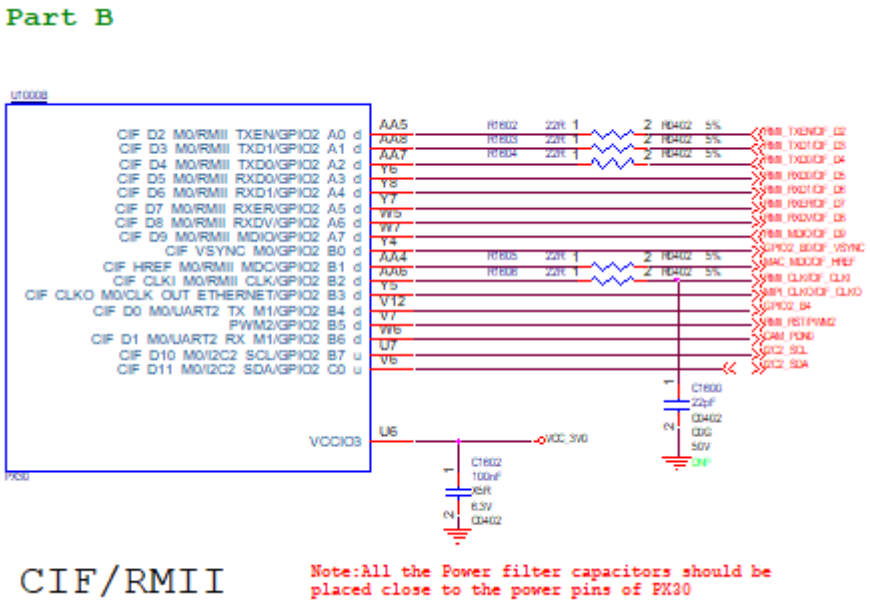


Figure 3-54 RK3358J CIF module

3.3.6 RMII circuit

RMII reuses with CIF, can config 100M Ethernet PHY and implement 100M internet function. For 100M Ethernet design please refer to the design document from PHY vendor. PHY working clock can be provided by an external crystal or the MAC_CLK pin.

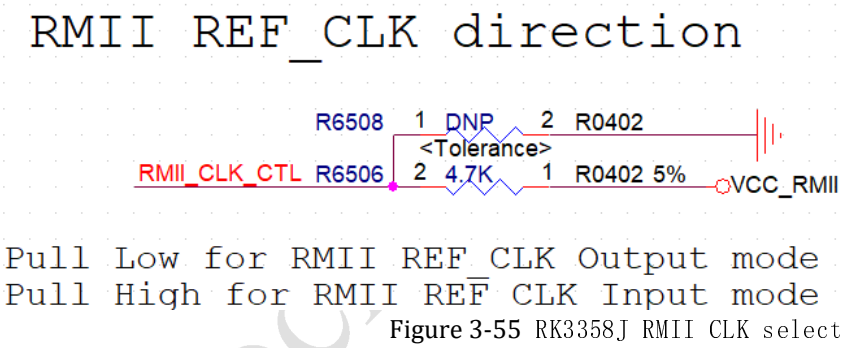


Figure 3-55 RK3358J RMII CLK selection

3.3.7 ADC circuit

RK3358J uses SARADC ADC_IN2 as keyboad input port and reuses it as RECOVERY mode (no need to upgrade LOADER), as shown in the follow picture. When system already flashes image, pull down ADKEY_IN to make ADC_IN2 keep 0V during system bootup, and then RK3358J enters Rockusb flashing mode. When PC recognizes USB device, release the button to recover ADC_IN2 back to high voltage (1.8V), and then can start image flashing.

RK3358J SARADC sampling range is 0-1.8V and the sampling precision is 10 bits. Button array type is parallel and the input key value can be adjusted by increasing/decreasing button and adjusting divider resistance ratio to accomplish multikey input to meet with the customer product requirements. Suggest any two buttom key values must be bigger than +/-35, that means the central voltage difference must be bigger than 123mV.

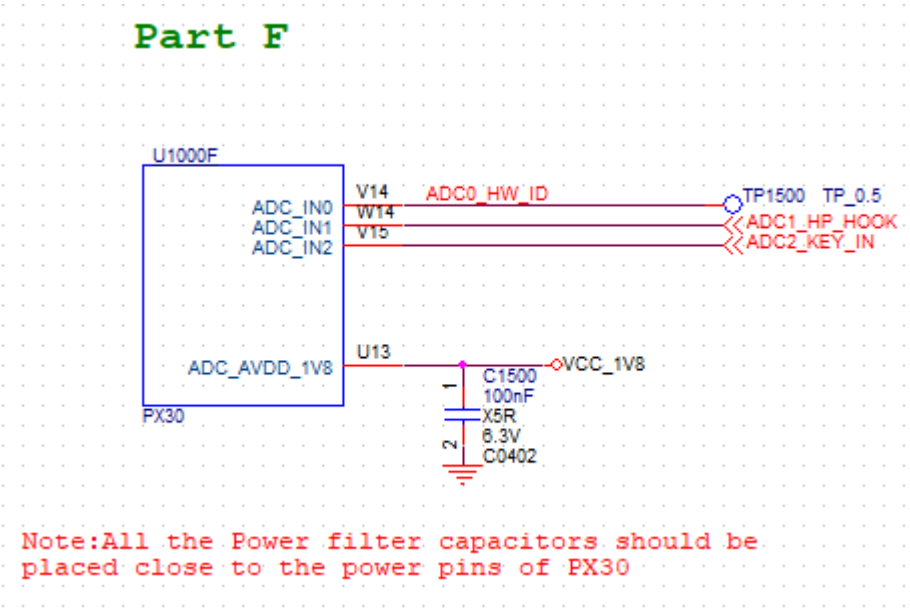


Figure 3-56 RK3358J SAR-ADC module

3.3.8 SDIO/UART circuit

RK3358J supports WIFI/BT module with SDIO 3.0 interface as shown in the picture 3-56. When using WIFI/BT modules with SDIO and UART interfaces, please note that RK3358J SDIO and UART controller power supply must keep same as the IO voltage level of the module.

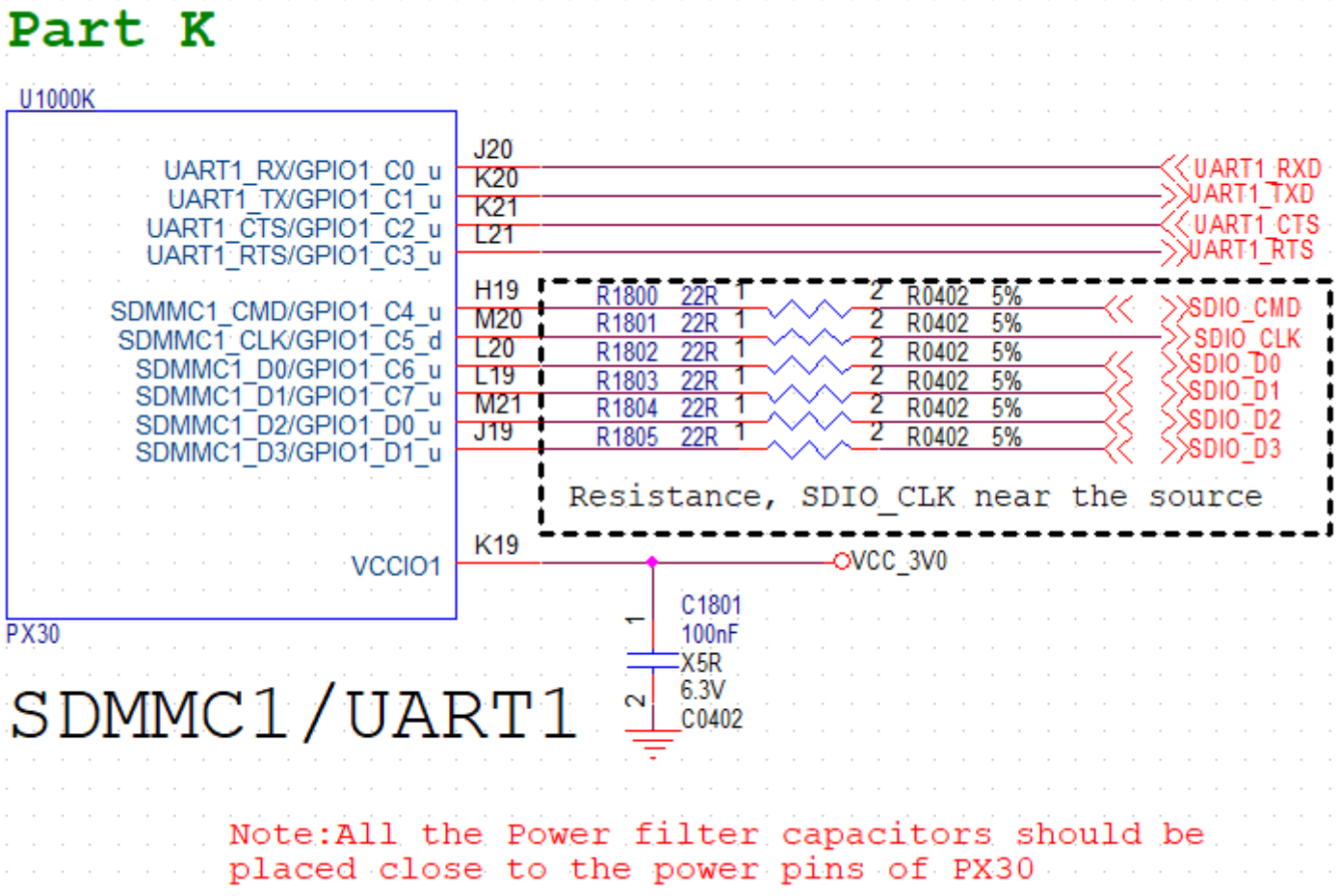


Figure 3-57 RK3358J SDIO/UART module

3.3.8.1 SDIO

The SDIO interface pull up/down and the matching design recommendation is shown as table 3-14.

Table 3-14 RK3358J SDIO interface design

signal	internal pull up/down	connection method	description(chip side)
SDIO_DQn[0:3]	pull up	connection 22ohm resistordelete if the line is short	SDIO data sending/receiving
SDIO_CLK	pull down	series connection 22ohm resistor	SDIO clock sending
SDIO_CMD	pull down	connection 22ohm resistordelete if the line is short	SDIO command sending/receiving

3.3.8.2 UART

The UART interface pull up/down and the matching design recommendation is shown as table 3-15.

Table 3-15 RK3358J UART interface design

signal	internal pull up/down	connection method	description(chip side)
UART1_RX	pull up	direct connection	UART1 data input
UART1_TX	pull up	direct connection	UART1 data output
UART1_CTSn	pull up	direct connection	UART1 permission sending signal
UART1_RTSn	pull up	direct connection	UART request sending signal

U UART Debug circuit

RK3358J debug UART2 is reused with SDMMC interface. You can connect external conversion board to convert UART to USB for debugging.

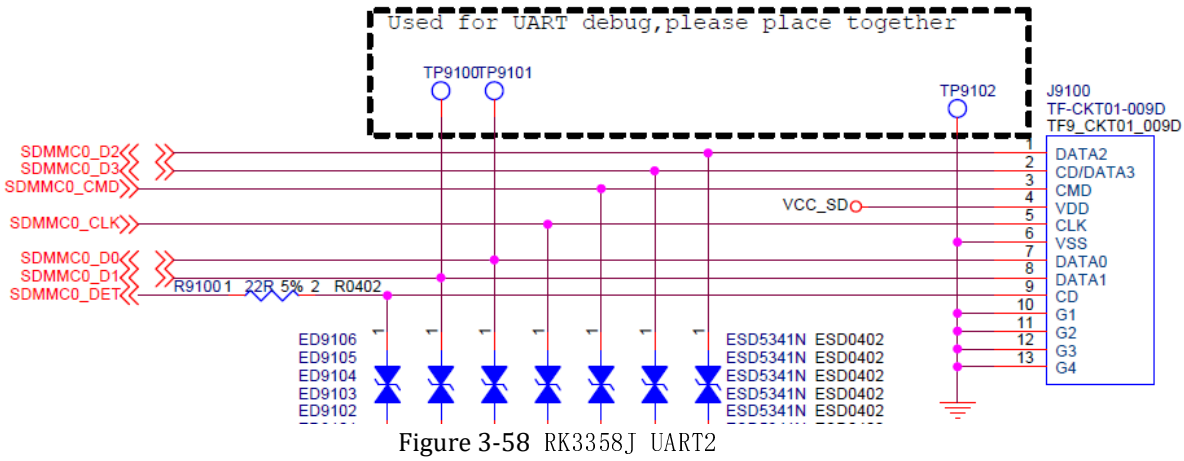


Figure 3-58 RK3358J UART2

Please select the PC port which connected with the development board, select 1.5M for baud rate and no need to select flow control RTS/CTS.

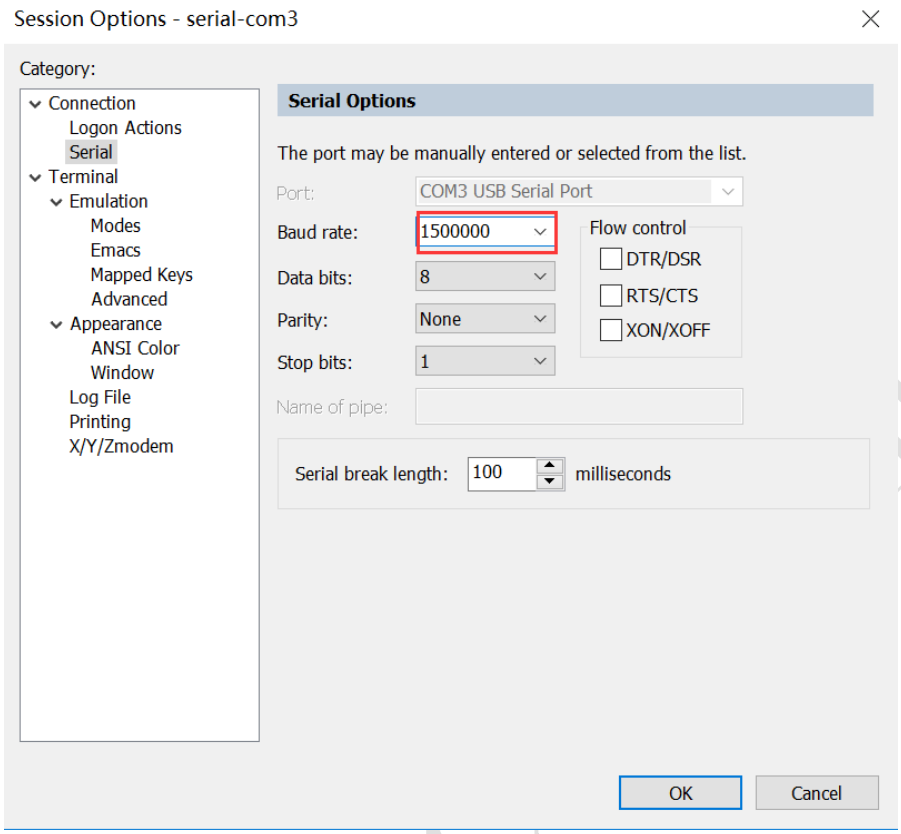


Figure 3-59 RK3358J serial port config

4 Thermal design suggestion

4.1 thermal simulation result

Aiming at RK3358J TFBGA395L package, based on JEDEC standard PCB, use finite element modeling to get the thermal resistance simulation report. This report is achieved based on JEDEC JESD51-2 standard, but the system design and environment may be different from JEDEC JESD51-2 standard, need to analyze according to the application condition.

note

Thermal resistance is the reference value when there is no heat sink on PCB. The detailed temperature is related with the single board's design, size, thickness, material and other physical factors.

4.1.1 result overview

The thermal resistance simulation result is as below:

Table 4-1 RK3358J thermal resistance simulation result

Package (EHS-FCBGA)	θ_{JA}(℃/W)	θ_{JB}(℃/W)	θ_{JC}(℃/W)
PCB	26.9	NA	8.2

4.1.2 PCB description

The PCB structure of the thermal resistance simulation is shown as below table:

Table 4-2 RK3358J PCB structure of thermal resistance simulation

PCB	PCB Dimension (L x W)	114.3 x 101.5mm
	PCB Thickness	1.6mm
	Number of Cu Layer	4-layers

4.1.3 term interpretation

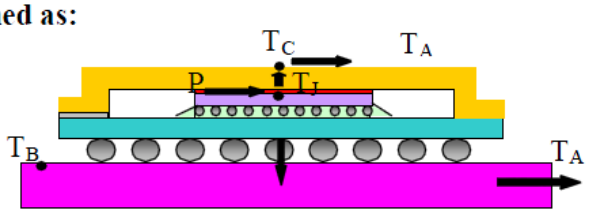
The terms of this chapter are as below:

- T_J: The maximum junction temperature;
- T_A: The ambient or environment temperature;
- T_C: The maximum compound surface temperature;
- T_B: The maximum surface temperature of PCB bottom;
- P: Total input power

The thermal parameter can be define as following

1. *Junction to ambient thermal resistance,* θ_{JA}**, defined as:**

$$\theta_{JA} = \frac{T_J - T_A}{P} \quad ; \qquad (1)$$



Thermal Dissipation of EHS-FCBGA

Figure 4-1 θJA definition

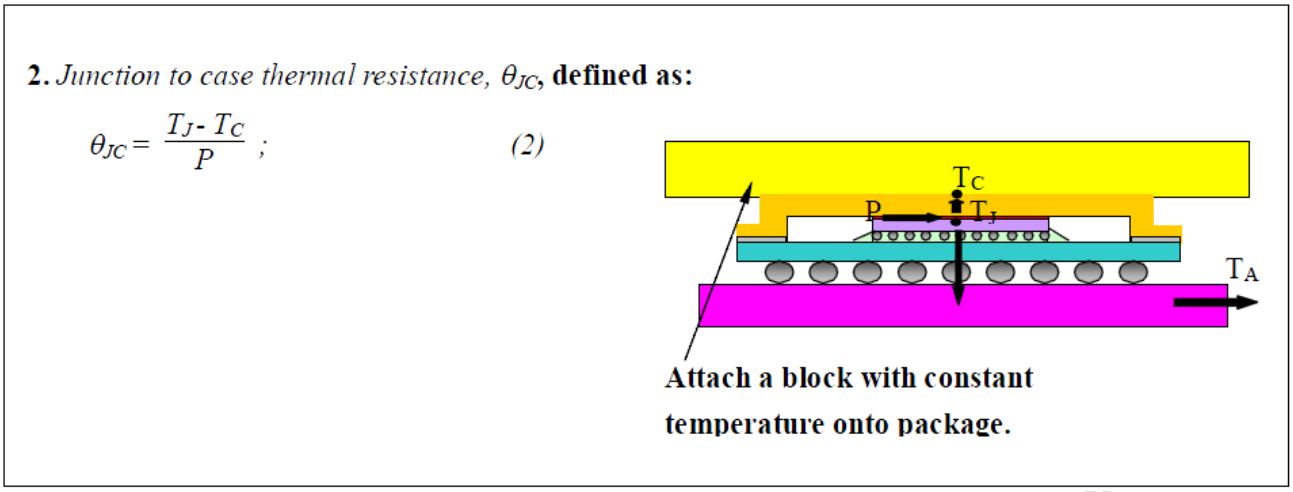


Figure 4-2 θJC definition

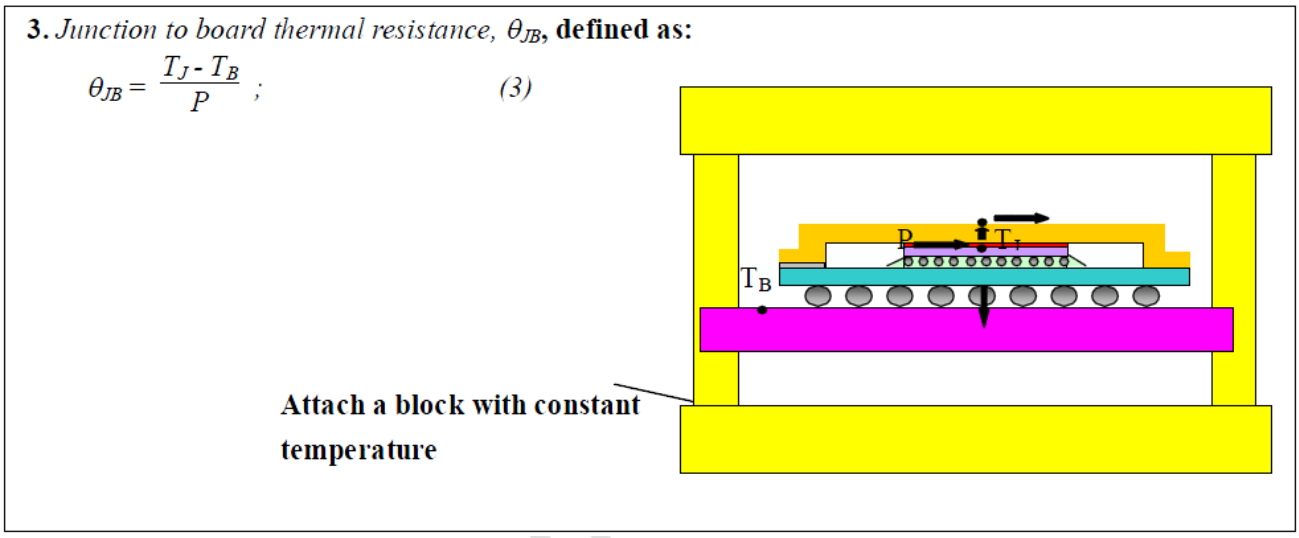


Figure 4-3 θJB definition

4.2 thermal control method inside the chip

4.2.1 thermal control strategy

linux Generic Thermal System Drivers, In linux kernel, it defines one set of thermal control frame linux Generic Thermal System Drivers. It can control the system temperature through different strategies. Currently below 3 strategies are commonly used:

- Power_allocator: Introduce PID (percentage-integral-differential) control to dynamically allocate power for modules according to current temperature, and convert power to frequency, so as to achieve the effect of limiting the frequency according to temperature.
- Step_wise : Limit the frequency step by step according to current temperature.
- Userspace: Do not limit frequency.

RK3358J uses T-sensor inside the chip to detect the internal temperature. Use Power_allocator strategy by default and there are several working status as below:

- when the temperature is over the set value:
  - temperature tendency goes up, start to decrease frequency
  - temperature tendency goes down, start to increase frequency
- when the temperature decreases to the set value:
  - temperature tendency goes up, keep the frequency unchanged;
  - temperature tendency goes down, start to increase frequency;
- When the frequency increases to the max, but the temperature is still under the set

value, CPU frequency is not controlled by thermal and will be adjusted by system loading.

- If the temperature is still too high after decreasing frequency (such as poor heat dissipation), firmware will trigger restart when over 95 degrees. If fail to restart due to deadlock or other reasons, when the chip temperature over 100 degrees, it will trigger otp_out inside the chip for PMIC to power off directly. Please refer to chapter 3.2.5.1 for detailed operations.

Note

Temperature tendency is achieved by comparing the two values captured adjacently. When the device temperature is not over the threshold value, capture the temperature every 1 second; when the device temperature is over the threshold value, capture the temperature every 20 ms and limit the frequency.

4.2.2 temperature control config

RK3358J SDK provides separate thermal control strategies for CPU and GPU. Please refer to 《Rockchip thermal development guide》 for detailed config.

5 ESD/EMI protection design

5.1 overview

This chapter provides ESD/EMI protection design suggestion for RK3358J product design to help customers to improve the anti-static and anti-electromagnetic interference ability of the product.

5.2 term interpretation

the terms of this chapter are explained as below:

- Electro-Static discharge (ESD):
- Electromagnetic Interference (EMI): electromagnetic interference, including conduction interference and radiation interference.

5.3 ESD protection

- ensure reasonable mold design; reserve anti ESD component for port and connectors.
- protect and isolate the sensitive components in PCB layout.
- Try best to put RK3358J and core components in the center of PCB layout. If not able to put them in the center, need to ensure that the shielding cover has 2mm at least distance from the board edge and is connected to GND safely.
- PCB layout should consider function module and signal flow direction, sensitive components should be mutually independent, and it is better to isolate the areas that are easy to interference.
- Place ESD components reasonably. Generally place at the source, that is, place ESD components in the junction or electrostatic discharge.
- Components layout should be away from the board edge and hav some distance from the connectors.
- PCB surface must have good GND loop and all connectors need to have good GND connection loop on the surface layer. Shielding cover should try best to connect with the surface layer GND and make as many ground holes as possible in the soldering place to connect with GND. In order to achieve this, it is required that the connecting parts should not go through the surface, and there should not be a wide range of cutting off the copper surface in layout.
- Do not go through the surface layer edge and make as many ground holes as possible.
- Isolate signal from ground if necessary.
- Expose copper as much as possible to enhance the electrostatic discharging effect or make it convenient to add remedial measures such as foam.

5.4 EMI protection

- The electromagnetic interference has three factors: interference source, coupling channel and sensitive devices. We cannot deal with sensitive devices, so need to handle EMI from interference source and coupling channel. The best way to resolve EMI issues is to eliminate the interference source. If cannot eliminate, try to cut off coupling channel or avoid antenna effect.
- It is difficult to eliminate the interference source on PCB. We can take actions such as filtering, grouding, balancing, resistance controlling, improving signal quality (e.g. termination connection) etc. Generally several methods will be applied together, but the basic requirement is good grouding.
- The commonly used EMI material include shielding cover, special filter, resistor, capacitor, inductor, magnetic bead, common mode choke/magnetic ring, wave-absorbing material, spread spectrum component etc.

- The principle to select filter: if the loading (receiver) is high resistance (normal single port signal interface is high resistance, such as SDIO, RBG, CIF etc.), select capacitive filter component and parallel connect to the circuit; if the loading (receiver) is low resistance (such as power output interface), select inductive filter component and series connect to the circuit. If using filter component, should ensure the signal quality within its SI permission range. Differential interface usually uses common mode choke to suppress EMI.
- The shielding measures on PCB should have good grounding, otherwise it will cause radiation leakage or form antenna effect. The shielding of connectors should conform with the relative technical standard.
- RK3358J spread spectrum function is used per modules. The degree of the spread spectrum is defined according to the signal requirement of the relative parts. Detailed measures refer to RK3358J spread spectrum description.
- EMI has the same high requirement as ESD on layout. The ESD Layout requirements described above are mostly suitable for EMI protection. Besides, add below requirement.
  - Try best to ensure the signal integrality.
  - Differential line should have equal length and be tight coupling to ensure the symmetry of the differential signal, in order to reduce the differential signal malposition and clock, to avoid converting to the common mode signal which will cause EMI issues.
  - Components with metal shell such as plug-in electrolytic capacitors should avoid coupling interference signals to radiate. Also need to avoid component interference signals coupling from the shell to other signal lines.