RK3326 Hardware Design Guide

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Preface

Overview

This document mainly describes the key points of hardware design and notices for RK3326 processor, aiming to help RK customers shorten the product design cycle, improving the product design stability and reducing the failure rate. Please refer to the requirements of this guide to do the hardware design, and suggest to use the relevant core templates released by Rockchip. If need to modify due to specific reasons, please strictly follow the design rule of high-speed-digital-circuit and RK Schematic&PCB checklist requirements.

Chip Type

The corresponding chip type is RK3326 in this document.

Applicable Object

This document is mainly suitable for below:

- Product hardware development engineers
- Field application engineers
- Test engineers

Revision History

The revision history accumulates instructions for each update of the document and the latest version contains updates of all previous versions.

Version	Author	Revision Date	Revision Description	Remark
V1.0	Linus.Lin	2018.08.06	The initial version release	
V1.1	Linus.Lin	2018.11.29	2.3.6 Modify to use "ADC_IN2 of SARADC as the sampling port" instead of "ADC_IN1 of SARADC as the sampling port". Table 2-3 modify FLASH_VOLSEL description in initialization configuration.	
V1.2	Linus.Lin	2019.06.18	2.2.2.3 Modify CPU voltage drop range to 60mV 2.2.2.3 Modify GPU/LOGIC voltage drop range to 60mV	

Acronym

Acronym includes the abbreviations of commonly used phrases in this document:

DDR	Double Data Rate	双倍速率同步动态随机存储器
eMMC	Embedded Multi Media Card	内嵌式多媒体存储卡
GPU	Graphics Processing Unit	图形处理器
HDMI	High Definition Multimedia Interface	高清晰度多媒体接口
I^2C	Inter-Integrated Circuit	内部整合电路(两线式串行通讯总线)
JTAG	Joint Test Action Group	联合测试行为组织定义的一种国际标准测试协议（IEEE 1149.1兼容）
LDO	Low Drop Out Linear Regulator	低压差线性稳压器
LVDS	Low-Voltage Differential Signaling	低电压差分信号
MIPI	Mobile Industry Processor Interface	移动产业处理器接口
PMIC	Power Management IC	电源管理芯片
PMU	Power Management Unit	电源管理单元
Rockchip	Rockchip Electronics Co.,Ltd.	瑞芯微电子股份有限公司
SD Card	Secure Digital Memory Card	安全数码卡
SDIO	Secure Digital Input and Output Card	安全数字输入输出卡
SDMMC	Secure Digital Multi Media Card	安全数字多媒体存储卡
SPI	Serial Peripheral Interface	串行外设接口
TF Card	Micro SD Card(Trans-flash Card)	外置记忆卡
USB	Universal Serial Bus	通用串行总线

Table of Contents

Contents of Figure

Contents of Table

1 Introduction

1.1 Overview

RK3326 is a high-performance Quad-core application processor designed for personal tablet and smart audio device.

Many embedded powerful hardware engines are provided to optimize performance for high-end application. RK3326 supports almost full-format H.264 decoder by 1080p@60fps, H.265 decoder by 1080p@60fps, also support H.264 encoder by 1080p@30fps, high-quality JPEG encoder/decoder.

Embedded ARM G31-2EE GPU makes RK3326 completely compatible with OpenGL ES 1.1/2.0/3.2, DirectX 11 FL9_3, OpenCL 2.0 and Vulkan 1.0. Special 2D hardware engine will maximize display performance and provide very smoothly operation.

RK3326 has high-performance external memory interface (DDR3/DDR3L/DDR4 /LPDDR2/LPDDR3) capable of sustaining demanding memory bandwidths.

1.2 Block Diagram

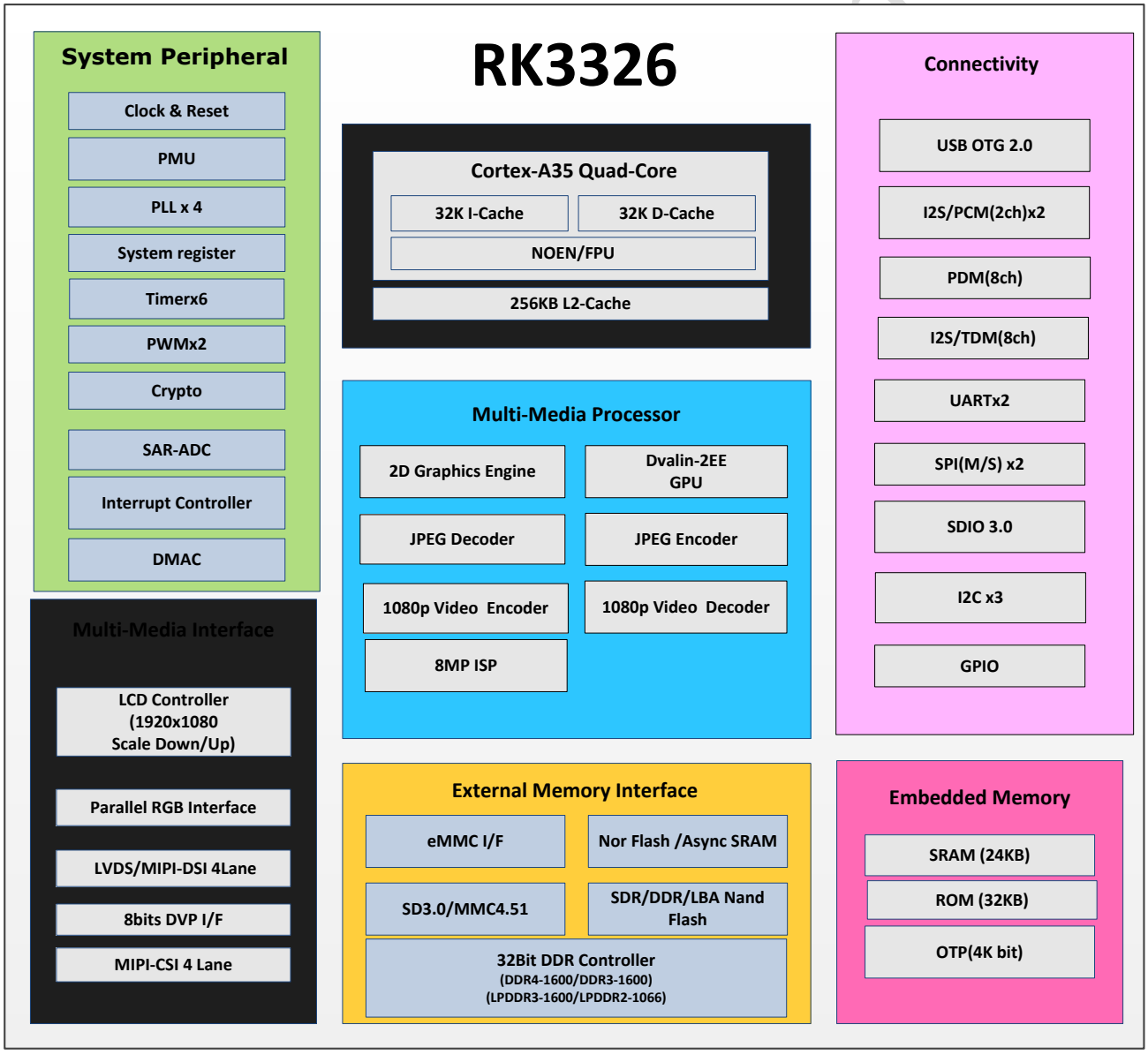


Figure 1-1 RK3326 Block Diagram

1.3 Application Block Diagram

1.3.1 RK817-1 Application

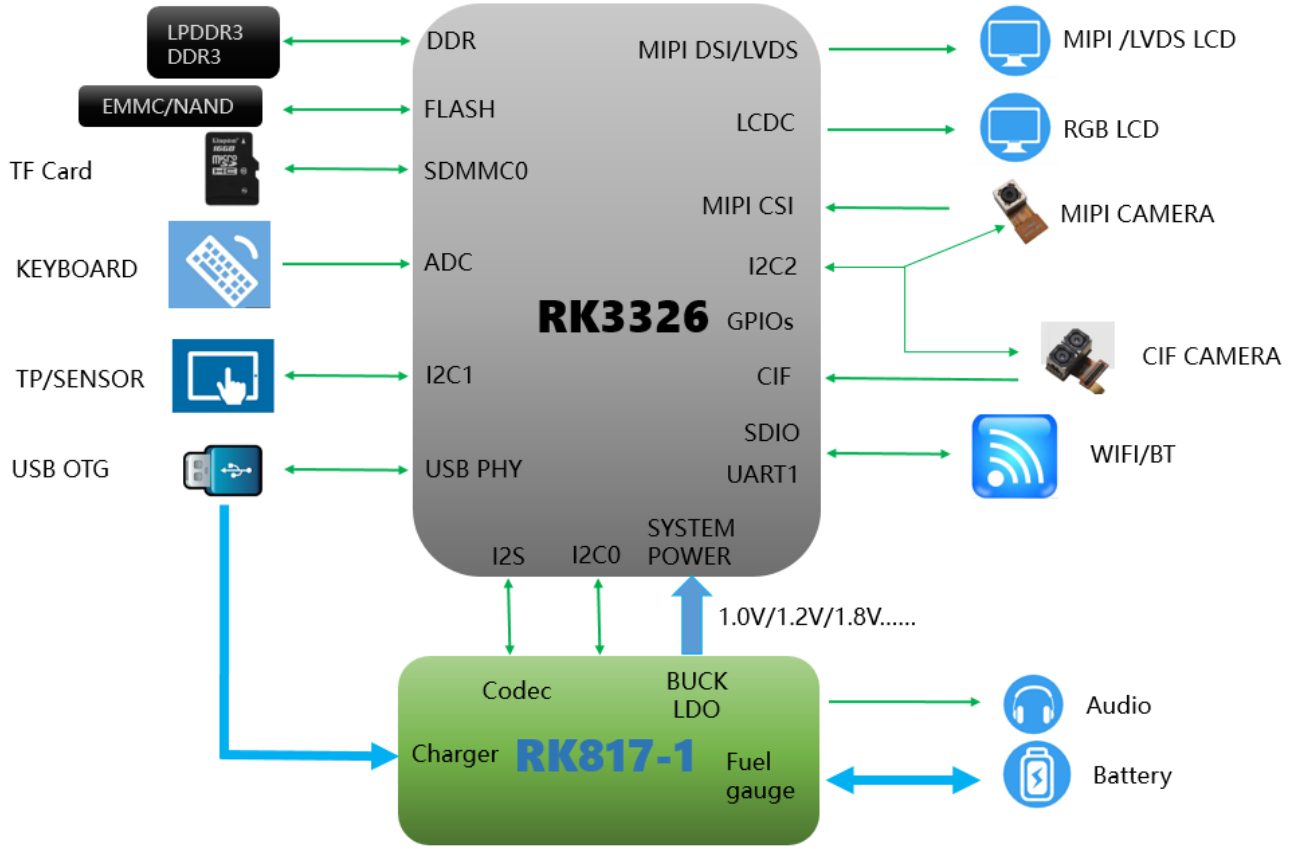


Figure 1-2 RK3326 RK817-1 Application

1.3.2 RK809-1 Application

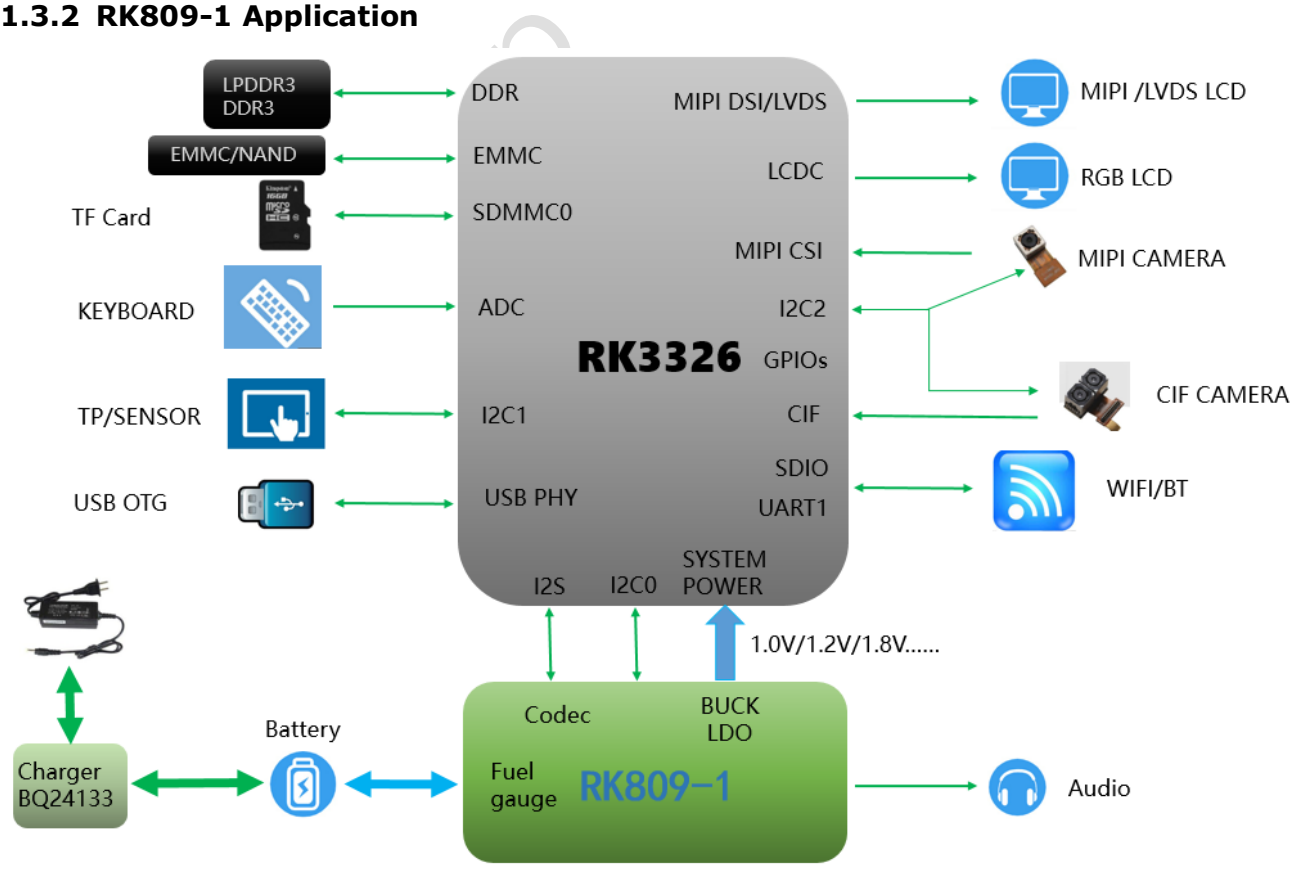


Figure 1-3 RK3326 RK809-1 Application

Above shows the application block diagrams of RK3326 chip solution. For more details please refer to the reference design schematic released by Rockchip.

2 Schematic Design Recommendation

2.1 Minimum System Design

2.1.1 Clock Circuit

RK3326 internal oscillator circuit and external 24MHz crystal constitute the internal oscillator clock source, as Figure 2-1 shows:

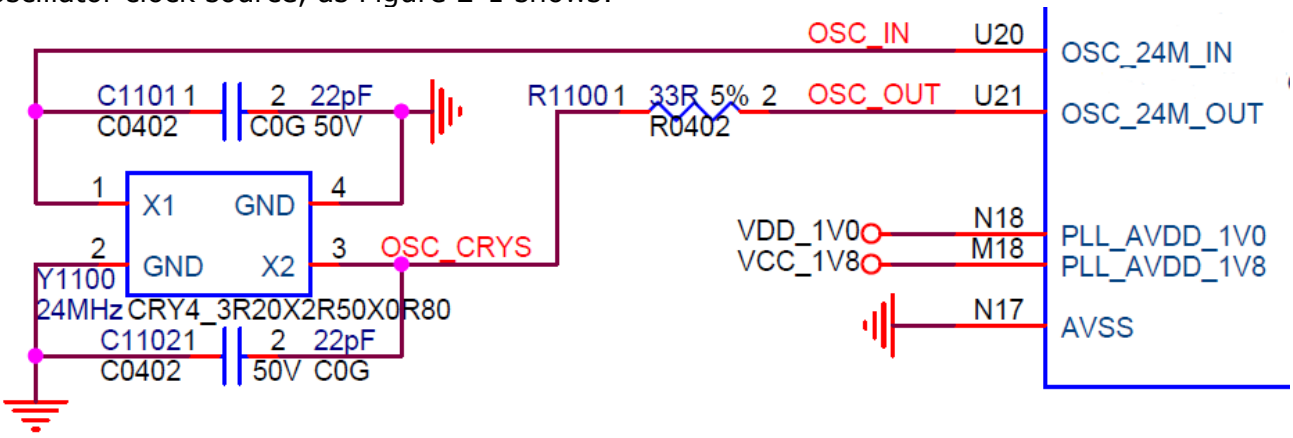


Figure 2-1 RK3326 Crystal Implementation

Note

The value of crystal load capacitance should be selected according to the load capacitance value of crystal. 22pF is the capacitance value of crystal used by Rockchip which may be not commonly used.

The system clock can also be generated by digital clock source. The 1.0V compatible clock source is connected to the XIN_OSC pin. In this mode of operation, the XOUT_OSC pin is left unconnected and should not be used to source any external components:

Table 2-1 RK3326 24MHz Digital Clock Source

Parameter	Spec.			Description
	Min.	Max.	Unit	
Frequency	24.000000		MHz	
Frequency Tolerance	+/-20		ppm	Frequency tolerance
Clock amplitude	1.0		V	Peak-to-Peak value
Operating Temperature	-20	70	℃	
ESR	/	40	Ohm	

The internal oscillator clock source will be switched to the external 32.768 KHz clock source to reduce the system power consumption when RK3326 is in standby mode. The signal can be acquired from PMIC or external RTC clock source, The clock input is shown as below:

Figure 2-2 RK3326 Standby Mode Clock Input

The external 32.768KHz RTC clock parameters are shown as below table:

Table 2-2 RK3326 32.768KHz Clock Requirement

Parameter	Spec.			Description
	Min.	Max.	Unit	
Frequency	32.768000		kHz	
Frequency Tolerance	+/-30		ppm	Frequency tolerance
Operating temperature	-20	70	℃	
Duty ratio	50		%	

2.1.2 Reset Circuit

RK3326 internally integrates POR (Power on Reset) circuit, low active, and the minimum pulse width time is 100 cycles of 24MHz clock (at least 4us), to ensure SoC operation stably and normally. The reset signal connects 100nF capacitor to eliminate the jitter to avoid the reset triggered mistakenly. Please place the capacitor close to the chip pin for layout.

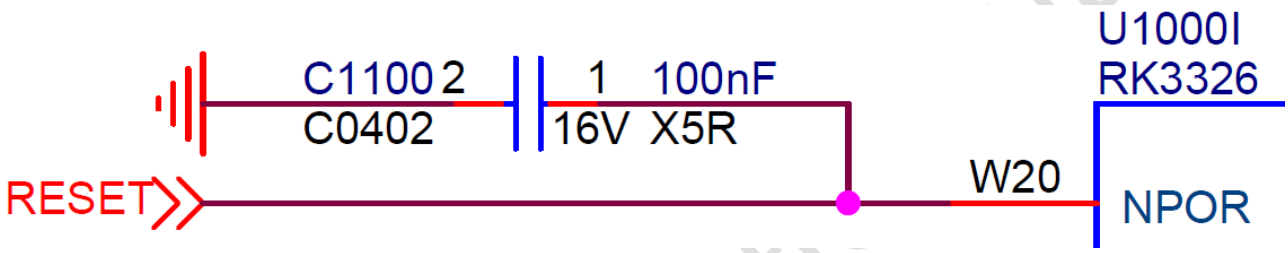


Figure 2-3 RK3326 Reset Input

2.1.3 System Boot Sequence

RK3326 supports boot from Nand/eMMC/SPI/SDMMC/USB, and boot priority from high to low as below:

- Nand FALSH
- eMMC FLASH
- SFC/SPI FLASH
- SDMMC CARD
- USB OTG

2.1.4 System Initialization Configuration Signal

RK3326 has two important signals which need to be configured before power-on. They are the IO supply configuration pin of VCCIO6 (FLASH) power domain and JTAG/SDMMC function control pin.

RK3326 VCCIO6 power domain's IO supply needs to be configured, because it belongs to FLASH power domain and the signal will be used during system boot up. When system boots up, it must specify the default level mode through the hardware configuration, and it cannot be adjusted through register. The configuration is shown as Table 2-3.

RK3326 reuses JTAG function and SDMMC function together to reduce IO, and use SDMMC0_DET pin to switch the output function, so it also needs to be configured before power-on, otherwise UART/JTAG without output will influence the debugging in boot up stage, while SDMMC without output will influence SDMMC boot function. The pin is shown as below:

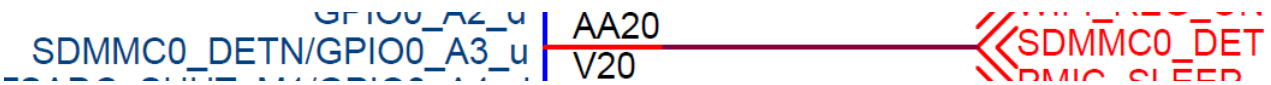


Figure 2-4 RK3326 SDMMC0/JTAG Reused Control Pin

The two pins configurations are shown in below table:

Table 2-3 RK3326 System Initialization Configuration Signal Description

signal name	internl pull up/down	description
FLASH_VOLSEL	pull up	FLASH(VCCIO6) power domain IO supply configuration pin: 0: IO level mode is 3.3V. 1: IO level mode is 1.8V (default).
SDMMC0_DET	pull up	JTAG pin resued to select control signal: 0: recognized as sd card insertion, SDMMC/JTAG/UART pin reused as SDMMC output. 1: recognized as SD card not insertion, SDMMC/JTAG/UART pin reused as JTAG/UART output (default).

2.1.5 JTAG Debug Circuit

RK3326 JTAG interface is compliant with IEEE1149.1 standard. PC can connect with DSTREAM emulator by SWD mode (Two-line mode) to debug internal ARM core within the SoC.

Before connecting the emulator, need to pull SDMMC0_DET pin high, otherwise it can not enter JTAG debugging mode.The JTAG interface description is shown as below table:

Table 2-4 RK3326 JTAG Debug Interface Signal

Signal name	Description
JTAG_TCK	AP JTAG clock inout
JTAG_TMS	AP JTAG mode select input

2.1.6 DDR Circuit

- **2.1.6.1 DDR Controller Introduction**

RK3326 DDR controller interface supports JEDEC SDRAM standard, and has features following:

- Support DDR3/DDR3L/DDR4/LPDDR2/LPDDR3 etc. standards;
- Provide one 32bit DDR controller interfaces, support data bus bit width 32bit/16bit configurable, and support address bus up to 16 bit.
- Support DDR up to 4GB.
- Support low power consumption modes such as Power Down, Self Refresh and so on.

- **2.1.6.2 DDR Topological Structure and Connection**

Take LPDDR3 as an example, RK3326 SDRAM topological structure is shown as below:

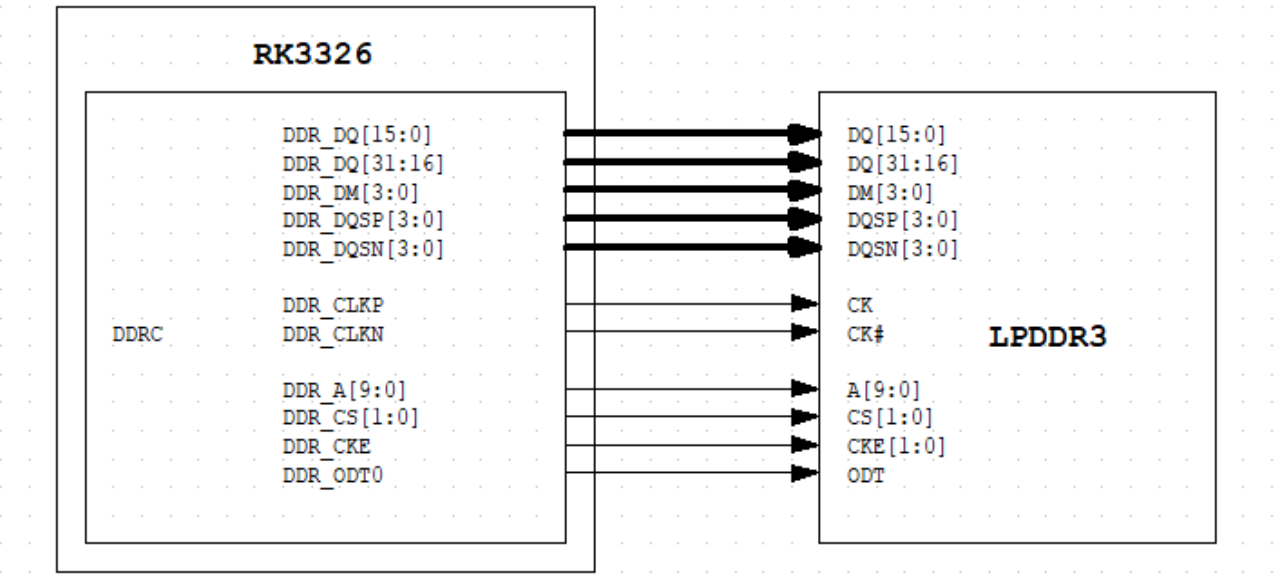


Figure 2-5 RK3326 LPDDR3 Topological Structure

- **2.1.6.3 DDR Power Up Sequence Requirement**

RK3326 DDR controller only has one group of power supply:

- DDRIO_VDD: Supply power for Core of DDR controller, interface I/O and Buffer.

SDRAM component has two groups of power supply. The power up sequence refers to JEDEC standard:

DDR3 SDRAM power up sequence is shown as below:

1. Apply power (RESET# is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET# needs to be maintained for minimum 200 us with stable power. CKE is pulled "Low" anytime before RESET# being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp, VDD > VDDQ and (VDD - VDDQ) < 0.3 volts.
   - VDD and VDDQ are driven from a single power converter output, AND
   - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
   - Vref tracks VDDQ/2.

OR

- Apply VDD without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
- The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

Figure 2-6 DDR3 SDRAM Power Up Sequence

LPDDR3 SDRAM power up sequence is shown as below:

After...	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2}—200mV
	V_{DD1} and V_{DD2} must be greater than V_{DDCA}—200mV
	V_{DD1} and V_{DD2} must be greater than V_{DDQ}—200mV
	V_{Ref} must always be less than all other supply voltages

Figure 2-7 LPDDR3 SDRAM Power Up Sequence

DDR4 SDRAM power up sequence is shown as below:

1. Apply power (RESET_n is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET_n needs to be maintained for minimum 200us with stable power. CKE is pulled " Low" anytime before RESET_n being de-asserted (min. time 10ns) . The power voltage ramp time between 300mV to V_{DD} min must be no greater than 200ms; and during the ramp, $V_{DD} \geq V_{DDQ}$ and (V_{DD}-V_{DDQ}) < 0.3volts. VPP must ramp at the same time or earlier than VDD and VPP must be equal to or higher than VDD at all times.
   - V_{DD} and V_{DDQ} are driven from a single power converter output, AND
   - The voltage levels on all pins other than V_{DD},V_{DDQ},V_{SS},V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side. In addition, V_{TT} is limited to TBDV max once power ramp is finished, AND
   - VrefCA tracks TBD.

   or
   - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}
   - Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} & VrefCA.
   - Apply VPP without any slope reversal before or at the same time as VDD.
   - The voltage levels on all pins other than V_{DD},V_{DDQ},V_{SS},V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.

Figure 2-8 DDR4 SDRAM Power Up Sequence

● 2.1.6.4 DDR Support List

RK3326 DDR interfaces DDR3/LPDDR3 support operating frequency up to 800MHz. Please refer to the document 《RK DDR Support List》 released by Rockchip for the components available. The document can be downloaded from redmine through below link:
https://redmine.rockchip.com.cn/projects/fae/documents?tdsourcetag=s_pctim_aiomsg

2.1.7 eMMC Circuit

● 2.1.7.1 eMMC Controller Introduction

RK3326 eMMC interface supports eMMC 4.51 and is also compatible with 4.41, 5.0 and 5.1 protocol. The controller supports the following features:

- Support SFC FLASH, Nand FLASH and eMMC FLASH.
- Support 1-bit, 4-bit and 8-bit mode of data bus width.
- Support HS200 mode at most, but not support CMD Queue.

● 2.1.7.2 eMMC Topological Structure and Connection

eMMC interface supported pull up/down and the matching design are recommended as Table 2-5:

Table 2-5 RK3326 eMMC Interface Design

Signal	internal pull up/down	connection method	Description(chip side)
eMMC_DQ[7:0]	pull up	direct connection	eMMC data output/input
eMMC_CLK	pull up	Series connect 22ohm resistor	eMMC clock output

eMMC_CMD	pull up	direct connection	eMMC command output/input

- **2.1.7.3 eMMC Power Up Sequence Requirement**

RK3326 eMMC controller only has one group of power supply:

- VCCIOO: I/O power of eMMC controller

eMMC component has two groups of power supply. The power up sequence refers to JEDEC standard:

- VCC and VCCQ have no required sequence in power-on.
- VCC and VCCQ must be powered up before RK3326 CMD command is sent out, and the power supply must work stably.
- RK3326 can power VCC off to reduce the power consumption in sleep mode;
- VCC power must be powered up and work stably before the component is wakened from sleep mode.

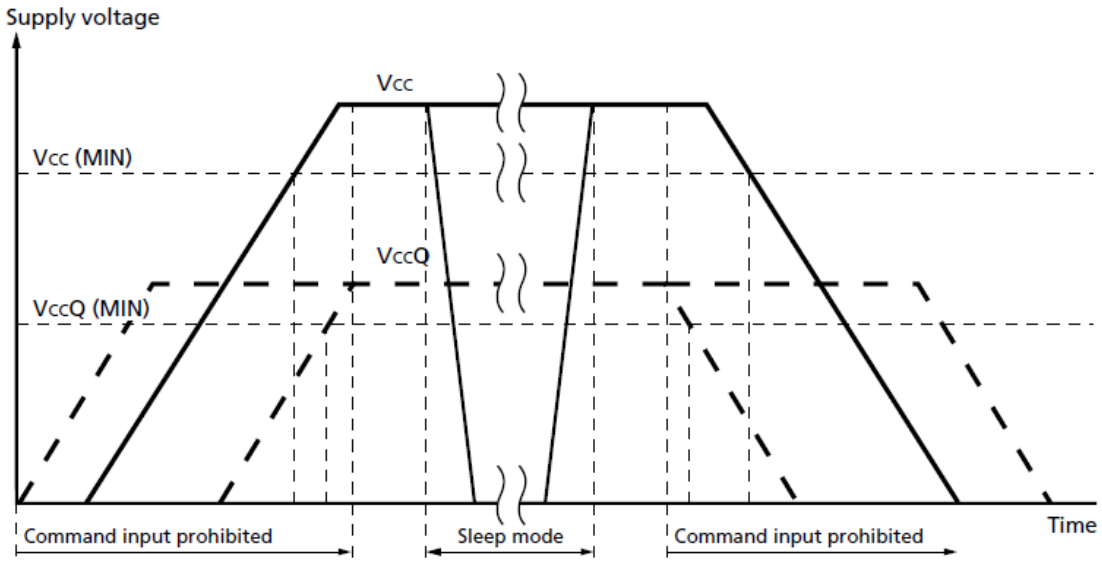


Figure 2-9 eMMC Flash Power Up/Down Sequence

- **2.1.7.4 eMMC Support List**

RK3326 eMMC support list please refer to《RK eMMCSupportList》released by Rockchip. The document can be downloaded from redmine through below link:
https://redmine.rockchip.com.cn/projects/fae/documents?tdsourcetag=s_pctim_aiomsg

2.1.8 SPI Circuit

- **2.1.8.1 SPI Controller Introduction**

RK3326 has 2 SPI controllers which can be used to connect SPI devices and SPI0 can be used as boot.

- **2.1.8.2 SPI Topological Structure and Connection**

SPI interface pull up/down and the matching design are recommended as below table:

Table 2-6 RK3326 SPI Interface Design

Signal	Internal pull up/down	Connection method	Description(chip side)
SPI0_MOSI	pull down	Direct connection	SPI data output

SPI0_MISO	pull up	Direct connection	SPI data input
SPI0_CLK	pull up	Series connect 22ohm resistor	SPI clock output
SPI0_CSN	pull up	Direct connection	SPI chip select signal

- **2.1.8.3 SPI Power Up Sequence Requirement**

SPI controller power up sequence should follow the power up sequence requirement of GPIO power domain.

SPI Flash component only has one power, so there is no requirement on power up sequence.

2.1.9 GPIO Circuit

RK3326 GPIO type is 1.8V/3.3V configurable.

- **2.1.9.1 GPIO Driving Capability**

RK3326 GPIO provides 4 level of driving capability to adjust which is 2mA/4mA/8mA/12mA. The default driving capability is different according to different GPIO types. Please refer to TRM to modify the configuration.

- **2.1.9.2 GPIO Power**

The power pin of GPIO power domain is described as below:

Table 2-7 RK3326 GPIO Power Pin Description

Power domain	GPIO type	Pin name	Description
PMUIO1	1.8V/3.3V	PMUIO_VDD_1V0	1.0V logic power for this GPIO domain (group).
		PMUIO1	1.8V or 3.3V IO supply for this GPIO domain (group).
PMUIO2	1.8V/3.3V	PMUIO2	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO1	1.8V/3.3V	VCCIO1	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO2	1.8V/3.3V	VCCIO2	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO3	1.8V/3.3V	VCCIO3	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO4	1.8V/3.3V	VCCIO4	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO5	1.8V/3.3V	VCCIO5	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO6	1.8V/3.3V	VCCIO6	1.8V or 3.3V IO supply for this GPIO domain (group).

2.2 Power Design

2.2.1 Minimum System Power Introduction

- **2.2.1.1 Power Requirement**
  - PLL:PLL_AVDD_1V0、PLL_AVDD_1V8
  - CPU:VDD_ARM
  - LOGIC&GPU:VDD_LOG
  - DDR: VCC_DDR
  - GPIO:PMUIO_VDD_1V0、PMUIO1、PMUIO2

- **2.2.1.2 Power Up Sequence**

Theoretically follow the rule to power up the low voltage earlier than the high voltage in the same IP and the same voltage in one IP could be powered up at the same time. There is no sequence requirement among different IPs.

Recommended power up sequence refers to below:

PLL_AVDD_1V0&PMUIO_VDD_1V0&VDD_LOG-→VDD_CPU-→PLL_AVDD_1V8-→VCC_DDR-→PMUIO1&PMUIO2

2.2.2 Power Design Recommendation

- **2.2.2.1 Standby Circuit Solution**

RK3326 system uses the standby solution and the system consists of constant power supply area and power-off in standby area which supply power independently as shown below:

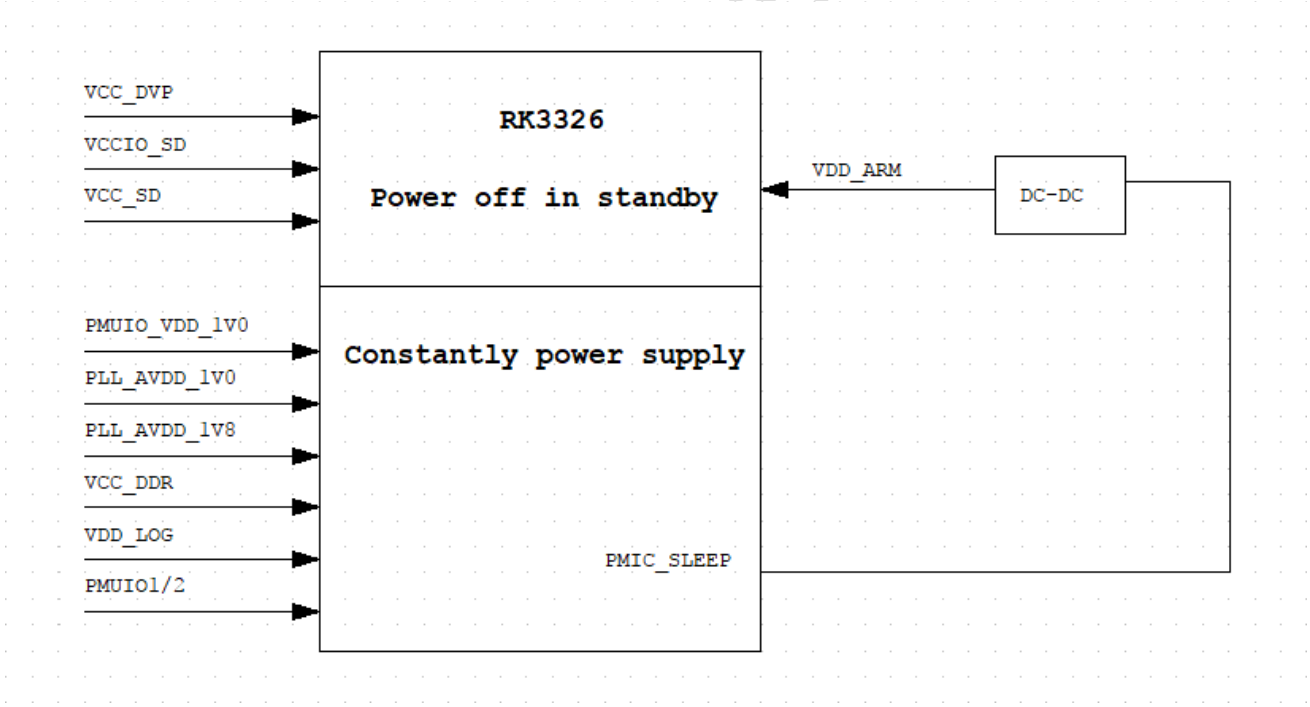


Figure 2-10 RK3326 Standby Circuit Solution

The power of the power-off in standby area is controlled by PMIC to turn off each independent power supply and PMIC_SLEEP_H is used to control other powers to turn off the power supply in standby mode.

The power of the constant power supply area is directly provided by the power chip and at least the following 4 groups of power must be always on in standby:

- DDR: VCC_DDR, power for DDR self-refresh.
- GPIO:PMUIO1 & PMUIO2, provide IO power for PMUIO1 & PMUIO2 power domain to maintain output status and interrupt response.
- LOGIC: PMUIO_VDD_1V0 & VDD_LOG, provide power for Logic core of PMUIO1 &

PMUIO2 power domain.

- PLL: PLL_AVDD_1V0&PLL_AVDD_1V8, provide power for PLL and CPU OSC to work.

- **2.2.2.2 PLL Power**

RK3326 internally has 6 PLL as allocated below:

Table 2-8 RK3326 Internal PLL Introduction

	Quantity	Power	status in Standby
PMU/OSC	1	PMU_VDD_1V0、PMUIO1	Cannot turn off the power supply
Part inside SoC	5	PLL_AVDD_1V0，PLL_AVDD_1V8	Cannot turn off the power supply

Recommend to use a LDO as a separate power supply for PLL, especially when DDR operating frequency is relatively high, the stable PLL power is helpful for improving the stability. The decoupling capacitor should be placed close to the pin.

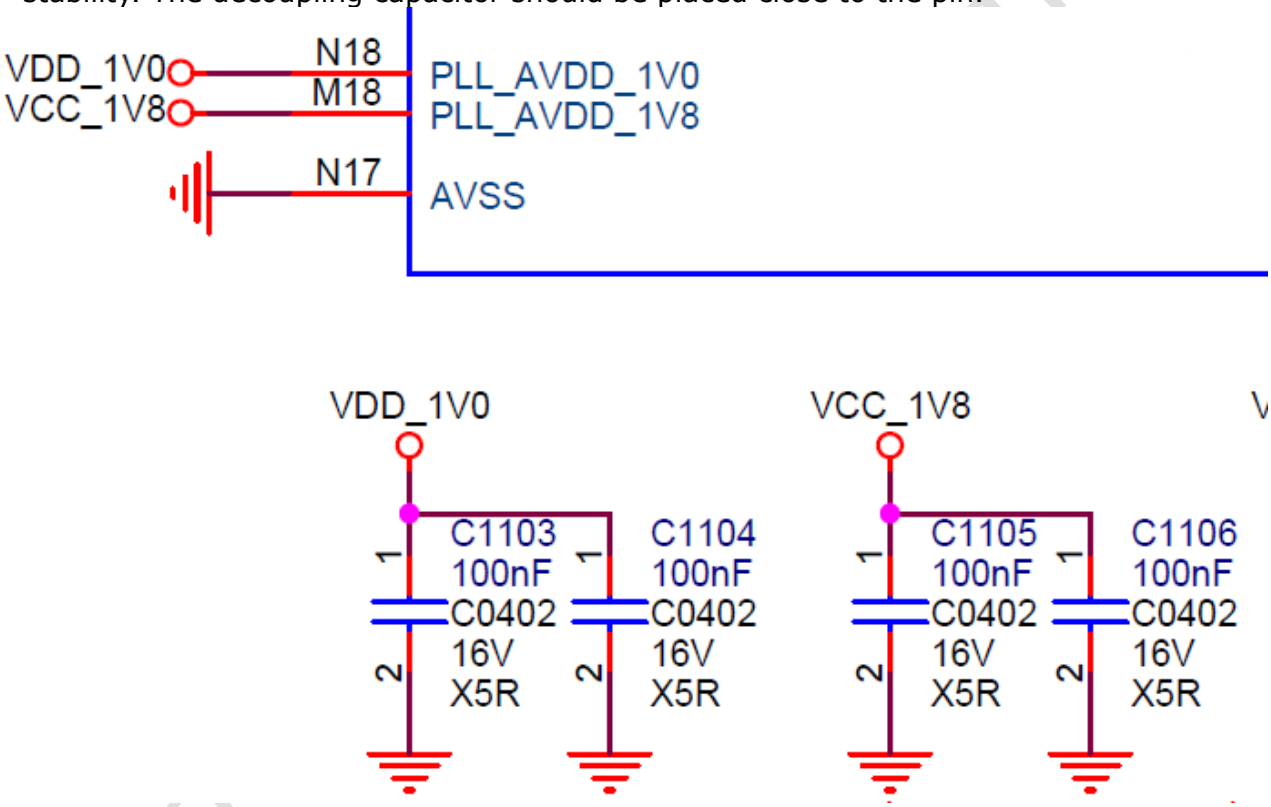


Figure 2-11 RK3326 PLL Power

- **2.2.2.3 CPU Power**

RK3326 uses independent power domains to supply power for CPU, as shown in below figure, VDD_ARM supplies power for ARM Cortex-A53 core. Support DVFS (Dynamic Voltage Frequency Scaling) function. Use separate DC-DC power supply and the peak current could be up to 1.2A, so please do not reduce or delete the capacitors as required in RK3326 reference design schematic. For layout, the high- capacity capacitors should be placed on the back of RK3326 chip (close to the chip for boards of single-sided SMT) to ensure that the power ripple is controlled within 60mV to avoid the power ripple abnormality with high load. The capacitor is shown as below:

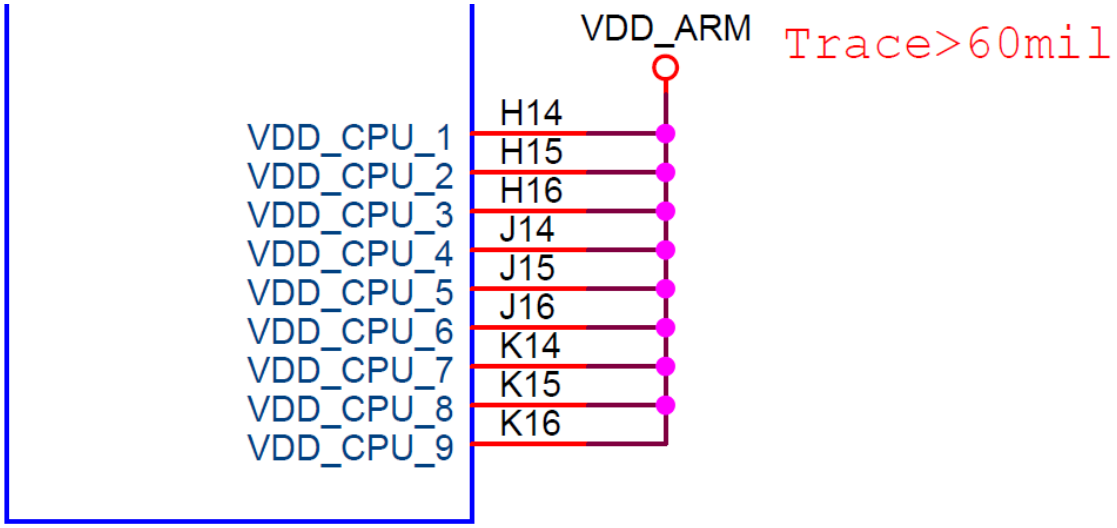


Figure 2-12 RK3326 VDD_CPU Power

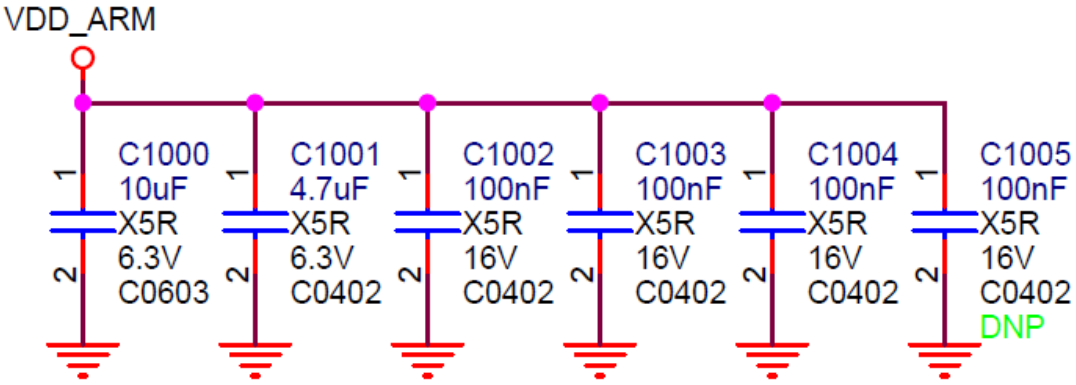


Figure 2-13 RK3326 VDD_CPU Power Decoupling

- **2.2.2.4 GPU&LOGIC Power**

RK3326 uses DC-DC to supply power separately for GPU & LOGIC, such as power supply of VDD_LOG in below figure, supports DVFS (Dynamic Voltage Frequency Scaling) function and the peak current could be up to 1.1A, so please do not reduce or delete the capacitors required in RK3326 reference design schematic. For layout, the high-capacity capacitors should be placed on the back of RK3326 chip (close to the chip for boards of single-sided SMT) to ensure that the power ripple is controlled within 60mV to avoid the power ripple abnormality with high load. The capacitor is shown as below:

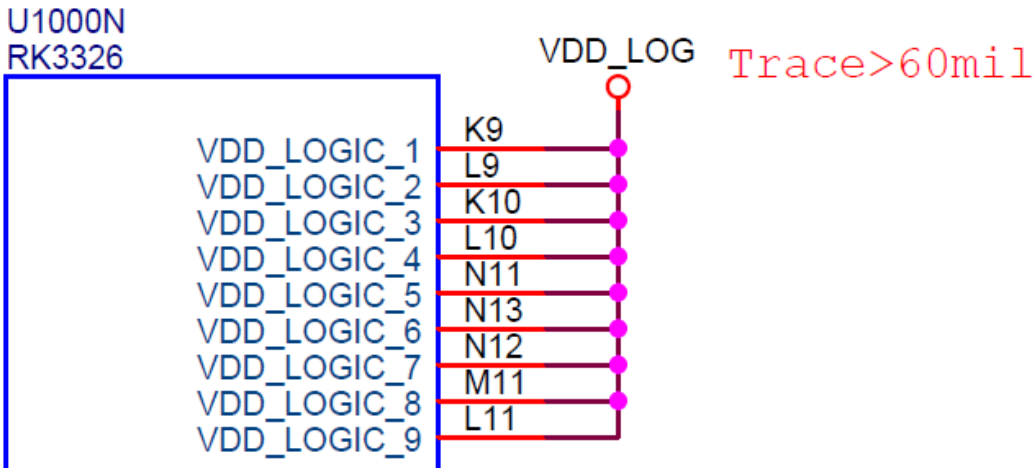


Figure 2-14 RK3326 VDD_GPU Power

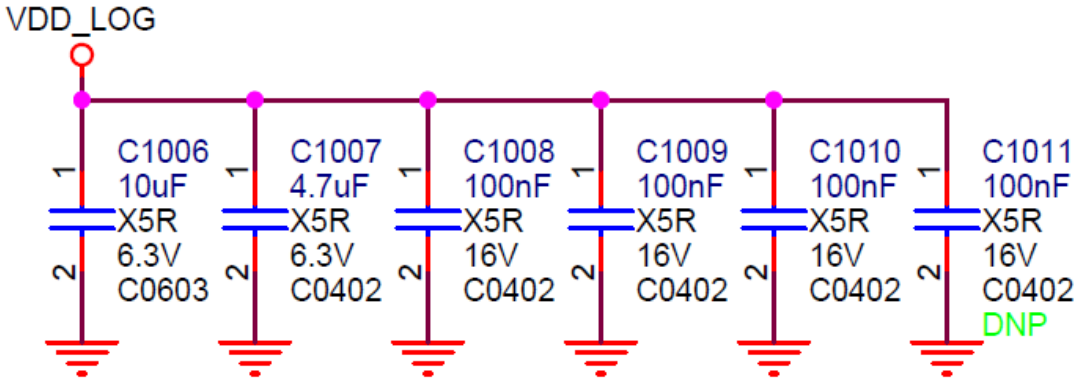


Figure 2-15 RK3326 VDD_GPU Power Decoupling

- **2.2.2.5 DDR Power**

RK3326 DDR controller interface supports DDR3/DDR3L/DDR4/LPDDR2/LPDDR3 protocol. Only need to supply power for DDRIO_VDD and the power level is different for different DDR components. There are three levels 1.2V/1.35V/1.5V to be adjusted. Please confirm to meet the product design requirement according to the component used.

RK3326 DDR controller internally integrates Vref circuit to generate the required reference voltage: Vref=VCC_DDR/2. The Vref of SDRAM side is generated by resistance divider circuit, Vref_CA=VCC_DDR/2, while Vref_DQ can be adjusted according to ODT strategy, the corresponding Vref voltage can be adjusted according to the drive strength and the ODT value.

Take LPDDR3 as an example: At 800MHz frequency, the driving capability of RK3326 chip side is 34.3ohm, SDRAM side ODT is configured as 240ohm, when ODT is enabled, calculate according to the formula SDRAM Vref=0.56*VCC_DDR.

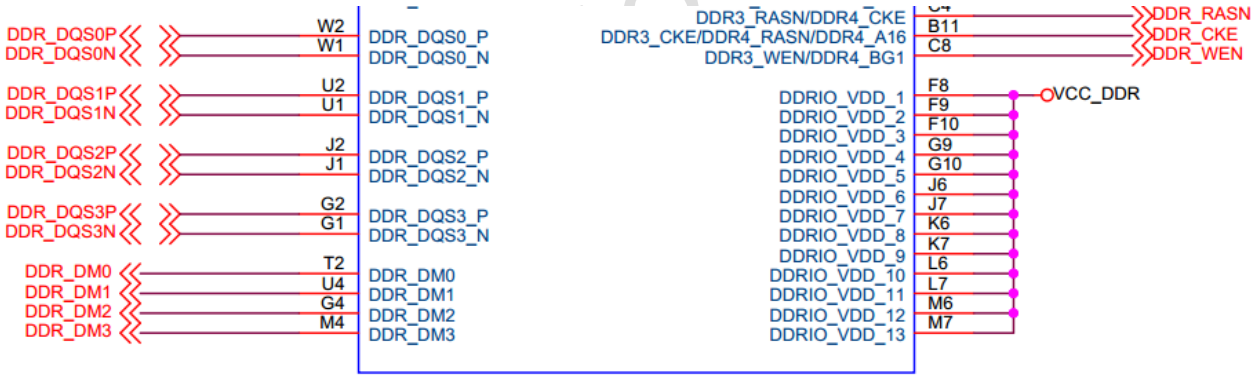
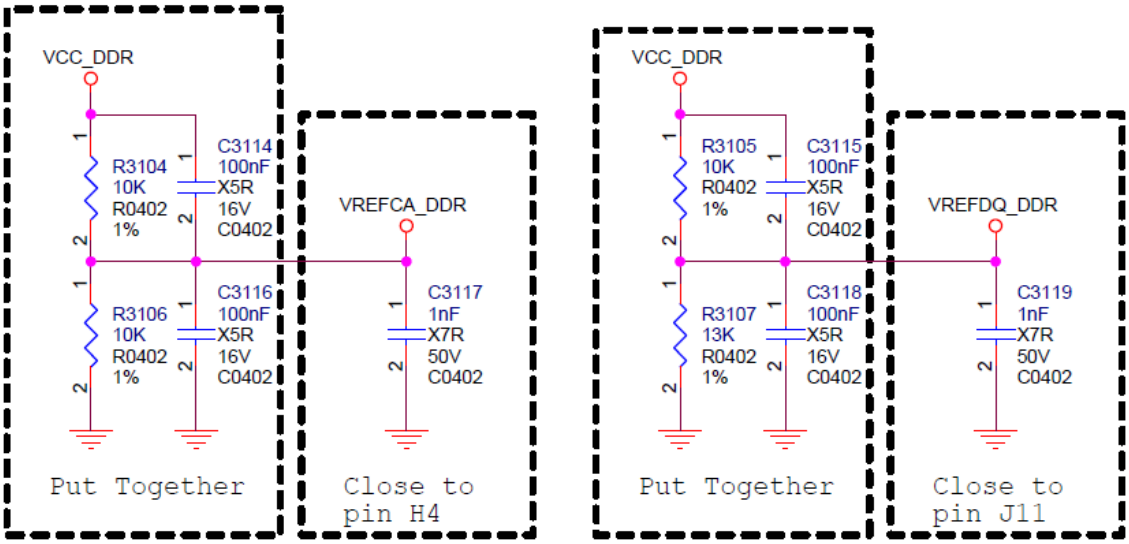


Figure 2-16 RK3326 VCC_DDR Power



Note:
Vih=VCC
Vil=VCC*Ron/(Ron+Rodt)
VREFDQ_DDR=(Vih+Vil)/2

eg:VCC=1.2V,Ron=34ohm,Rodt=240ohm
so,Vih=1.2V,Vil=0.149V,VREFDQ_DDR=0.674V

Figure 2-17 RK3326 LPDDR3 SDRAM VREF Power Design

Note

As for Vref_DQ design of different components:
LPDDR2 doesn't support ODT function; DDR4 Vref_DQ can be adjusted through software within the component; DDR3/DDR3L internal pull up/down will occur at the same time when ODT function is enabled, Vref_DQ=Vref_CA=VCC_DDR/2; so only LPDDR3 needs to adjust Vref_DQ separately.

The SDRAM VREF_DQ and VREF_CA of LPDDR3 use a separate VREF voltage reference circuit. The power of VREF_DQ pin can be supplied by a 1K ohm resistors divider (1% accuracy), because VREF_CA power is constantly supplied, change to use a 10Kohm resistors divider (1% accuracy) can reduce the standby power consumption and parallel connect 100nF capacitor can improve the power following characteristic of VCC_DDR. Place a 1nF decoupling capacitor close to each reference power pin.

- **2.2.2.6 GPIO Power**

Refer to Section 2.1.9 for GPIO power. Recommend to place a 100nF decoupling capacitor close to each power pin. For detailed design please refer to RK3326 reference design schematic.

2.2.3 RK817-1 Solution Introduction

- **2.2.3.1 RK817-1 Block Diagram**

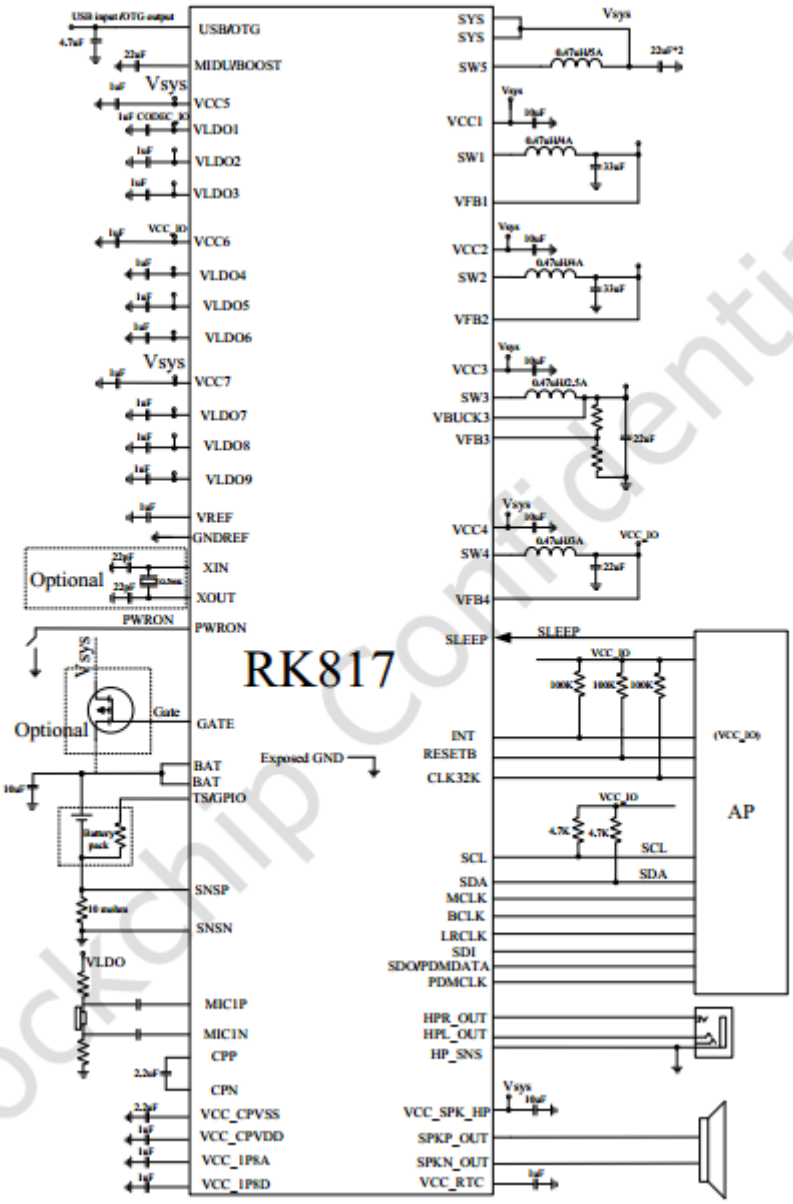


Figure 2-18 RK817-1 Block Diagram

- **2.2.3.2 RK817-1 Features**
  - Input range: 3.8V - 5.5V for USB input; 2.7V - 5.5V for BAT input
  - Switch mode Li-ion battery charger providing charging current up to 3.5A
  - Power path controller with 4A current path with optional extended external mos
  - Accurate battery fuel gauge with two separate battery voltage and current ADC
  - Real time clock（RTC）
  - Low standby current of 16uA (at 32.768KHz clock frequency)
  - Real ground HeadPhone driver
  - 1.3W ClassD PA without external filter inductor
  - OTP Programmable power up/down sequences and voltage
  - High performance Audio CODEC
    - One internal PLL
    - Support microphone input
    - Support I2S as the digital signal interface for both DAC and ADC
    - Support Automatic Level Control(ALC),limiter and noise gating
    - Support programmable digital and analog gains
    - Audio resolution from 16bits to 32bits
    - Sample rate up to 192KHz
    - Provides master and slave work mode, software configurable

- Support 3 I2S formats (normal, left-justified, right-justified)
- Support PDM mode(external input PCLK)

- Power channels:
  - CH1:Synchronous BUCK converter,2.5A max
  - CH2:Synchronous BUCK converter,2.5A max
  - CH3:Synchronous BUCK converter,1.5A max
  - CH4:Synchronous BUCK converter,1.5A max
  - CH5:Synchronous BOOST converter,1.5A max(Can not be used at the same time with the charger function)
  - CH6~CH7,CH9~CH14:LDOs, 400mA max
  - Channel 8: low dropout regulator with low noise, high power supply rejection ratio, 100mA max
  - CH15:OTG Switch,1.5A max(Can not be used at the same time with the charger function)
- Package: 7mmx7mm QFN68

2.2.3.3 RK3326+RK817-1 Power Tree

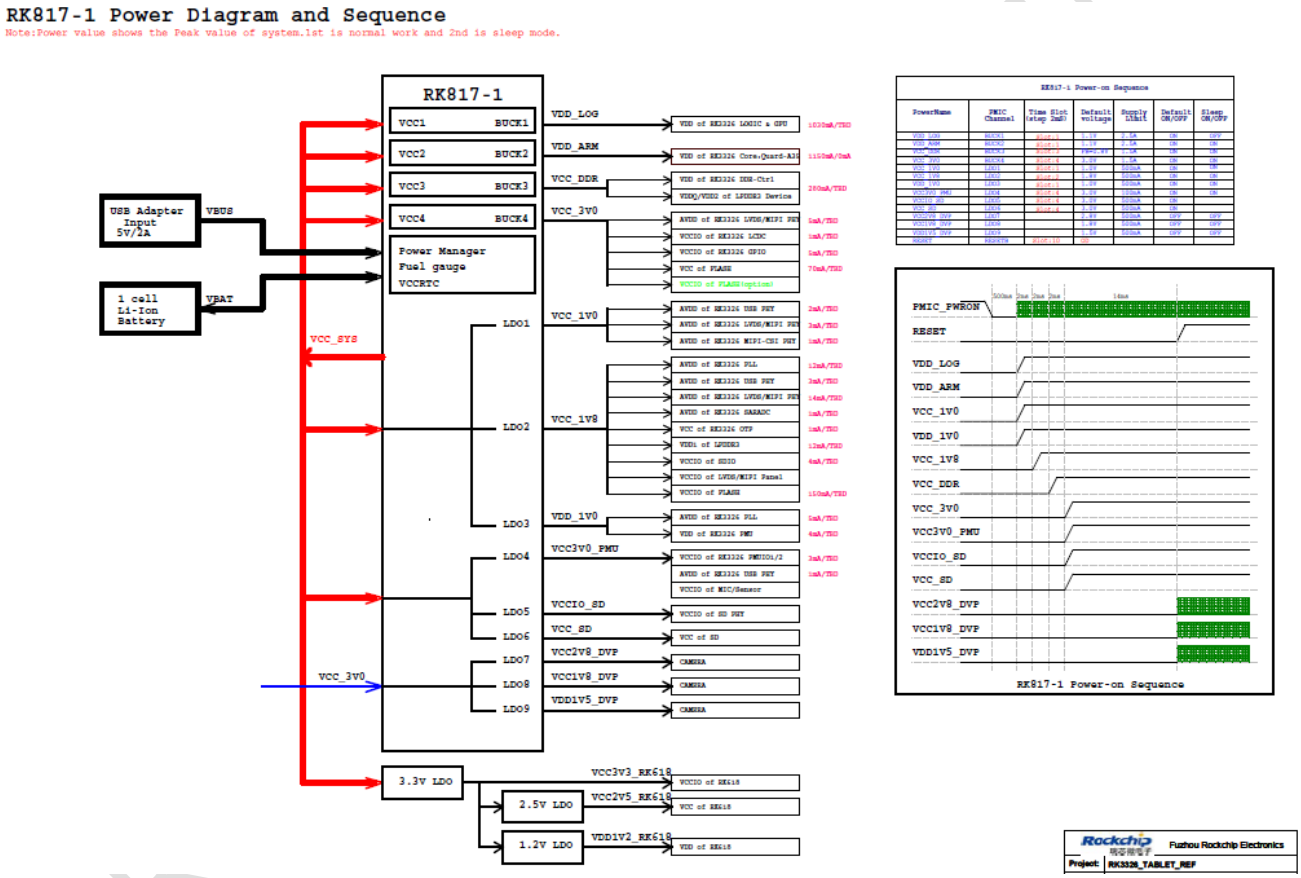


Figure 2-19 RK817-1 Power Tree

2.2.3.4 RK817-1 Notice

- The recommended matching capacitance of 32.768kHz crystal is 22pF, and users can fine tune the parameter according to the specification of the crystal used.

Note

In order to reduce the power consumption, PMIC RTC crystal oscillation is relatively weak, can not measure the oscillation signal on the XOUT or XIN pin with a normal oscilloscope, or oscilloscope probe will cause OSC stop working. Please test CLK32K pin if want to measure 32.768K signal.

- The output capacitance of BUCK1, BUCK2 must be bigger than 30uF to ensure the good decoupling effect, especially in the case with large current and high dynamic load, you can appropriately increase the output decoupling capacitance.
- RK817-1 has the function of USB OTG power supply, short circuit protection, and can configure 1.0-1.5A output current limit.
- The power on/off logic controlled by the switch is: PWRON pin embeds pull up resistor, pull up to VCCRTC, it will automatically power on when detecting the low level over 500ms. After power on, if PWRON pin is pulled down over 6s, it will power off forcely (usually used for forced power off after system crash, then power on). Before sleep and resume operation, the low level of PWRON pin should maintain over 20ms.
- RK817-1 work basic condition:
  - VBAT is bigger than 3.3V or VBUA is bigger than 4.4V.
  - When detecting one of below three cases, RK817-1 will automatically power on: PWRON pin keeps low level for 500ms; USB insertion; internal RTC Alarm power on is enabled and the time is up.
  - Start the power up process, each sequence interval is 2ms, the next sequence continues only when the output voltage of last sequence meets the requirement, until all the sequences power up end, and release reset, finish the power up process.

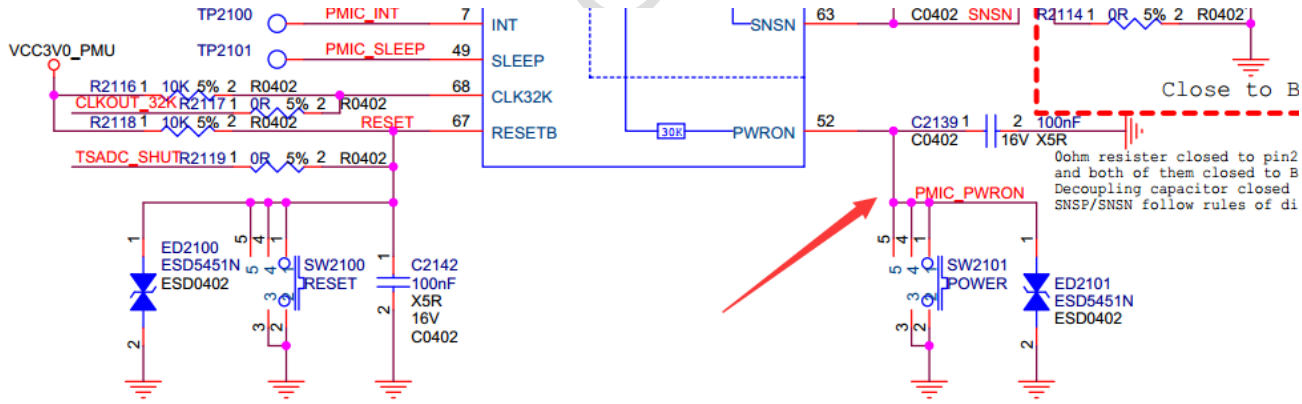


Figure 2-20 RK817-1 PWRON Pin

- When RK817-1 detects one of below two cases, it will automatically power off:
  - I2C write DEVICE_OFF=1
  - PWRON pin keeps low over 6s.
- When RK817-1 starts the power down process, it will pull down reset after one RTC clock cycle (around 30.5us), and then turn off all power output after 2ms, finish the power down process.
- When desigh of 1-cell li-on battery circuit discharge at a large current, the battery voltage is easy to drop because of the huge instantaneous current. However, when the fuel gauge detects that the battery voltage is lower than the set power off voltage, it enters the power off process, which will result in the remaining battery power not being released, causing the short battery life fo product. In this case, it is necessary to minimize the resistance of power circuit and battery.The

internal resistance of the power circuit is shown as the red arrow in the figure below. For PCB layout, try to use short and wide trace or copper to connect, drill as many vias as possible near the trace when change layer. The internal resistance of the battery should be reduced by using a low internal resistance battery cell and use protection board and power cord with lower conduction impedance.

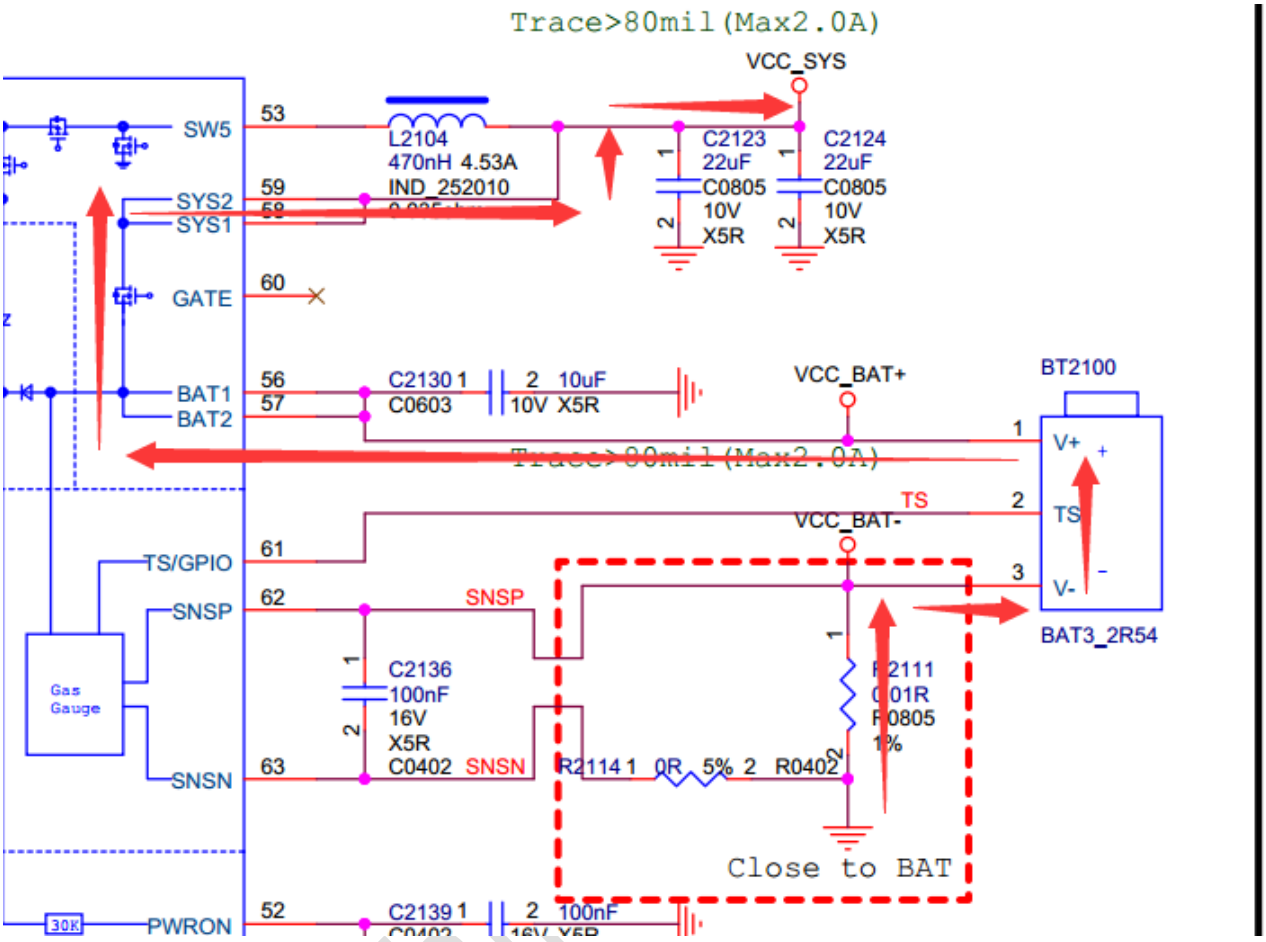


Figure 2-21 RK817-1 Battery Discharing Path

- **3.2.3.5 RK817-1 Design Instruction**

For the detailed design instruction of RK817-1, please refer to RK PMIC related design document 《RK817 Application Guide》.

2.2.4 RK809-1 Solution Introduction

- **2.2.4.1 RK809-1 Block Diagram**

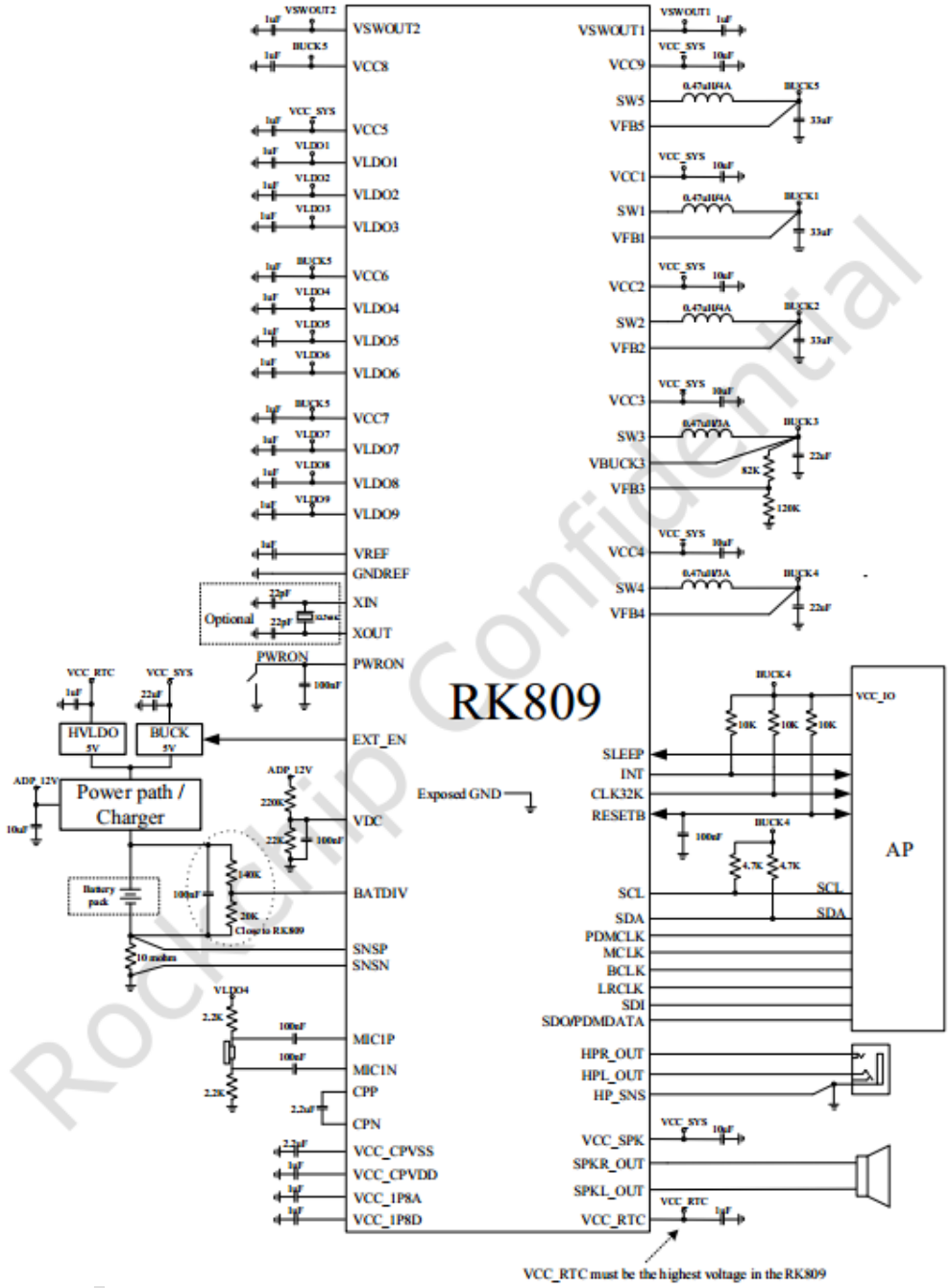


Figure 2-22 RK809-1 Block Diagram

- **2.2.4.2 RK809-1 Features**
  - Input range: 2.7V - 5.5V
  - Accurate battery fuel gauge with two separate battery voltage and current ADC
  - Real time clock（RTC）
  - Low standby current of 25uA (at 32.768KHz clock frequency)
  - Real ground HeadPhone driver
  - 1.3W ClassD PA without external filter inductor
  - OTP Programmable power up/down sequences and voltage
  - High performance Audio CODEC
    - One internal PLL
    - Support microphone input
    - Support I2S as the digital signal interface for both DAC and ADC
    - Support Automatic Level Control(ALC),limiter and noise gating
    - Support programmable digital and analog gains
    - Audio resolution from 16bits to 32bits

- Sample rate up to 192KHz
- Provides master and slave work mode, software configurable
- Support 3 I2S formats (normal, left-justified, right-justified)
- Support PDM mode(external input PCLK)

- Power supply:
  - CH1:Synchronous BUCK converter,2.5A max
  - CH2:Synchronous BUCK converter,2.5A max
  - CH3:Synchronous BUCK converter,1.5A max
  - CH4:Synchronous BUCK converter,1.5A max
  - CH5:Synchronous BUCK converter,2.5A max
  - CH6~CH7,CH9~CH14:LDOs, 400mA max
  - CH8:Low noise, high PSRR LDO,100mA max
  - CH15: Switch,1.5A max
  - CH16: Switch,3A max
- Package: 7mmx7mm QFN68

- **2.2.4.3 RK3326+RK809-1 Power Tree**

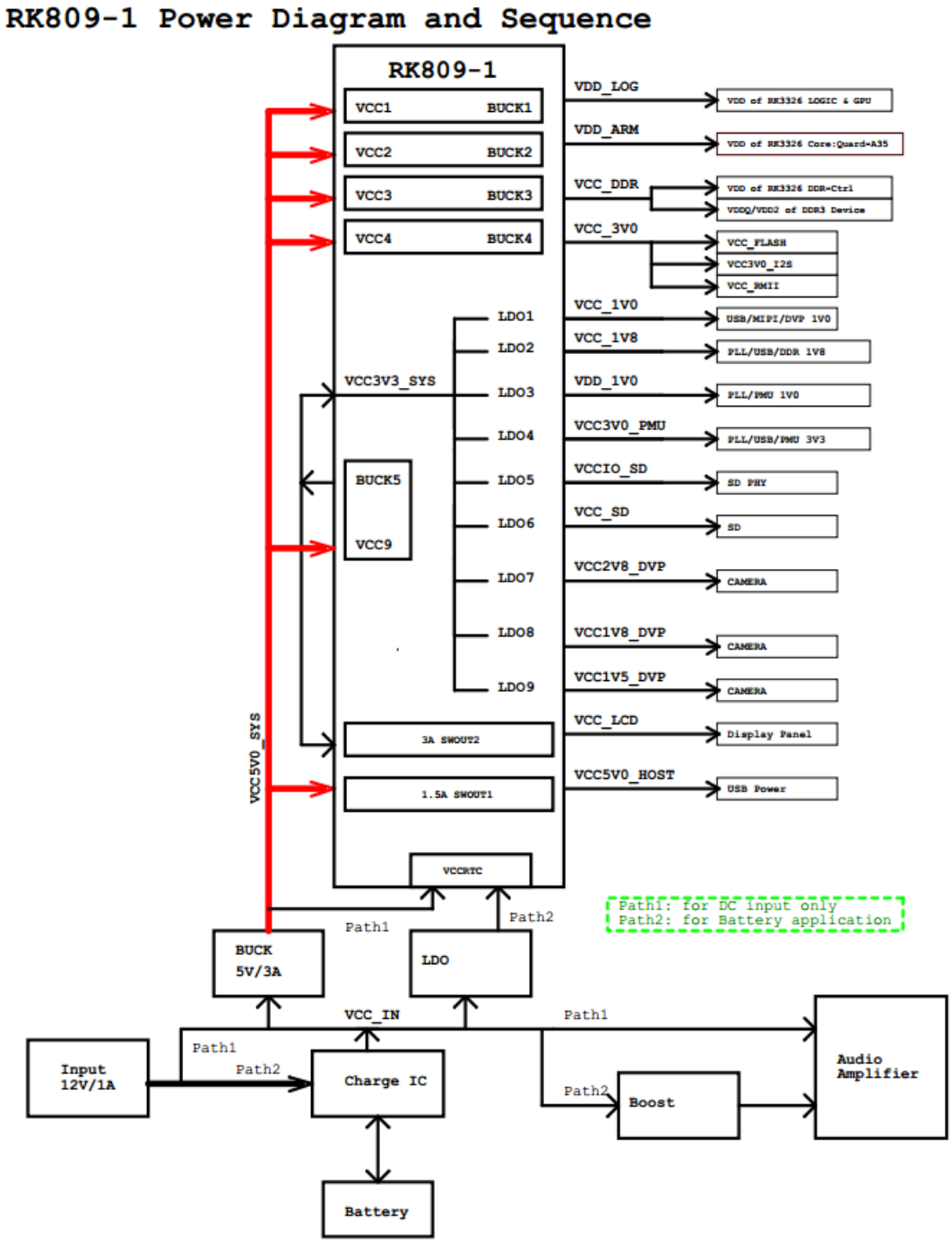


Figure 2-23 RK809-1 Power Tree

- **3.2.4.4 RK809-1 Notice**
  - The recommended matching capacitance of 32.768KHz crystal is 22pF, and users can fine tune the parameter according to the specification of the crystal used.

Note

In order to reduce the power consumption, PMIC RTC crystal oscillation is relatively weak, can not measure the oscillation signal on the XOUT or XIN pin with a normal oscilloscope, or oscilloscope probe will cause OSC stop working. Please test CLK32K pin if want to measure 32.768K signal.

  - VCC_RTC must be powered up first and the voltage value must be the highest one of the input powers supplying for RK809-3.

- The output capacitance of BUCK1, BUCK2 must be bigger than 30uF to ensure the good decoupling effect, especially in the case with large current and high dynamic load, you can appropriately increase the output decoupling capacitance.
- RK809-1 has the function of USB OTG power supply, short circuit protection, and can configure 1.0-1.5A output current limit.
- The power on logic directly controlled by input power is: when power input exists, primary DCDC buck output VCC5V0_SYS and VCC_RTC, the level input to VDC after external voltage divider circuit is more than 0.55V, and then PMIC starts to work and output the voltage.
- The power on/off logic controlled by the switch is: PWRON pin embeds pull up resistor, pull up to VCCRTC, it will automatically power on when detecting the low level over 500ms. After power on, if PWRON pin is pulled down over 6s, it will power off forcely (usually used for forced power off after system crash, then power on). Before sleep and resume operation, the low level of PWRON pin should maintain over 20ms.
- RK809-1 work basic condition:
  - VCC_RTC supply power.
  - VCC5V0_SYS supply power.
  - When detecting one of below three cases, RK809-1 will automatically power on: PWRON pin keeps low level for 500ms, VDC level is over 0.55V, internal RTC Alarm power on is enabled and the time is up.
  - Start the power up process, each sequence step is 2ms, the next sequence continues only when the output voltage of last sequence meets the requirement, until all the sequences power up end, and release reset, finish the power up process.

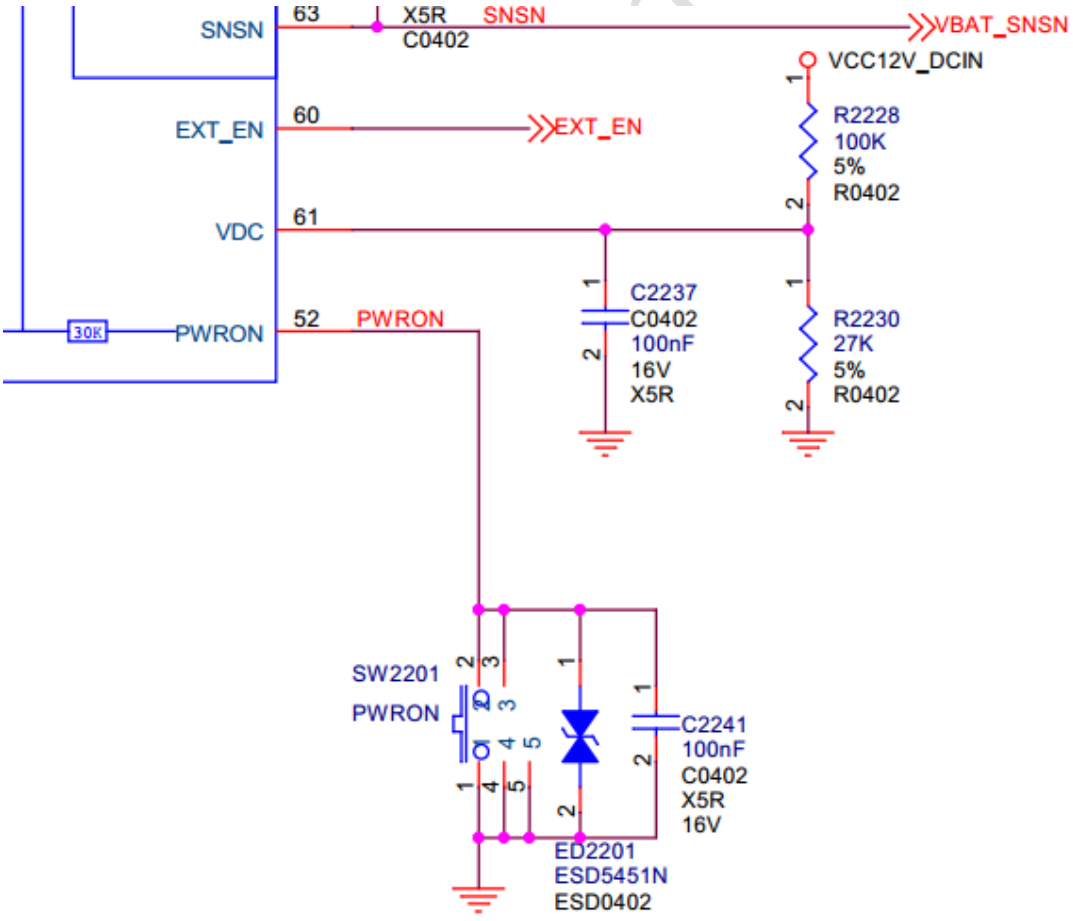


Figure 2-24 RK809-1 PWRON Pin

- When RK809-1 detects one of below two cases, it will automatically power off:
  - I2C write DEVICE_OFF=1

◆ PWRON pin keeps low over 6s.

■ When RK809-1 starts the power down process, it will pull down reset after one RTC clock cycle (around 30.5us), and then turn off all power output after 2ms, finish the power down process.

- **3.2.4.5 RK809-1 Design Instruction**

For the detailed design instruction of RK809-1, please refer to RK PMIC related design document 《RK809 Application Guide》.

2.2.5 Others

- **2.2.5.1 Over Temperature Protection Circuit**

When RK3326 occurs over-temperature or crash, the TSADC_SHUT pin of the chip will output low level to reset RK817-1 or RK809-1, and control the power off and restart, reset the whole system while the register is cleared.

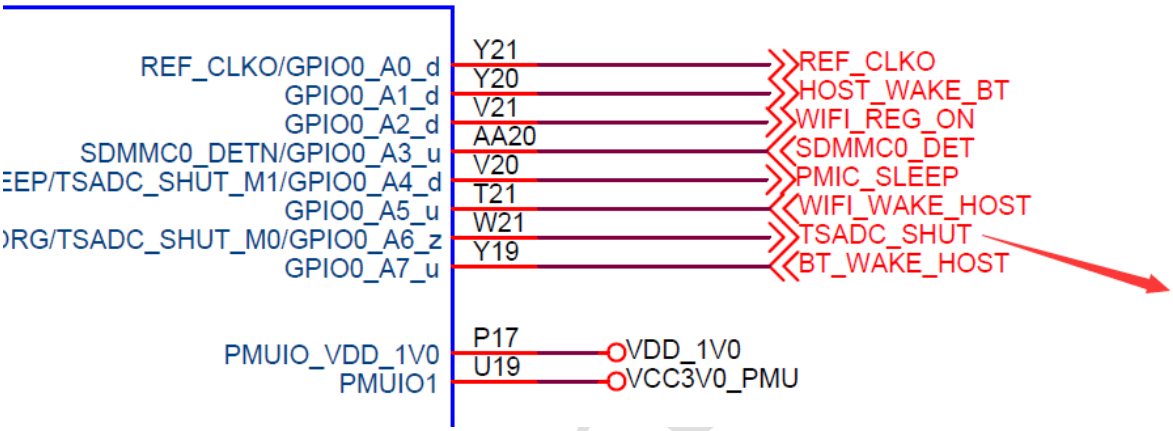


Figure 2-25 RK3326 OTP_OUT Over Temperature Protection Output

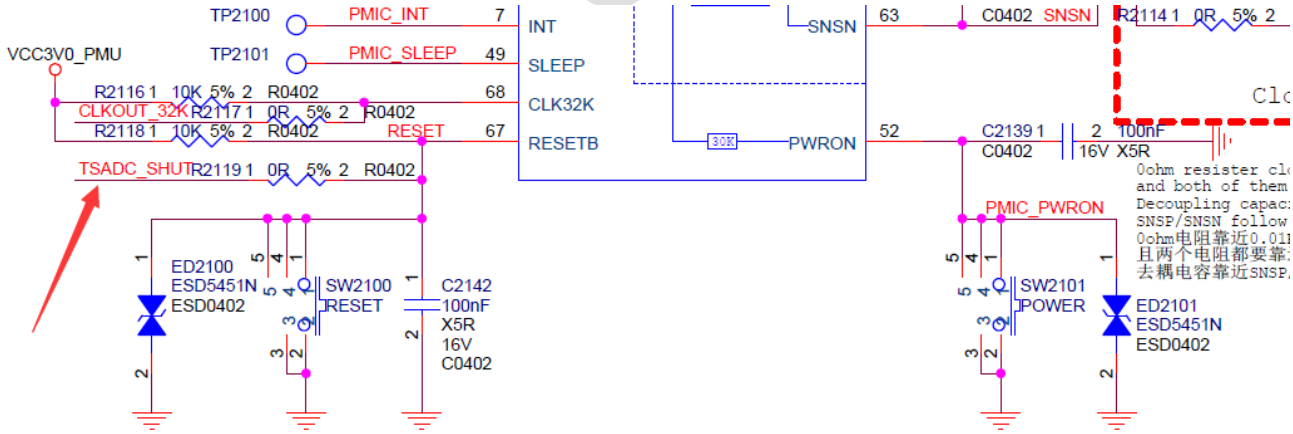


Figure 2-26 RK817-1 OTP_OUT Over Temperature Protection Input

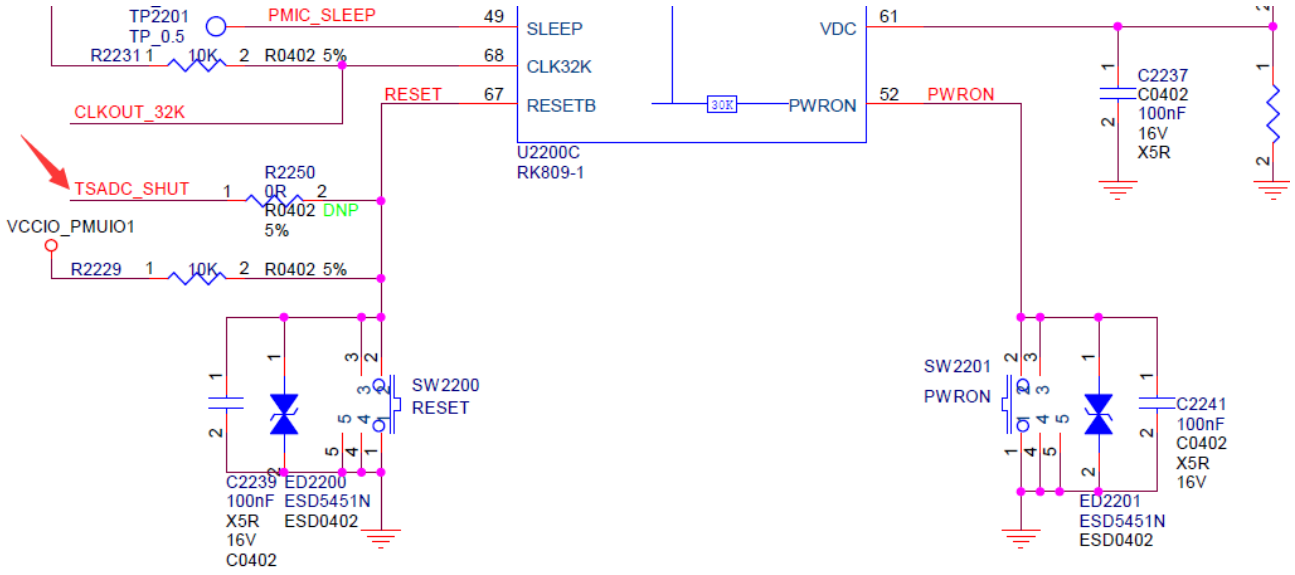


Figure 2-27 RK809-1 OTP_OUT Over Temperature Protection Input

- **2.2.5.2 PMIC Sleep Circuit**

When RK3326 is in work mode, the status pin PMIC_SLEEP of the chip will keep low level output.

When the system enters standby mode, the PMIC_SLEEP pin will output sleep indicating signal with high level, and then PMIC will enter sleep status controlled by the signal. According to the configuration of software dts file, some power supply will turn off, and some power supply will lower down the voltage.

When the system is resumed from standby mode, the PMIC_SLEEP pin will output low level at the first time, and the PMIC and all the power supply will be back to normal work state.

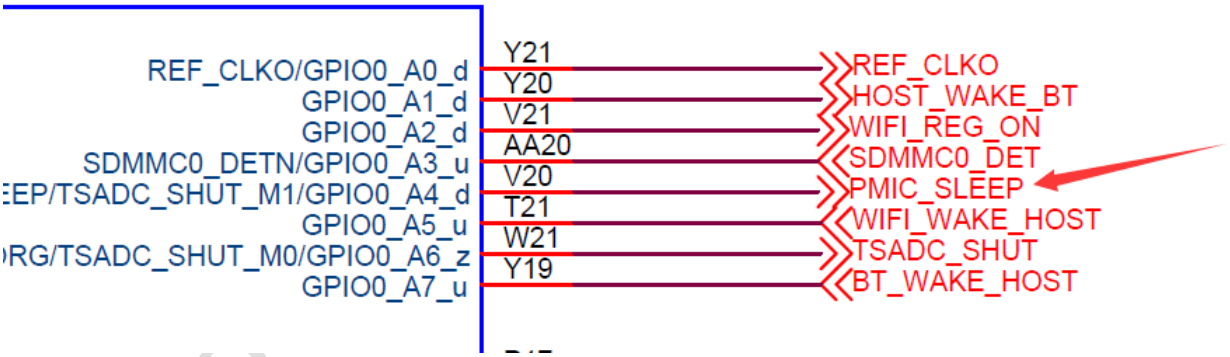


Figure 2-28 RK3326 PMIC_SLEEP Output

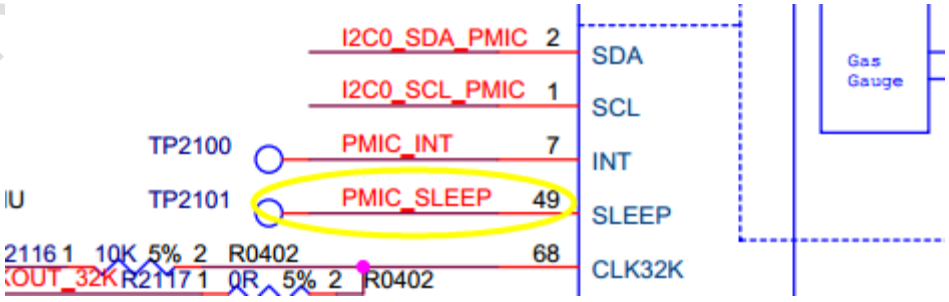


Figure 2-29 RK817-1 PMIC_SLEEP Input

2.2.6 Power Peak Current

Below table shows the peak current test result of the running mode for RK3326 tablet, only for reference. The test conditions are as below:

- APK Version: antutu v6.3.3
- CPU maximum frequency: 1.512GHz.
- GPU maximum frequency: 550MHz.
- DDR maximum frequency: 1x32bit LPDDR3 K4E6E304EB-EGCF, 800MHz.
- Oscilloscope enables the 20MHz bandwidth limitation.

Table 2-9 RK3326 Peak Current Table

PowerName	Voltage（V）	Peak Current(mA)
VCC_SYS	3.65V	1250.0
VDD_ARM	1.32V	1150.0
VDD_LOG	1.12V	1030.0
VCC_DDR	1.23V	280.0
VCC_3V0	2.94V	260.0
VCC_1V0	1.0V	5.1
VCC_1V8	1.81V	189.3
VDD_1V0	1.0V	7.8
VCC3V0_PMU	3.0V	3.7
VCCIO_SD	3.0V	3.4
VCC_SD	3.0V	TBD(depend on the type of memory card)

2.3 Function Interface Circuit Design Guide

2.3.1 Memory Card Circuit

RK3326 provides a SDMMC interface controller which can support SD v3.0 and MMC v4.51 protocol, as shown below:

- SDMMC controller has an independent power domain.
- SDMMC multiplexed with the functions such as UART2, JTAG etc., select function through SDMMC0_DET. For details please refer to section 2.1.4.
- VCCIO2 is IO supply, need to externally provide 3.3V power supply (SD 2.0 mode) or 3.3V/1.8V adjustable power supply (SD 3.0 mode).

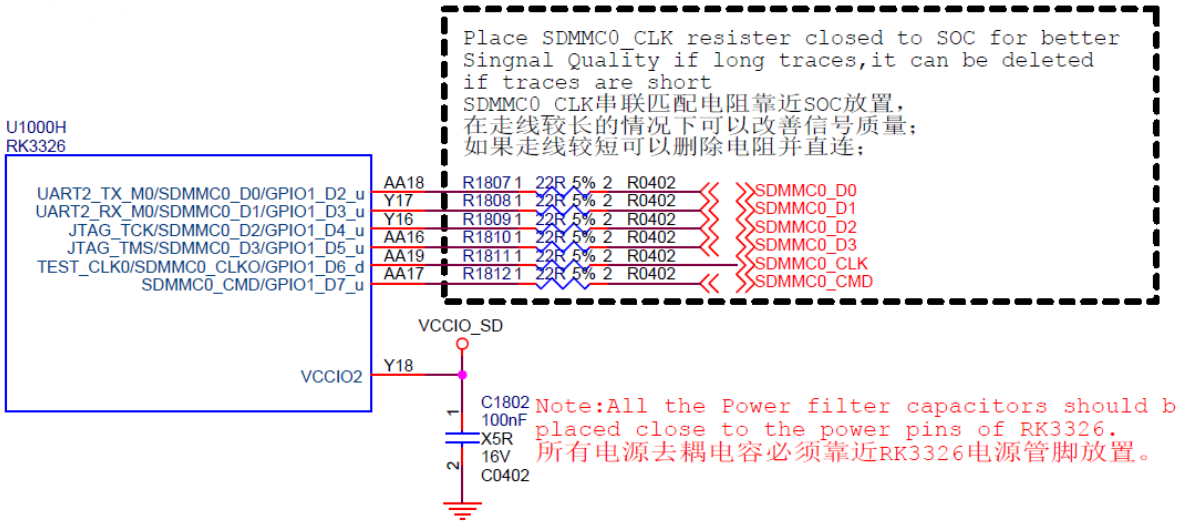


Figure 2-30 RK3326 SDMMC Part

The pull-up/down and matching design of the SDMMC interface are recommended as Table 2-10.

Table 2-10 RK3326 SDMMC Interface Design

Signal	Internal pull up/down	Connection method (SDR104 high-speed mode)	Description(chip side)
SDMMC_DQ[3:0]	Pull up	Series connect 22ohm resistor can be deleted if the trace is short	SD data output/input
SDMMC_CLK	Pull down	Series connect 22ohm resistor	SD clock output
SDMMC_CMD	Pull up	Series connect 22ohm resistor can be deleted if the trace is short	SD command output/input

2.3.2 USB Circuit

RK3326 has one USB 2.0 interface and supports OTG mode.

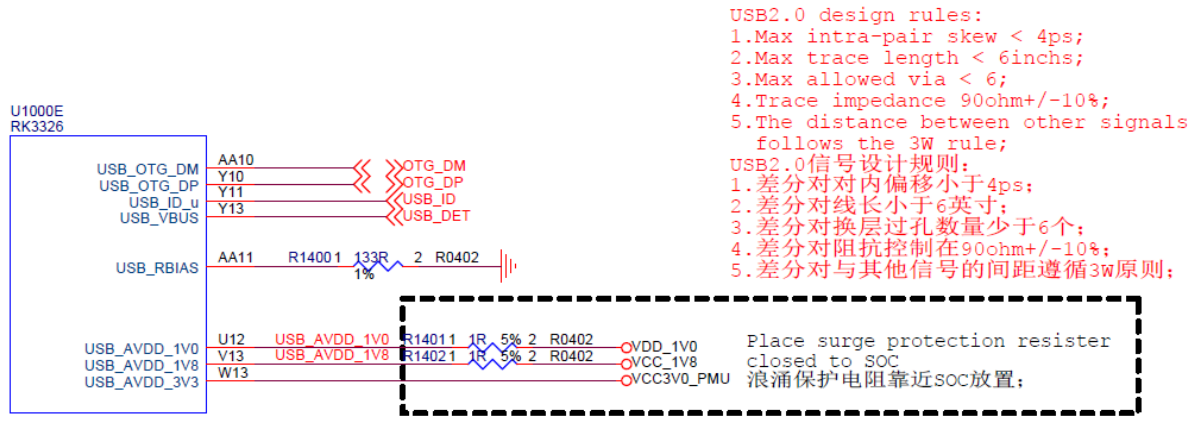


Figure 2-31 RK3326 USB Part

Please note for design:

- USB interface is default used as system firmware download port which must be reserved for debugging.

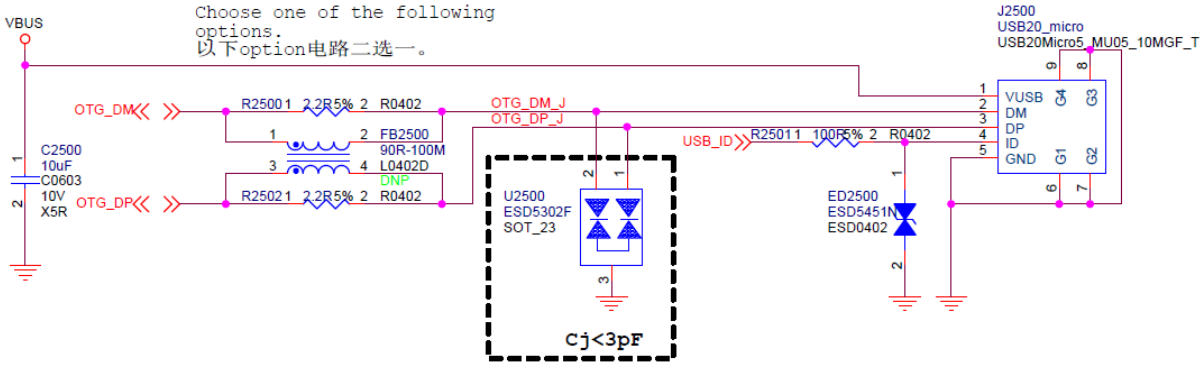


Figure 2-32 RK3326 USB Port

- USB_ID has an internal 200K pull up resistor, pull up to USB_AVDD_1V8, so OTG is default used as Device mode.
- USB_VBUS (USB_DET) is used as USB insertion detection, and it means there is USB inserted when detecting high level.

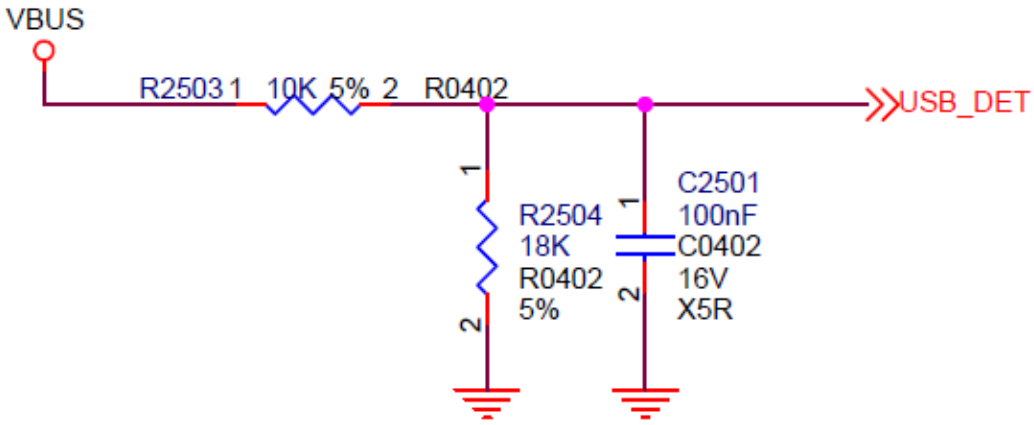


Figure 2-33 RK3326 USB Insertion Detection

- USB controller configuration reference resistor R1400 should select the resistor with 1% accuracy, because it will affect the USB amplitude and influence the quality of eye diagram.

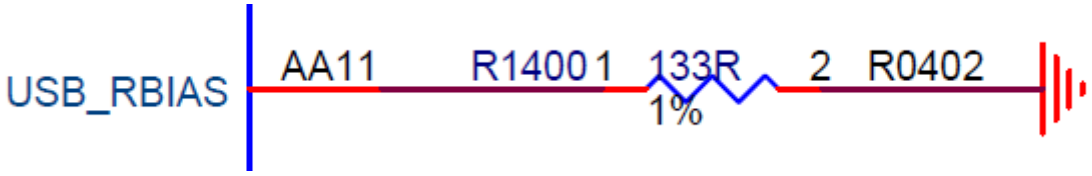


Figure 2-34 RK3326 USB Controller Reference Resistance

- The 1.0V/1.8V power supply of controller needs to series connect 1ohm resistor to avoid the damage caused by surge.

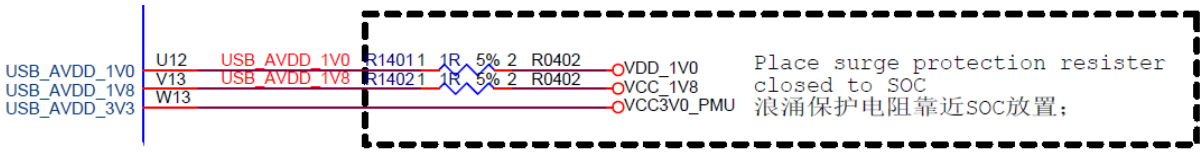


Figure 2-35 RK3326 USB Controller Power Anti-surge

- In order to improve USB performance, the decoupling capacitor of the controller power should be placed close to the pin.
- In order to suppress EMI, Common mode choke can be reserved in signal line and select to use resistor or common mode choke according to the actual situation during debugging.

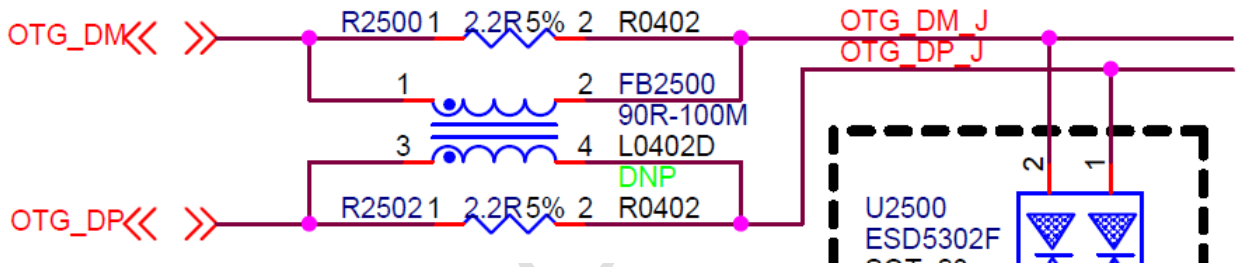


Figure 2-36 RK3326 USB Reserved Common Mode Choke

USB2.0 interface pull up/down and matching design are recommended as below Table:

Table 2-11 RK3326 USB Interface Design

Signal	Connection method	Description
USB_OTG_DP/DM	Series connect 2.2ohm resistor	USB OTG input/output
USB_ID	Direct connect(with internal 1.8V pull up)	USB OTG ID recognition, need to use for Micro-B interface
USB_VBUS	Resistor voltage divider detection	USB OTG insertion detection
USB_RBIAS		USB PHY configuration reference resistor, 133ohm connected to GND

2.3.3 Audio Circuit

RK3326 provides three groups of standard I2S interface, all supporting master or slave mode, the highest sampling rate up to 192 kHz, and bit rate from 16 bits to 32 bits.

- **2.3.3.1 I2S0**

  I2S0 interface contains independent 8 channels output and 8 channels input. In order

to meet the asynchronous sampling rate requirement of audio recording and playing, it provides two groups of bit clock and frame clock (SCLKTX\LRCKTX, SCLKRX\LRCKRX) accordingly. Need to pay attention to that, if SDOx and SDIx only refer to one group of bit/frame clock, prefer to use SCLKTX\LRCKTX as their common clock.

Need to pay attention to that, the I2S interface belongs to VCCIO4 power domain, and it is set to supply power for VCC_1V8 by default. If I2S peripheral IO level is 3.3V, need to adjust the power supply, and match with the relative IO level of the power domain.

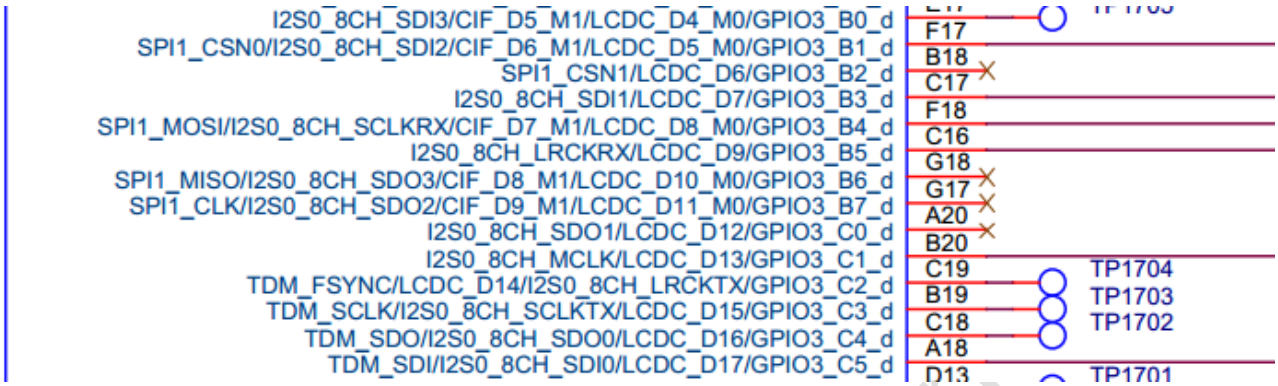


Figure 2-37 RK3326 I2S0 Part

I2S0 interface pull up/down and matching design are recommended as Table 2-12.

Table 2-12 RK3326 I2S0 Interface Design

Signal	Internal pull up/down	Connection method	Description(chip side)
I2S0_8CH_MCLK	Pull down	Series connect 22ohm resistor	I2S0 system clock output for slave
I2S0_8CH_SCLKTX	Pull down	Series connect 22ohm resistor	I2S0 continuous serial clock (TX, related with SDOx)
I2S0_8CH_LRCKTX	Pull down	Series connect 22ohm resistor	I2S0 L/R channel select clock, used for word select(TX, related with SDOx)
I2S0_8CH_SDO0	Pull down	Series connect 22ohm resistor	I2S0 serial data 0 output
I2S0_8CH_SDO1	Pull down	Series connect 22ohm resistor	I2S0 serial data 1 output
I2S0_8CH_SDO2	Pull down	Series connect 22ohm resistor	I2S0 serial data 2 output
I2S0_8CH_SDO3	Pull down	Series connect 22ohm resistor	I2S0 serial data 3 output
I2S0_8CH_SCLKRX	Pull down	Series connect 22ohm resistor	I2S0 continuous serial clock(RX, related with SDIx)
I2S0_8CH_LRCKRX	Pull down	Series connect 22ohm resistor	I2S0 L/R channel select clock, used for word select (RX, related with SDIx)

I2S0_8CH_SDI0	Pull down	Series connect 22ohm resistor	I2S0 serial data 0 input
I2S0_8CH_SDI1	Pull down	Series connect 22ohm resistor	I2S0 serial data 1 input
I2S0_8CH_SDI2	Pull down	Series connect 22ohm resistor	I2S0 serial data 2 input
I2S0_8CH_SDI3	Pull down	Series connect 22ohm resistor	I2S0 serial data 3 input

- **2.3.3.2 I2S1**

I2S1 supports 2 channels input and 2 channels output.

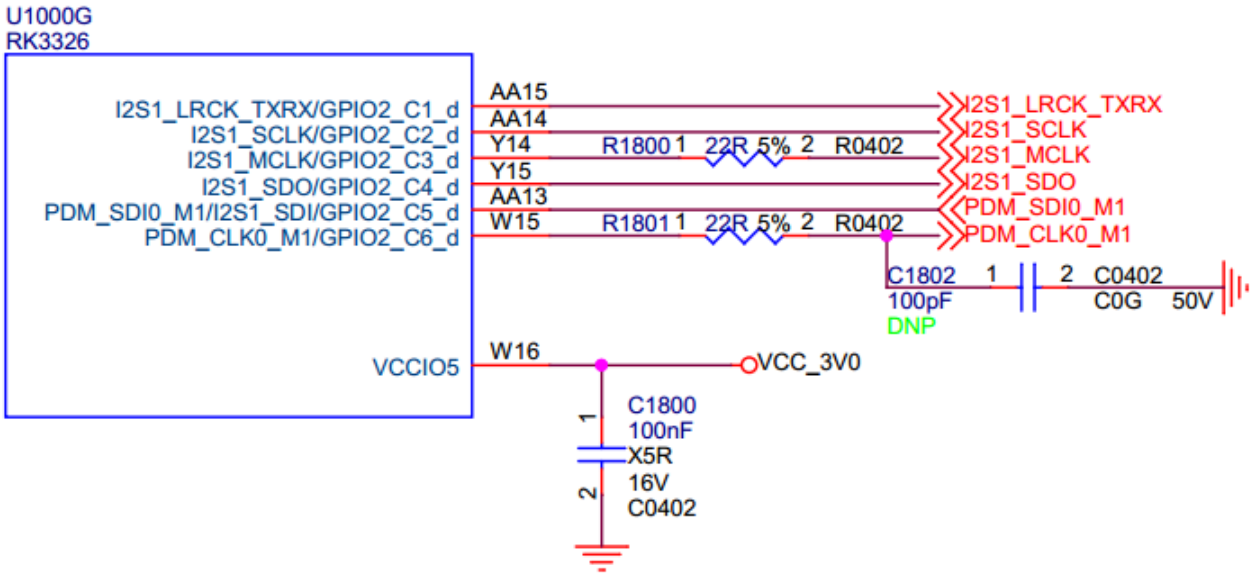


Figure 2-38 RK3326 I2S1 Part

I2S1 interface pull up/down and matching design are recommended as shown in Table 2-13.

Table 2-13 RK3326 I2S1 Interface Design

Signal	Internal pull up/down	Connection method	Description (chip side)
I2S1_MCLK	Pull down	Series connect 22ohm resistor	I2S1 system clock output for slave
I2S1_SCLK	Pull down	Series connect 22ohm resistor	I2S1 continuous serial clock
I2S1_LRCK_TXRX	Pull down	Series connect 22ohm resistor	I2S1 L/R channel select clock, used for word select
I2S1_SDO	Pull down	Series connect 22ohm resistor	I2S1 serial data 0 output
I2S1_SDI	Pull down	Series connect 22ohm resistor	I2S1 serial data 0 input

- **2.3.3.3 I2S2**

I2S2 supports 2 channels output and 2 channels input, used as PCM interface to connect BT module by default and used as the communication port for bluetooth call function under HFP protocol.

Need to pay attention to that, the I2S interface belongs to VCCIO4 power domain, when WIFI/BT module is in SDIO3.0 work mode, it is set to supply power for VCC_1V8. If the power supply of the power domain is set to 3.3V, PCM IO related level shift circuit need to be mounted to meet level matching.

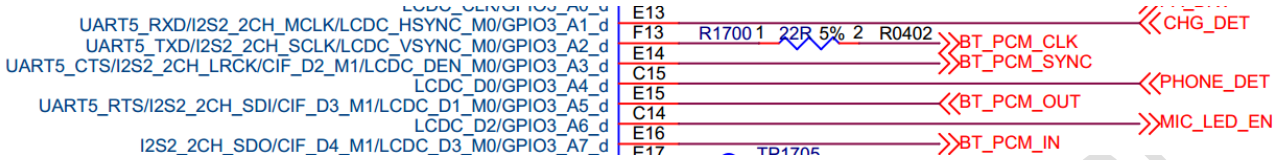


Figure 2-39 RK3326 I2S2 Part

I2S2 interface pull up/down and matching design are recommended as shown in Table 2-14.

Table 2-14 RK3326 I2S2 Interface Design

Signal	Internal pull up/down	Connection method	Description(chip side)
I2S2_2CH_MCLK	pull down	Series connect 22ohm resistor	I2S2 system clock output for slave
I2S2_2CH_SCLK PCM_CLK	pull down	Series connect 22ohm resistor	I2S2 continuous serial clock PCM clock
I2S2_2CH_LRCK PCM_SYNC	pull down	Series connect 22ohm resistor	I2S2 L/R channel select clock, used for word select PCM data frame sync
I2S2_2CH_SDO PCM_OUT	pull down	Series connect 22ohm resistor	I2S2 serial data output PCM data output
I2S2_2CH_SDI PCM_IN	pull down	Series connect 22ohm resistor	I2S2 serial data input PCM data input

RK3326 provides one group of PDM digital audio interface, supporting 8 channels PDM format audio input at most, the highest sampling rate up to 192 kHz, and bit rate from 16 bits to 32 bits.

In order to realize audio loop back input for RK809-1, the IO multiplexing here is relatively flexible, and need to avoid the reuse of the same signal in different locations.

When use PDM MIC for audio acquisition, also recommend to use PDM interface for loop back to simplify the software processing of audio recording data. In this way, for the commonly involved cases of 2-6 PDM MIC recording and 1-2 loop back channels, the input can be completed only by a complete 4-8 channel recording audio, and no additional splicing processing is required by the software.

If the 8-channel PDM MIC input needs to be connected, the I2S interface can only be used as the capture of the loop back channel, and software needs to do additional audio splicing processing to meet the data synchronization requirements of the algorithm.

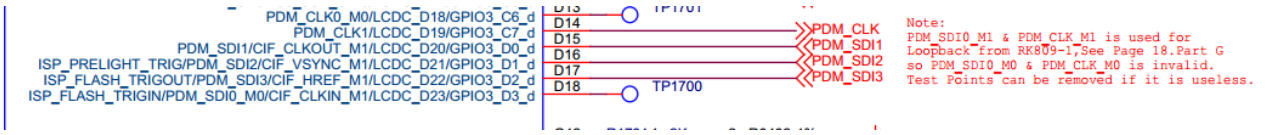


Figure 2-40 RK3326 PDM Part IOMux0

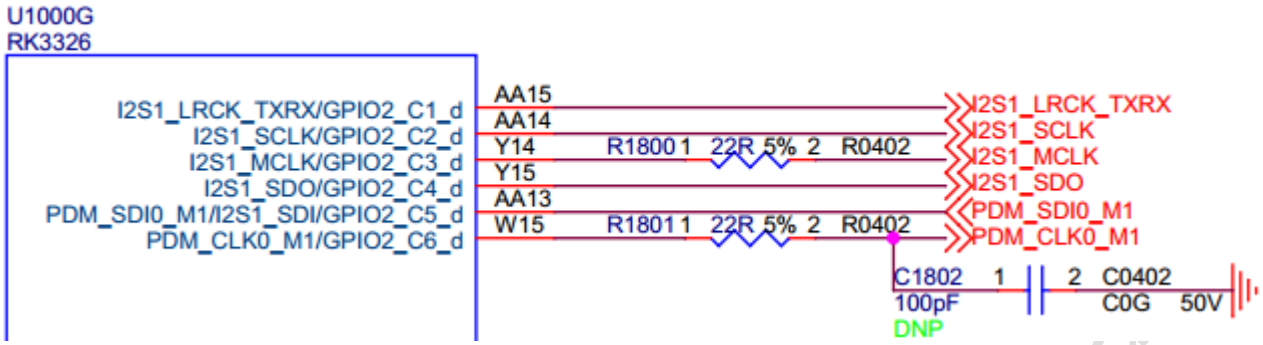


Figure 2-41 RK3326 PDM Part IOMux1

Table 2-15 RK3326 PDM Interface Design

Signal	Internal pull up/down	Connection method	Description(chip side)
PDM_CLK0_M0	pull down	Series connect 22ohm resistor	PDM clock 0, IOMUX 0, default not used
PDM_CLK0_M1	pull down	Series connect 22ohm resistor	PDM clock 0, IOMUX 0, default connect to RK809-1 and used for audio loop back
PDM_CLK1	pull down	Series connect 22ohm resistor	PDM clock 1, same source with PDM clock 0, used to drive PDM MIC by default
PDM_SDI0_M0	pull down	Series connect 22ohm resistor	PDM data 0 input, IOMUX 0, default not used
PDM_SDI0_M1	pull down	Series connect 22ohm resistor	PDM data 0 input, IOMUX 1, default connect to RK809-1 and used for audio loop back
PDM_SDI1	pull down	Series connect 22ohm resistor	PDM data 1 input
PDM_SDI2	pull down	Series connect 22ohm resistor	PDM data 2 input
PDM_SDI3	pull down	Series connect 22ohm resistor	PDM data 3 input

RK3326 provides one group of TDM digital audio interface, supporting master or slave mode, up to 8-channel TDM format audio output and 8-channel TDM format audio input, the highest sampling rate up to 192 kHz, and bit rate from 16 bits to 32 bits.

Figure 2-42 RK3326 TDM Interface

Table 2-16 RK3326 TDM Interface Design

Signal	Internal pull up/down	Connection method	Description(chip side)
TDM_SCLK	pull down	Series connect 22ohm resistor	TDM continuous serial clock
TDM_FSYNC	pull down	Series connect 22ohm resistor	TDM L/R channel select clock, used for word select
TDM_SDO	pull down	Series connect 22ohm resistor	TDM serial data output
TDM_SDI	pull down	Series connect 22ohm resistor	TDM serial data input

- **2.3.3.4 Codec**

RK817-1/RK809-1 has embedded Codec, connecting with RK3326 through I2S interface.

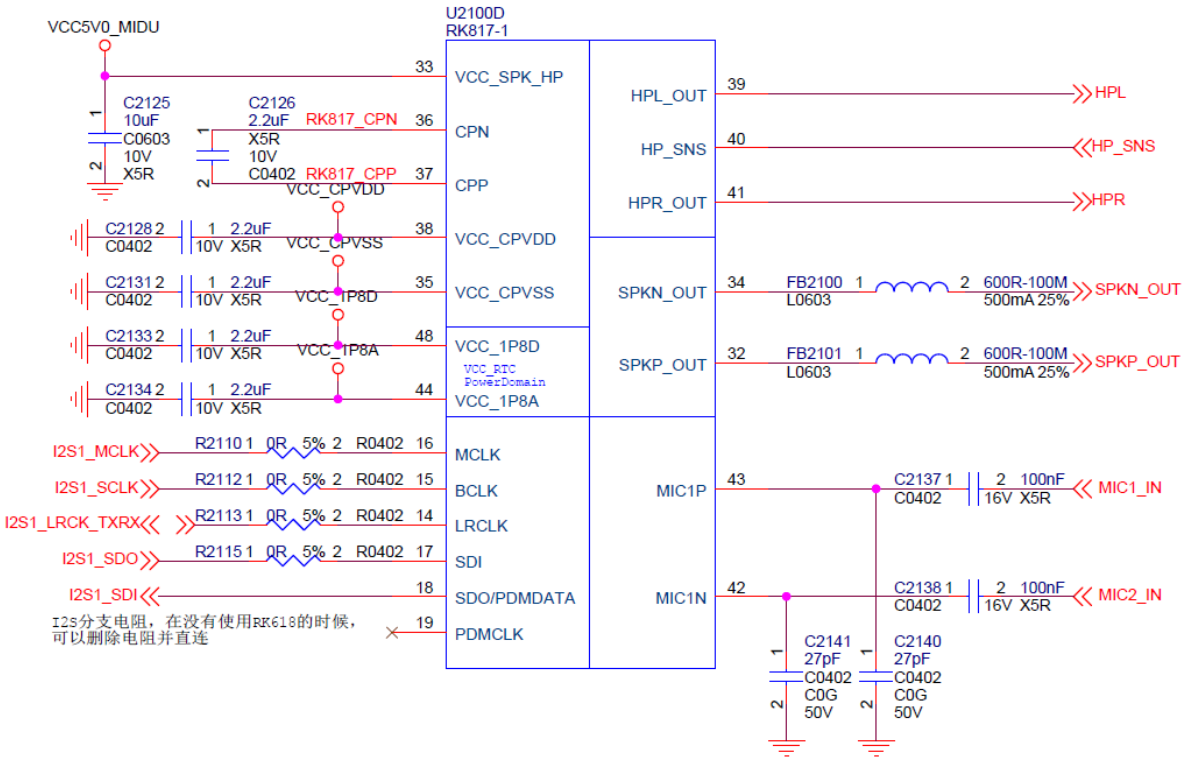


Figure 2-43 RK817-1 Codec Circuit

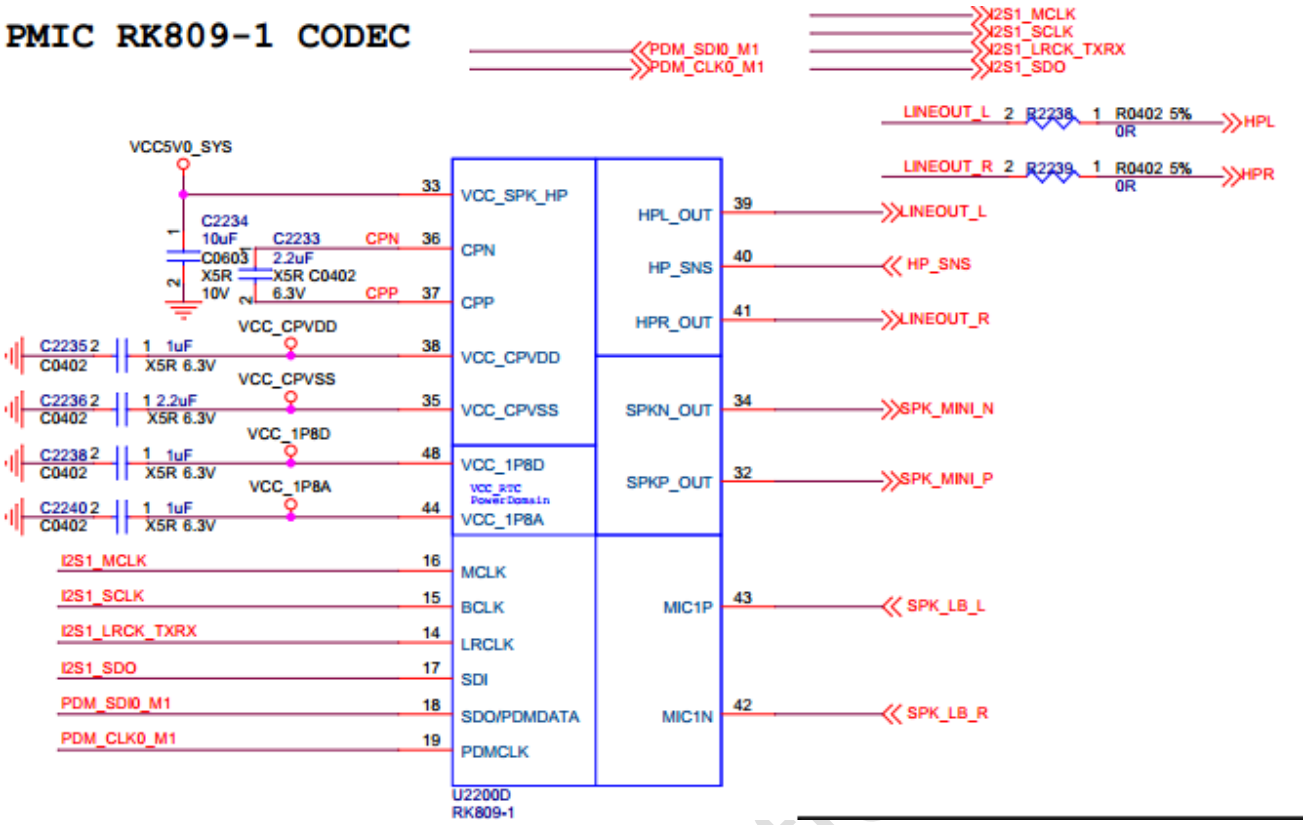


Figure 2-44 RK809-1 Codec Circuit

The HPSNS output from Codec is used as an internal Offset reference and needs to be connected to GND, which is connected with GND at the headset to reduce the level difference with the headphone GND. The traces should be accompanied in the middle of HPR/HPL to avoid the interference from other signals. If the Codec's GND is on the same complete GND plane as the headset GND, and the components layout is close, it can be connected directly to the GND plane.

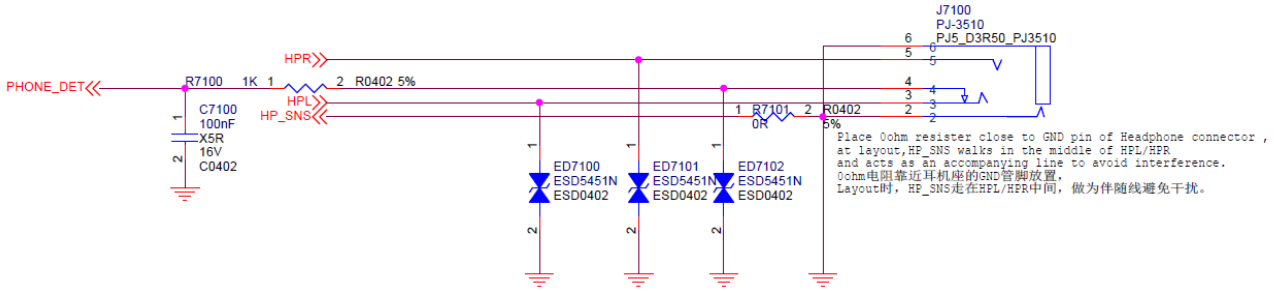


Figure 2-45 RK3326 Headphone Circuit

Codec embedded Mono filter free speaker drive circuit can provide the drive strength of 1.3W@8ohm, which can meet the requirement of mono channel application with small power and can save the additional cost of external power amplifier.

When use the embedded power amplifier to do the mic array loop back, the recommended loop back circuit is as below, after voltage division and filter, output differential loop back signal to the audio ADC interface of RK809-1, complete A/D conversion by RK809-1 and then transmit back to RK3326 through PDM/I2S interface.

Here RK809-1 is set as PDM interface to communicate with RK3326 by default, which is based on the consideration of using PDM MIC as described in PDM interface section.

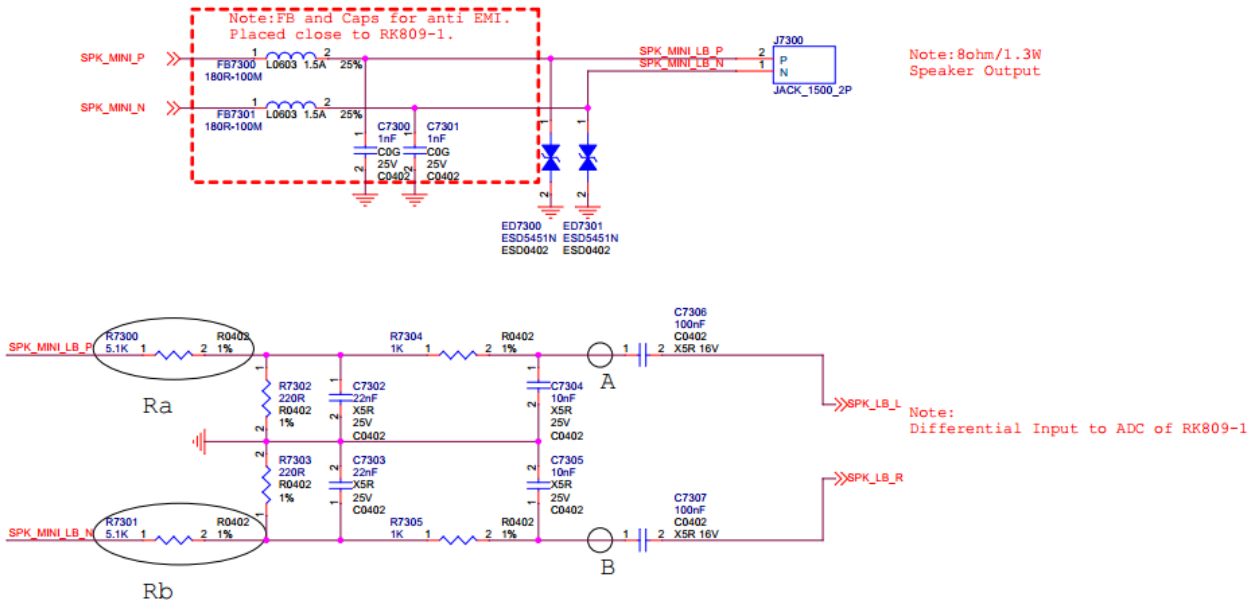


Figure 2-46 RK3326 Speaker Circuit

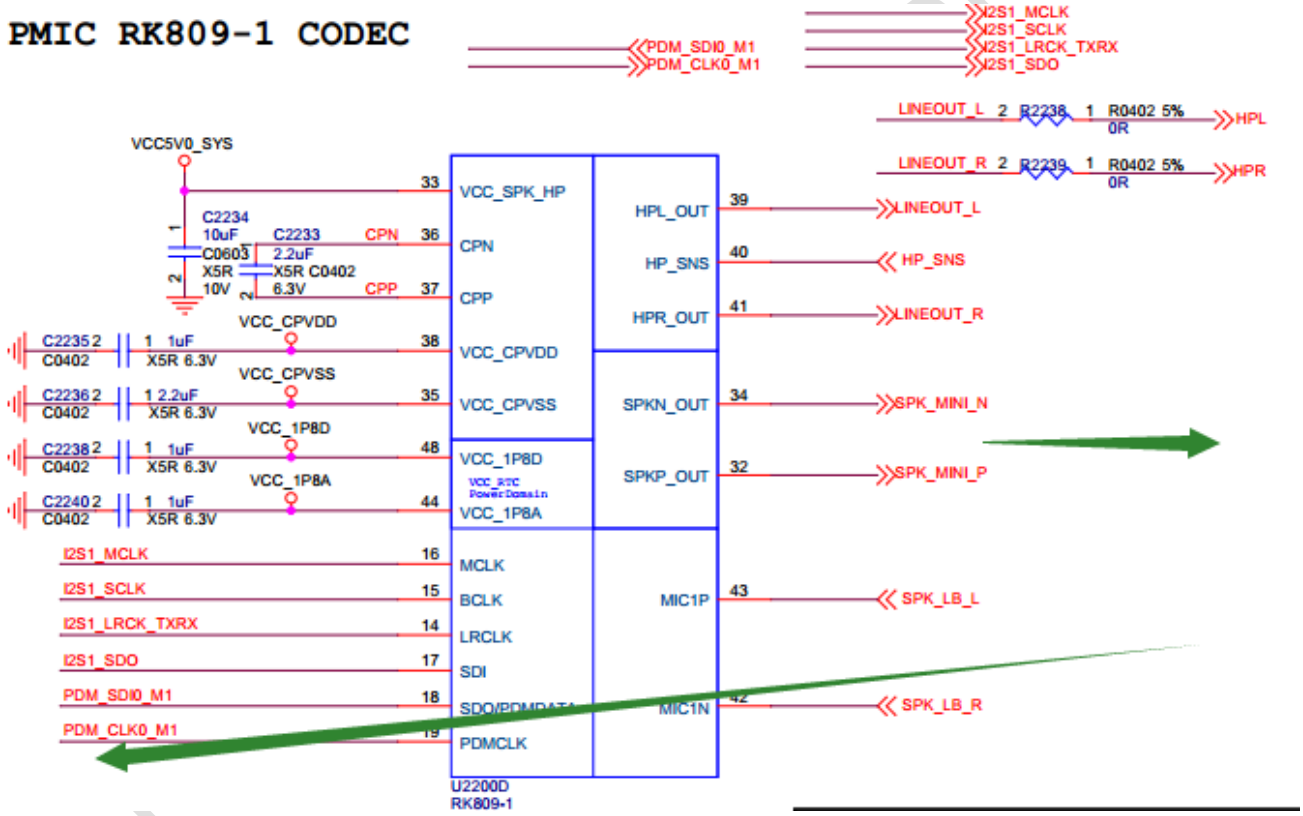


Figure 2-47 RK3326 Look Back Path

If the embedded Mono speaker drive circuit of Codec cannot meet the drive strength requirement, external separate analog/digital power amplifier can be connected, and the loop back also can refer to the above circuit. Need to pay attention to that Ra\Rb resistance should be adjusted according to the output level of the separate power amplifier, to make the max level measured at A/B points is not bigger than the input limit value of ADC, which is recommended to be less than 500mV based on debugging status.

For Stereo requirement, ADC of RK809-1 should be configured as two channels of single-end input to meet the requirement of two channels of loop back. In order to be compatible with different types of power amplifier, the loop back collection point is placed at LINEOUT side. Adjust according to the requirement of algorithm or use external ADC to do the loop back collection.

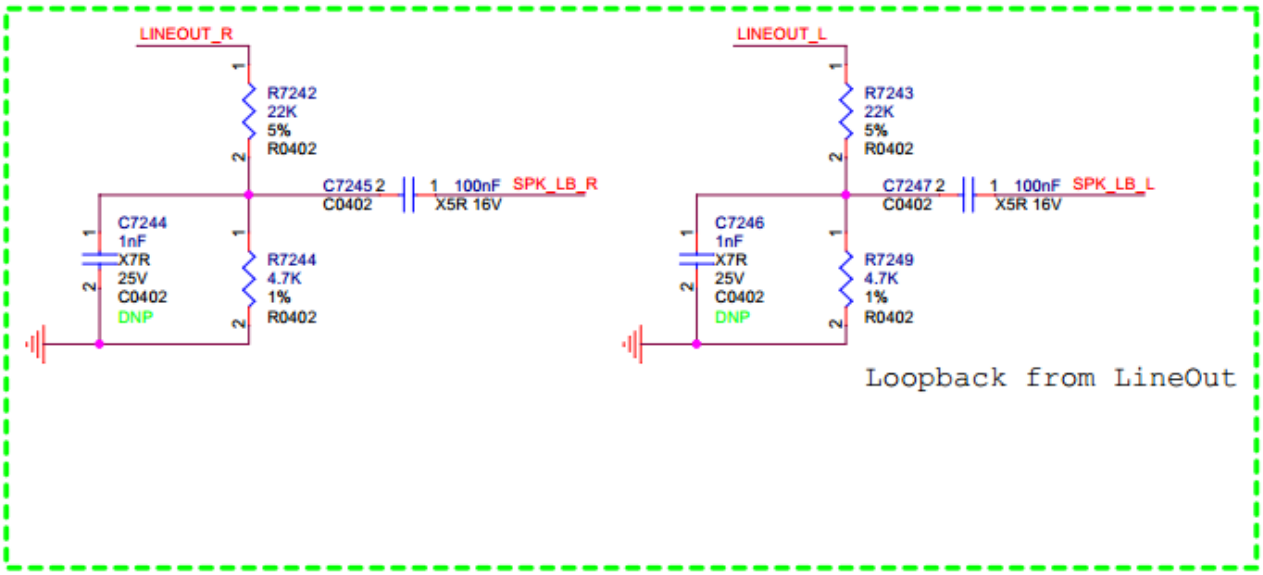


Figure 2-48 RK3326 Stereo Loop Back

- **2.3.3.5 MIC**

MIC circuit is shown as Figure 2-45. Select appropriate voltage divider R7105 and R7106 according to the electret microphone specifications.

If use analog interface MEMS MIC, please refer to the recommended design circuit.

If use digital interface MEMS MIC, it can be directly connected to I2S0 of RK3326 as Figure 3-65.

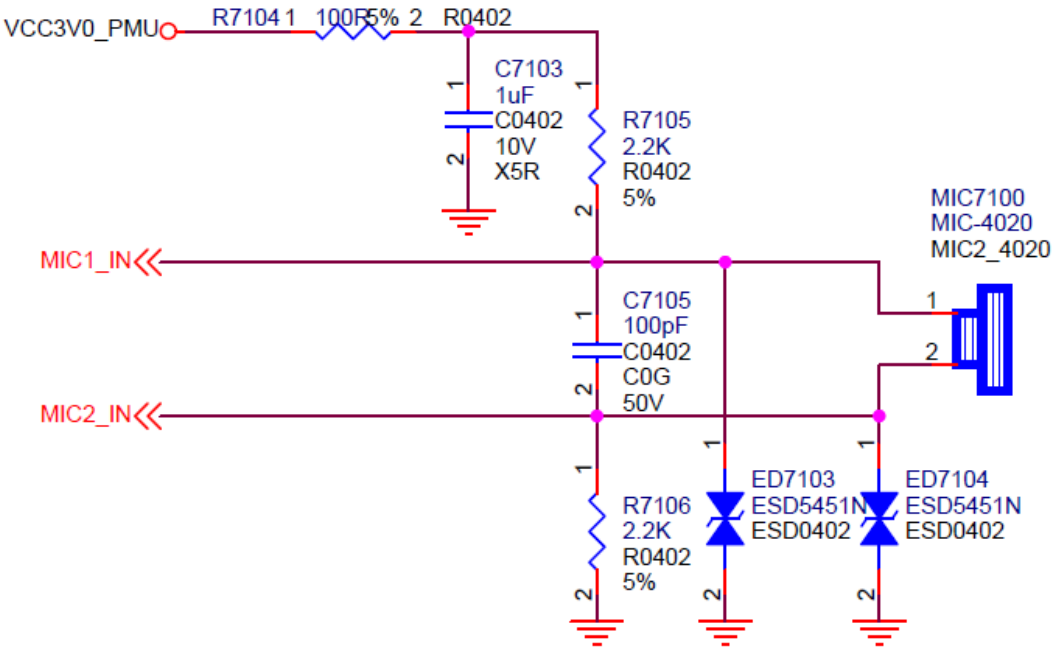


Figure 2-49 Differential MIC Circuit

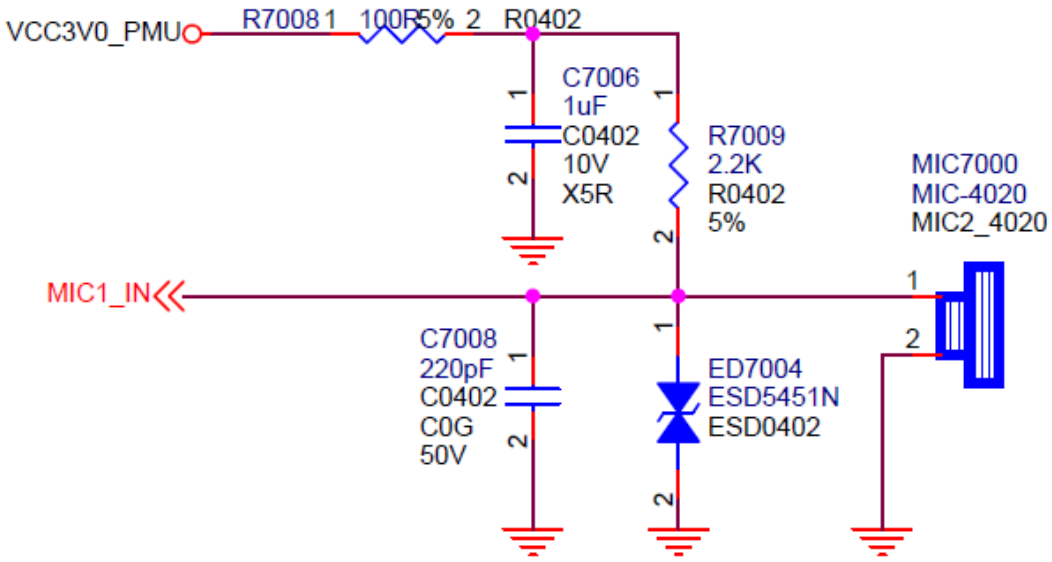


Figure 2-50 Single-end MIC Circuit

- **2.3.3.6 MIC for AI-VA**

Considering the main stream cases and cost, AI-VA provides two kinds of microphone reference circuit: PDM MIC solution and analog MIC solution of ADC input. For more details please refer to RK3326_AI_VA_MIC_REF_V11_20180718. Besides, it also provides the reference design of RGB LED drive circuit and ADC button circuit. The block diagram is shown as below:

PDM MIC Block Diagram

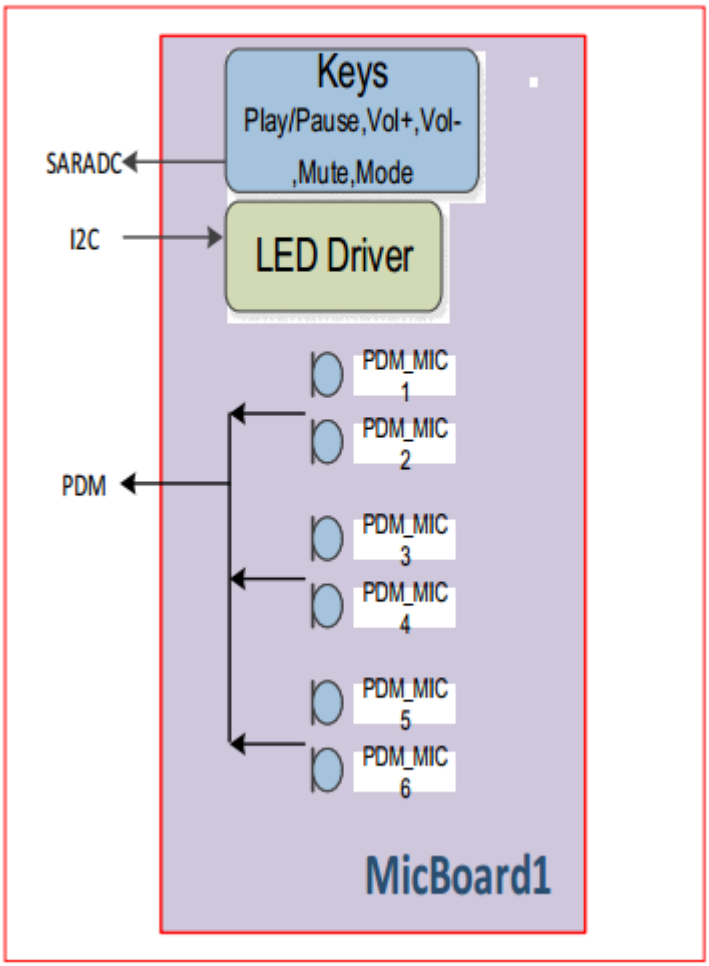


Figure 2-51 RK3326 PDM MIC Solution Block Diagram

Analog MIC Block Diagram
I2S Interface

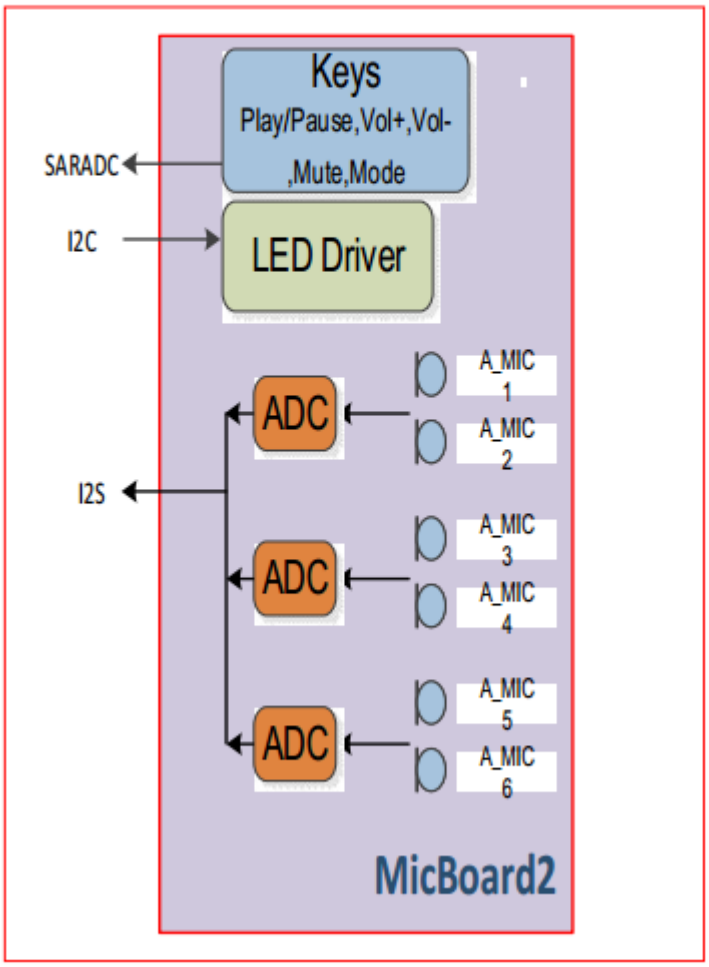


Figure 2-52 RK3326 Analog MIC Solution Block Diagram

The circuit of PDM MIC solution is very simple. The communication can be completed only by using one CLK to output drive MIC and one DATA to input data. The circuit is as below. PDM interface can connect two microphones, share clock and data bus, and respectively output data along two edges of CLK. For layout need to pay attention to the corresponding relationship between LR configuration and MIC channel to avoid the violation from the definition. RK3326 PDM register has polarity configuration bit, and LR polarity can be inverted.

PDM MIC drives more MIC. The trace uses Daisy Chain topological connection to shorten the branch of each node as possible and both sides of the signal are surrounded by GND.

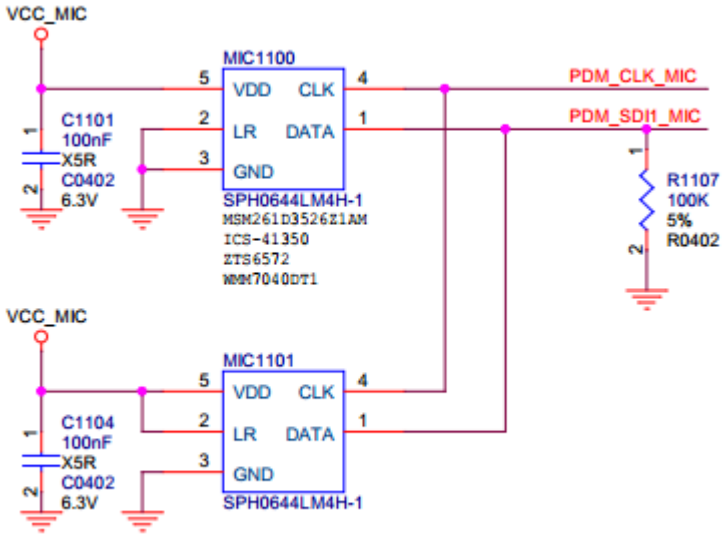


Figure 2-53 RK3326 PDM MIC Circuit

MIC of AI-VA products is usually placed on an independent MIC board, which is exposed below the sound inlet hole of the cover. Therefore, need to add electrostatic protective measures as close as possible to MIC, such as placing ESD protective component, series connect resistor, and so on.

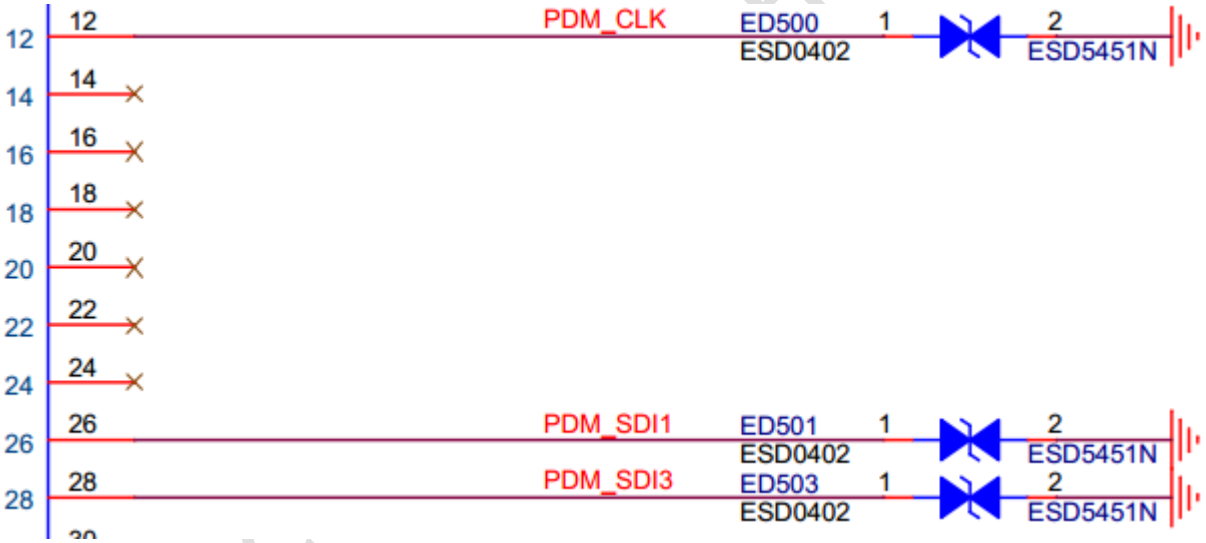


Figure 2-54 RK3326 PDM ESD

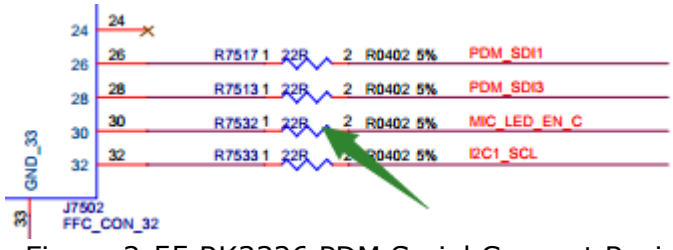


Figure 2-55 RK3326 PDM Serial Connect Resistor

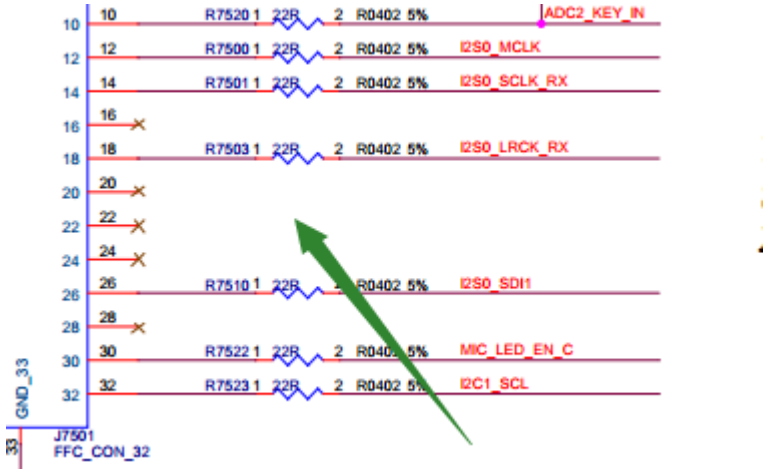


Figure 2-56 RK3326 I2S Serial Connect Resistor

For the analog MIC solution input by ADC, need to place ADC close to the analog MIC and convert the analog signal into digital signal as soon as possible for transmission to improve the anti interference ability of the whole input path.

In multi-mic application, may connect multiple external ADC at the same time, need to note that the trace of I2S CLK should use Daisy Chain topology connection, shorten the branch of each node as much as possible, and both sides of the signal (especially CLK) should be surrounded by GND while routing and layout.

For the electrostatic protection of analog MIC, it is also useful to place ESD component close to MIC or series connect resistance with signal line.

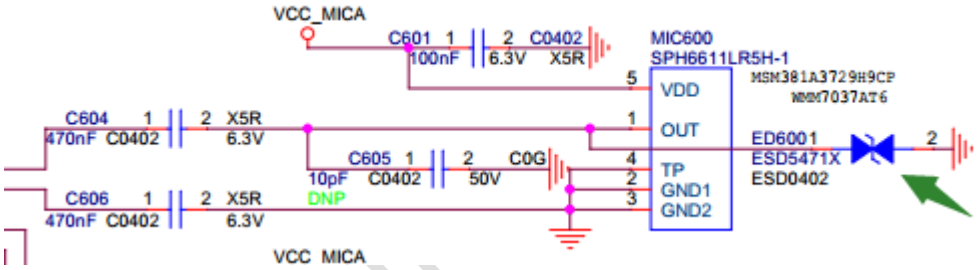


Figure 2-57 RK3326 Analog MIC Circuit

2.3.4 Video Circuit

RK3326 has embedded video controller, supporting RGB/LVDS/MIPI DSI three kinds of video output modes.

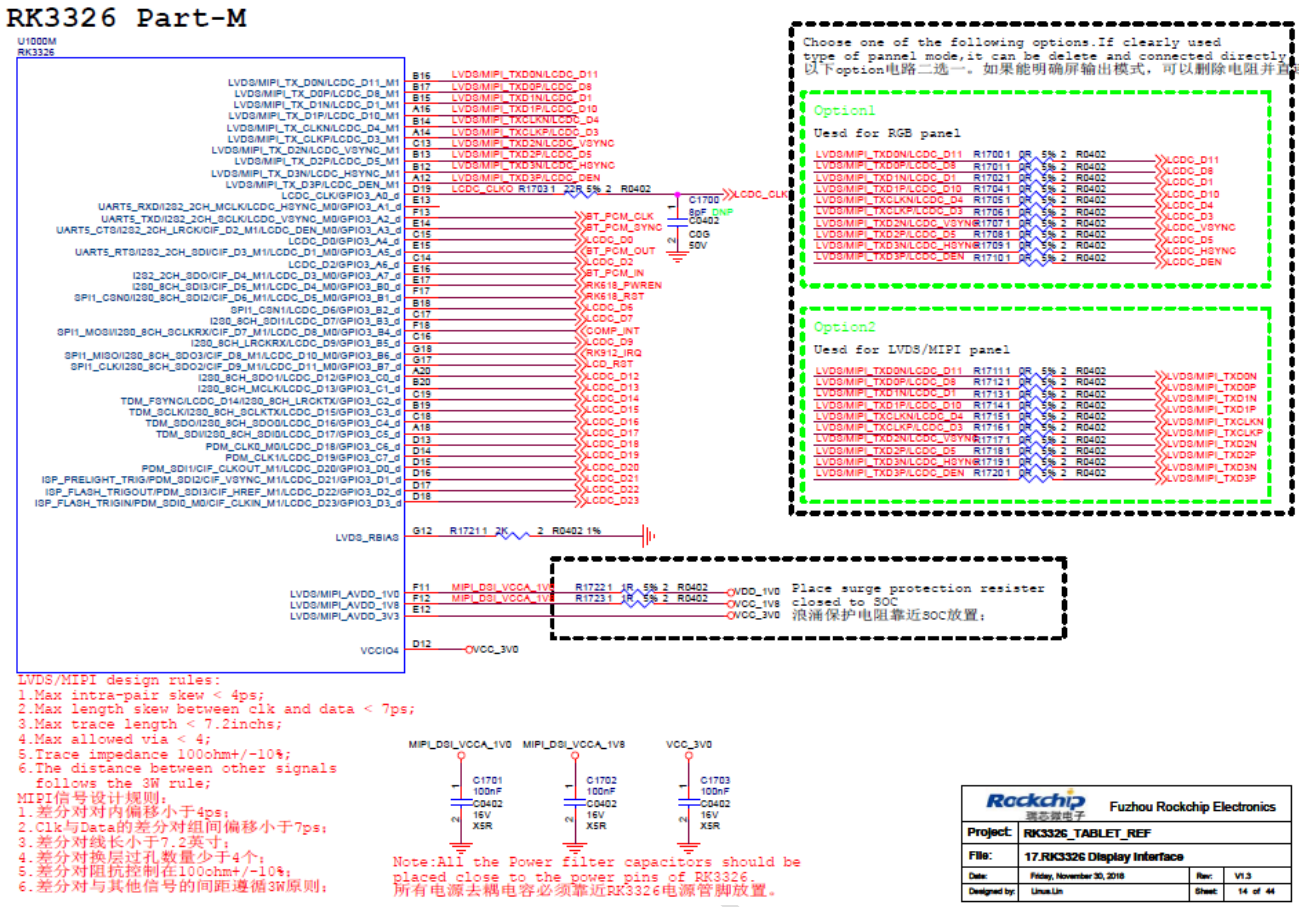


Figure 2-58 RK3326 Video Part

- **2.3.4.1 LVDS/MIPI-DSI Mode**

LVDS/MIPI-DSI uses the same one controller and some pins are multiplexed with RGB. Need to configure the corresponding output mode through software when use LVDS/MIPI-DSI to output.

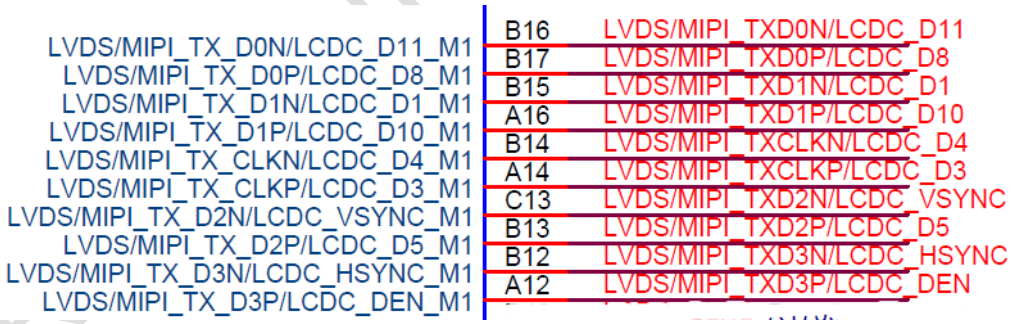


Figure 2-59 RK3326 LVDS/MIPI-DSI Part

Please note for design:

- The reference resistor of LVDS controller should select the resistor with 1% accuracy, and it will affect the signal quality of eye diagram. The resistor is not needed for MIPI/RGB mode.

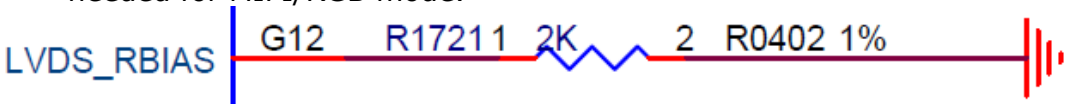


Figure 2-60 RK3326 LVDS Controller Reference Resistor

- In order to avoid the damage of surge, 1.0V/1.8V power supply of LVDS/MIPI-DSI controller needs to series connect 1ohm resistor.

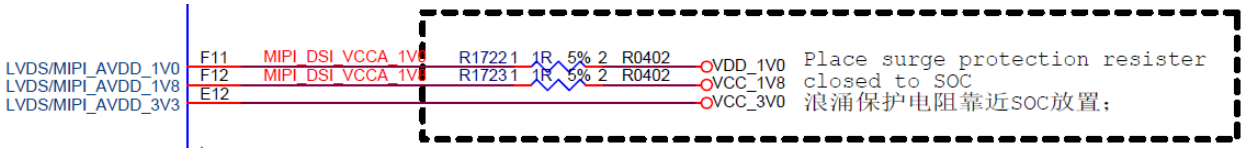


Figure 2-61 RK3326 LVDS/MIPI-DSI Part Power Anti-surge

- In order to improve LVDS/MIPI-DSI performance, the decoupling capacitor of the controller power should be placed close to the pin.

2.3.4.2 RGB Mode

RK3326 supports 24bit RGB output. Need to configure the output mode through software when use RGB output mode.

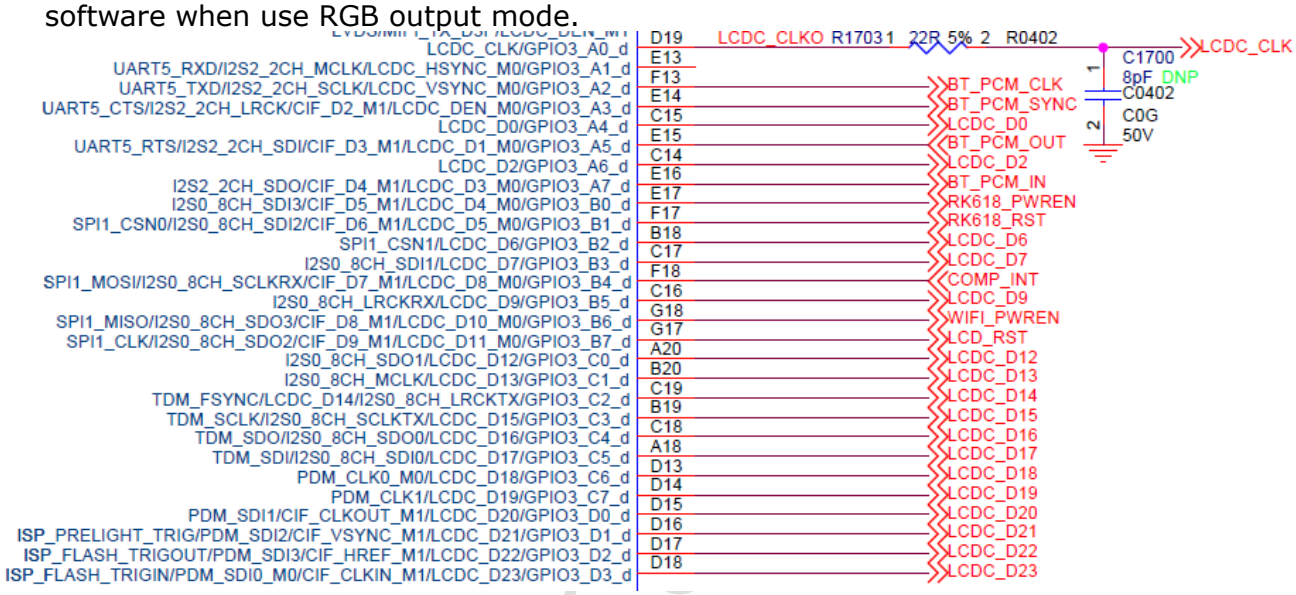


Figure 2-62 RK3326 RGB Part

- When use RGB888 24bit panel, the corresponding relationship of the signal is as below:

Correspondence between LCDC DATA and RGB			
LCDC_D0	B0	LCDC_D12	G4
LCDC_D1	B1	LCDC_D13	G5
LCDC_D2	B2	LCDC_D14	G6
LCDC_D3	B3	LCDC_D15	G7
LCDC_D4	B4	LCDC_D16	R0
LCDC_D5	B5	LCDC_D17	R1
LCDC_D6	B6	LCDC_D18	R2
LCDC_D7	B7	LCDC_D19	R3
LCDC_D8	G0	LCDC_D20	R4
LCDC_D9	G1	LCDC_D21	R5
LCDC_D10	G2	LCDC_D22	R6
LCDC_D11	G3	LCDC_D23	R7

Figure 2-63 RK3326 RGB 24bit Connection

- When use RGB666 18bit panel, only need to connect LCDC_D0-D17 data signal, and the corresponding relationship is as below:

Correspondence between LCDC DATA and RGB			
LCDC_D0	B2	LCDC_D9	G5
LCDC_D1	B3	LCDC_D10	G6
LCDC_D2	B4	LCDC_D11	G7
LCDC_D3	B5	LCDC_D12	R2
LCDC_D4	B6	LCDC_D13	R3
LCDC_D5	B7	LCDC_D14	R4
LCDC_D6	G2	LCDC_D15	R5
LCDC_D7	G3	LCDC_D16	R6
LCDC_D8	G4	LCDC_D17	R7

Figure 2-64 RK3326 RGB 18bit Connection

- The 10 signals including LCDC_D5/D8/D10 etc. have M0 and M1 two multiplexing relationship which can be configured freely. But in real product design, recommend to use the pin of M1. Because seen from the fan out figure of the chip, these pins are on the edge of the chip which is easy for routing no matter for two-layer or four-layer board.

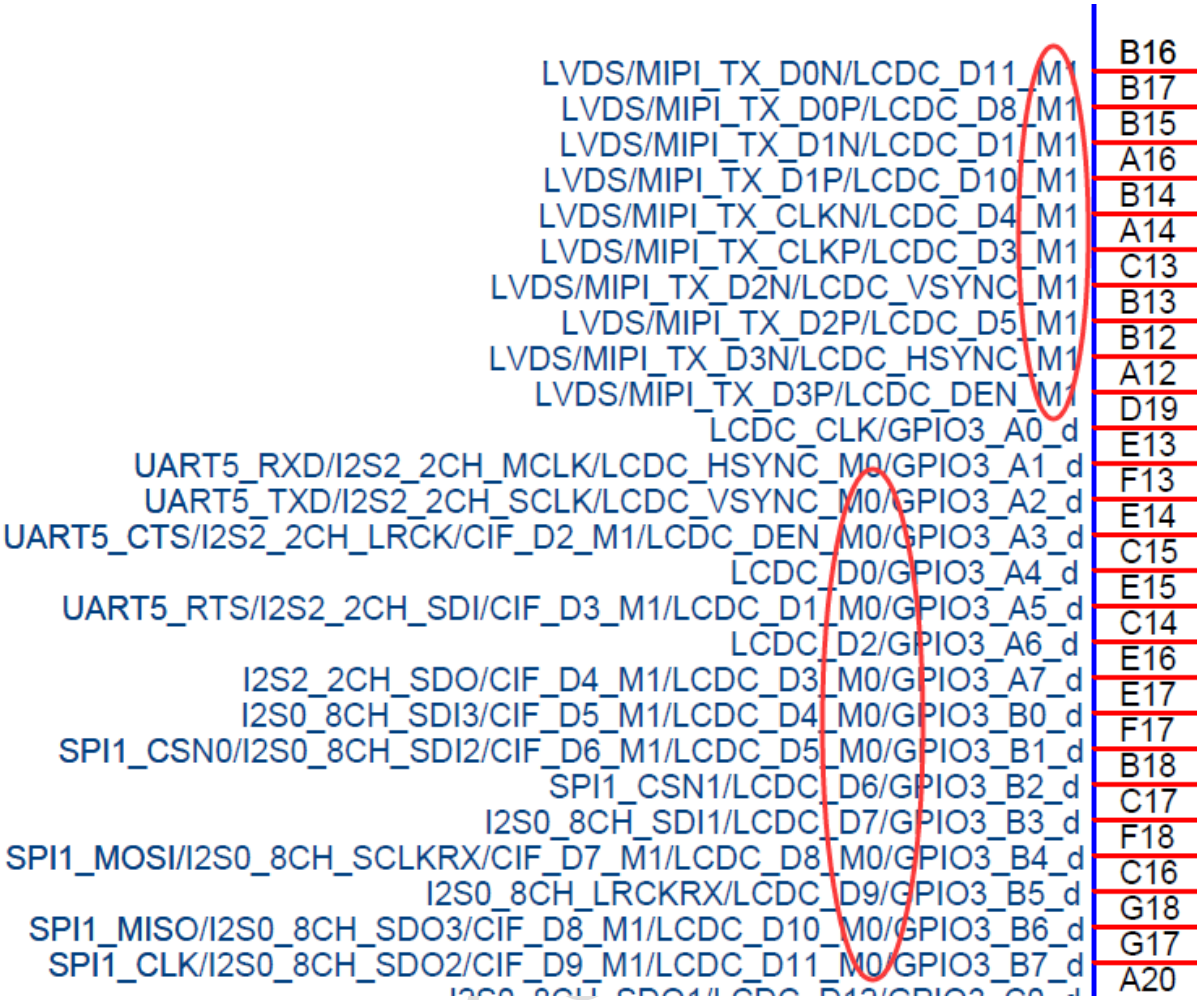


Figure 2-65 RK3326 LCDC M0&M1 Multiplexed Pin

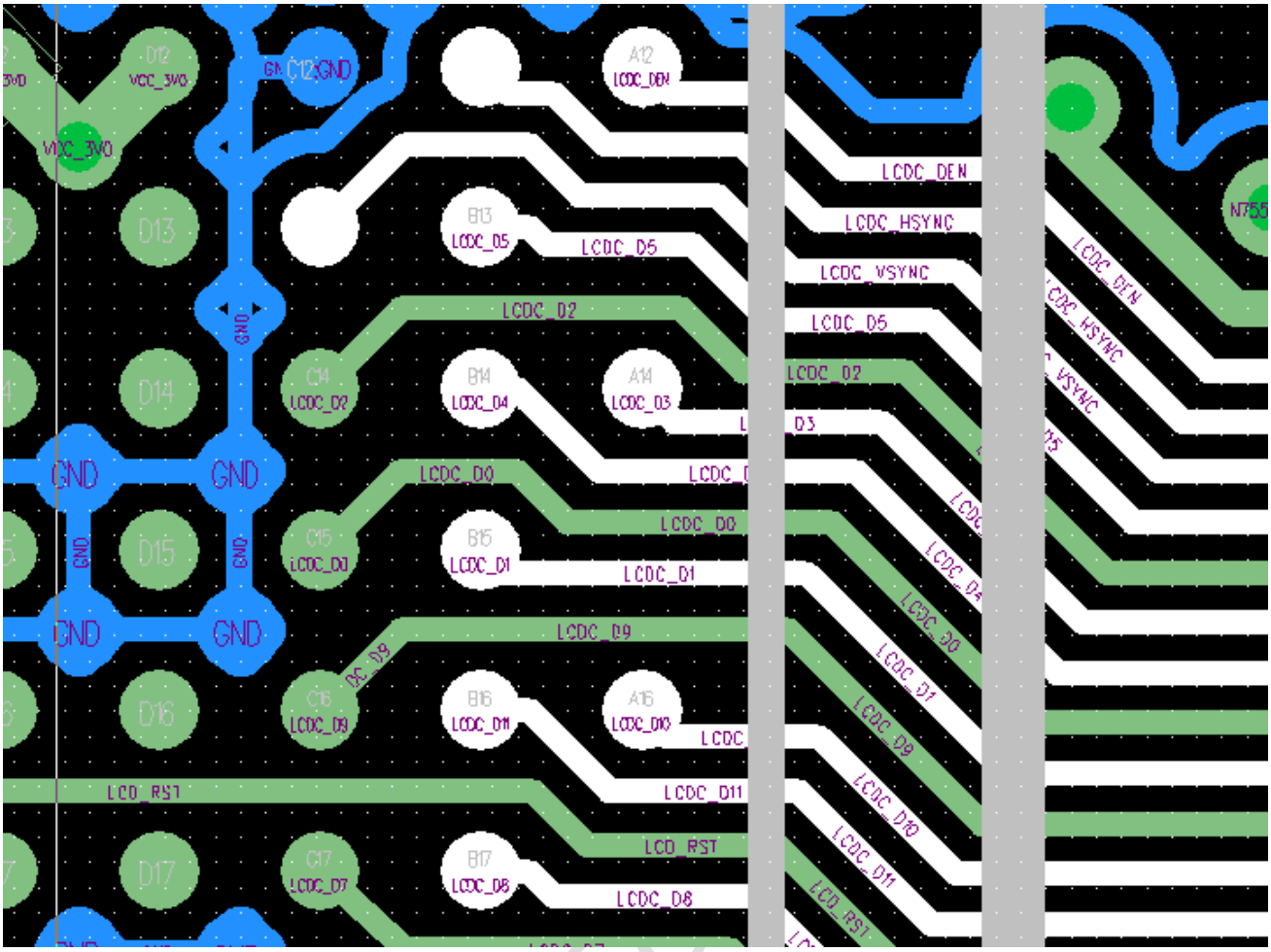


Figure 2-66 RK3326 LCDC M1 Pin Fanout

2.3.5 Camera Circuit

- **2.3.5.1 USB Camera**

  For USB Camera please refer to the USB design described in section 2.3.2.

- **2.3.5.2 MIPI-CSI Camera**

  RK3326 has one MIPI-CSI input with embedded ISP processor.

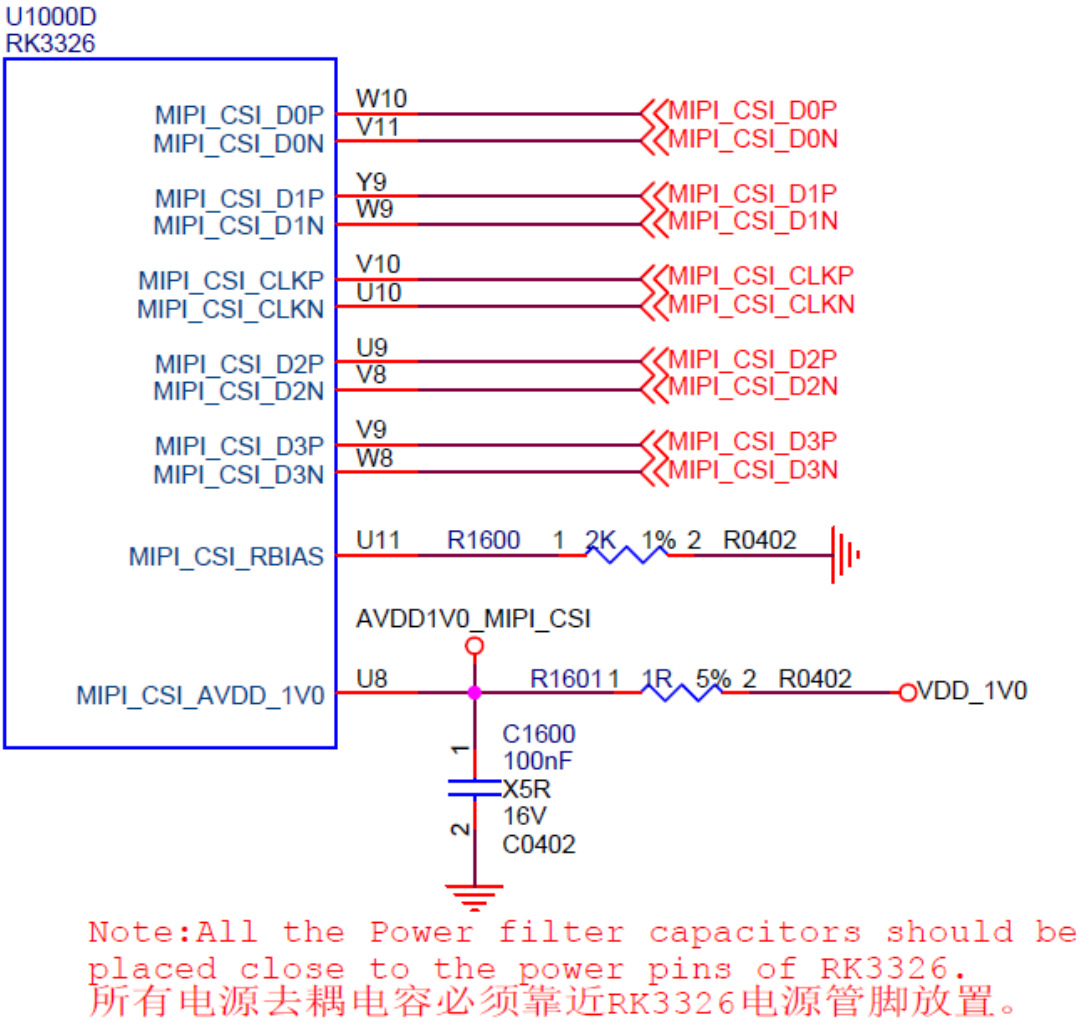


Figure 2-67 RK3326 MIPI-CSI Part

Please note for design:

- The reference resistor of the controller should select the resistor with 1% accuracy, and it will affect the signal quality of eye diagram.

Figure 2-68 RK3326 MIPI-CSI Controller Reference Resistor

- In order to avoid the damage of surge, the power of MIPI-CSI controller needs to series connect 1ohm resistance.

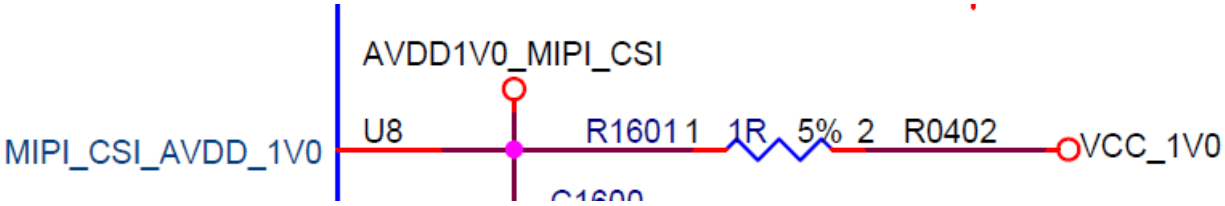
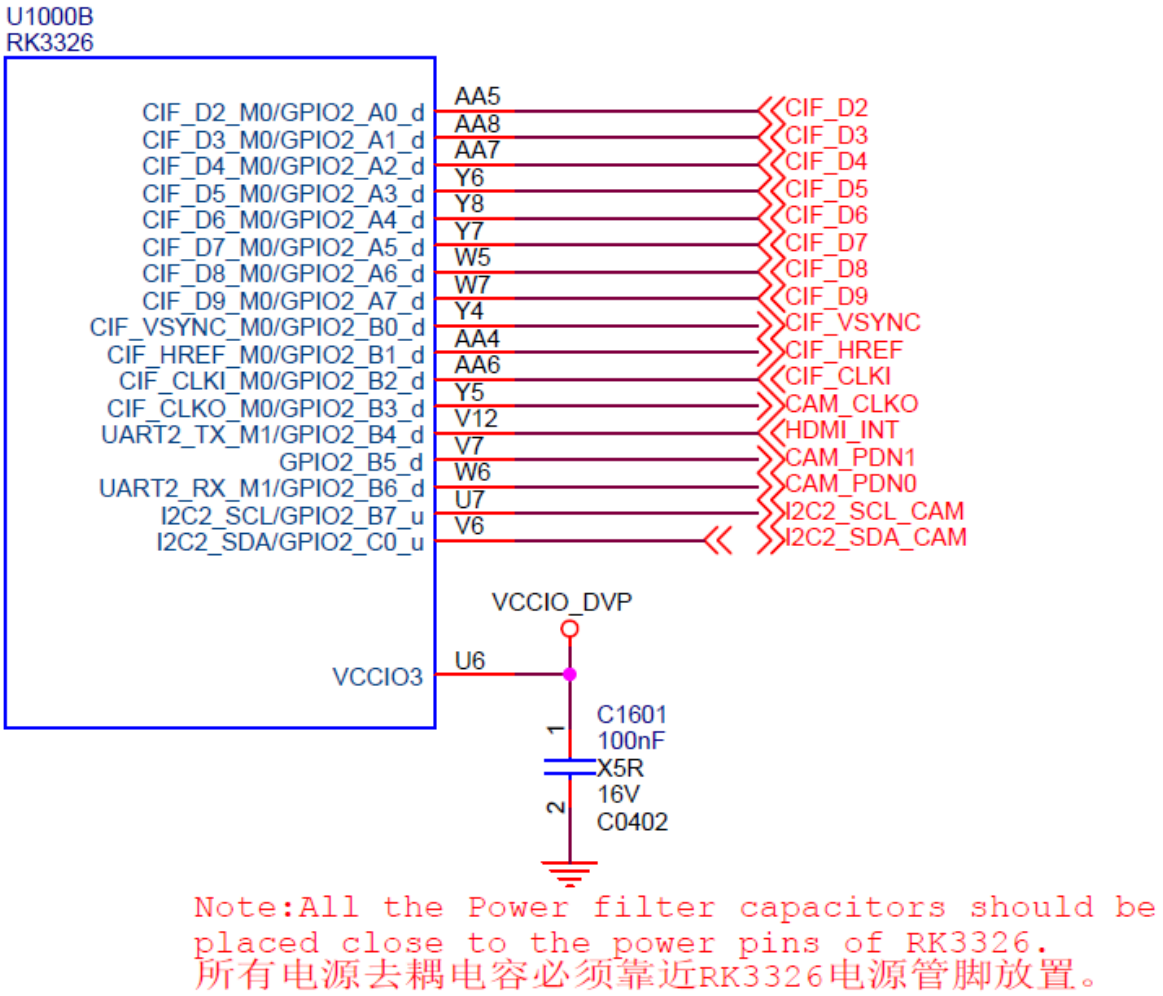


Figure 2-69 RK3326 MIPI-CSI Part Power Anti-surge

- In order to improve MIPI-CSI performance, the decoupling capacitor of the controller power should be placed close to the pin.

- **2.3.5.3 CIF Camera**

VCCIO3 is the power domain of CIF interface, and it can support 1.8V and 2.8V. Please select the corresponding voltage for IO supply(1.8V or 2.8V) in the application according to the product needs. Be noted that I2C pull-up level must be consistent with it otherwise the camera would not work normally.



Note:All the Power filter capacitors should be placed close to the power pins of RK3326.
所有电源去耦电容必须靠近RK3326电源管脚放置。

Figure 2-70 RK3326 CIF Part

2.3.6 ADC Circuit

RK3326 uses ADC_IN2 of SARADC as the sampling port of key value input and multiplexed with Recovery mode button (no need to update LOADER). If the system already has images, pull down ADKEY_IN when system boots up, keep ADC_IN2 to low level (0V), then RK3326 will enter Rockusb image download mode. When PC recognizes the USB device, release the button to make ADC_IN2 back to high level (1.8V), then the firmware can be downloaded to SOC.

RK3326 SARADC sampling range is 0-1.8V and the accuracy is 10bits. The key array is in parallel, and the key value can be adjusted by adding or reducing the key and tunning the proportion of the divider resistor to accomplish the multiple-key input to meet the customers' product requirements. It is recommended that the values between any two keys must be bigger than +/-35, that is the central voltage step must be bigger than 123mV.

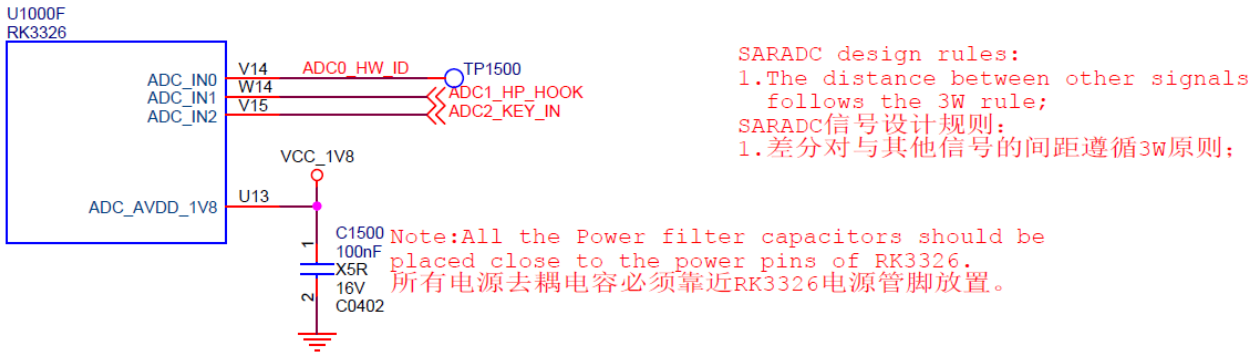


Figure 2-71 RK3326 SAR-ADC Part

2.3.7 SDIO/UART Circuit

RK3326 supports WIFI/BT module with SDIO 3.0 interface as shown below. It should be noted that the power supply of RK3326 SDIO and UART controller must be consistent with IO supply of the WIFI/BT modules.

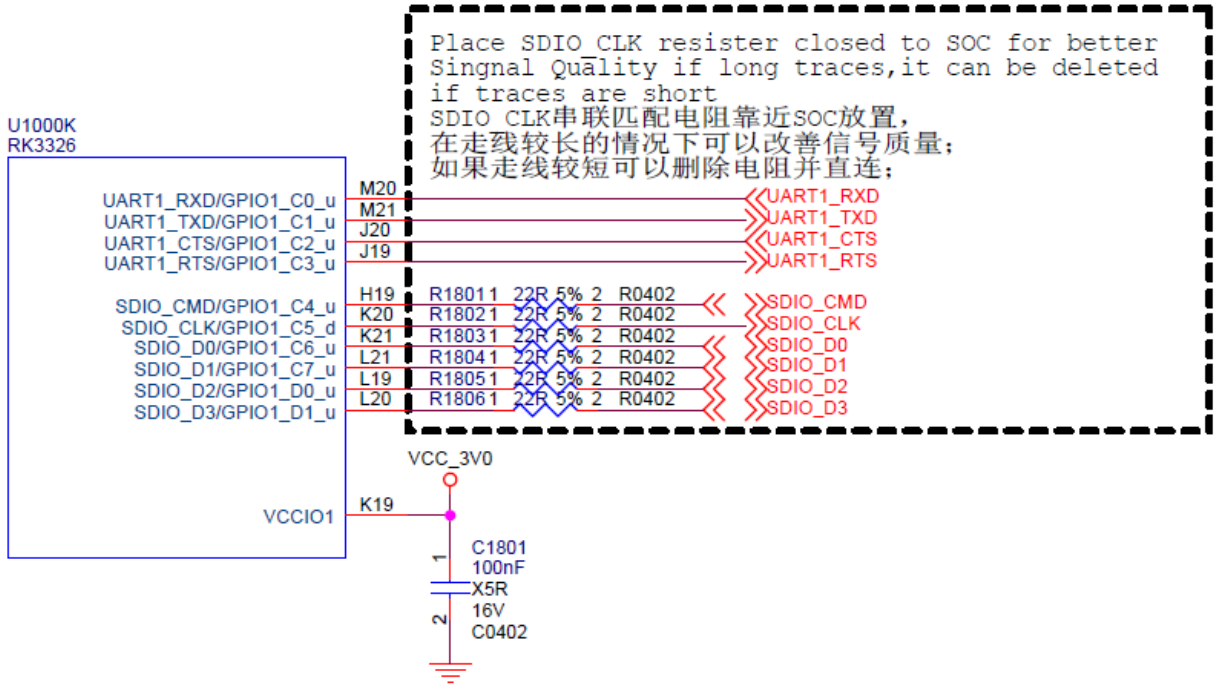


Figure 2-72 RK3326 SDIO/UART Part

- **2.3.7.1 SDIO**

SDIO interface pull up/down and matching design are recommended as below table.

Table 2-17 RK3326 SDIO Interface Design

Signal	Internal pull up/down	Connection method	Description (chip side)
SDIO_DQn[0:3]	pull up	Series connect 22ohm resistor can be deleted if the trace is short	SDIO data output/input
SDIO_CLK	pull down	Series connect 22ohm resistor	SDIO clock output

SDIO_CMD	pull down	Series connect 22ohm resistor can be deleted if the trace is short	SDIO command output/input

- **2.3.7.2 UART**

  UART interface pull up/down and matching design are recommended as Table 2-18.

Table 2-18 RK3326 UART Interface Design

Signal	Internal pull up/down	Connection method	Description (chip side)
UART1_RX	Pull up	Direct connection	UART1 data input
UART1_TX	Pull up	Direct connection	UART1 data output
UART1_CTSn	Pull up	Direct connection	UART1 permission output signal
UART1_RTSn	Pull up	Direct connection	UART1 request output signal

2.3.8 UART Debug Circuit

RK3326 Debug UART2 is reused with SDMMC interface, and you can externally connect UART-to-USB conversion board for debugging when needed.

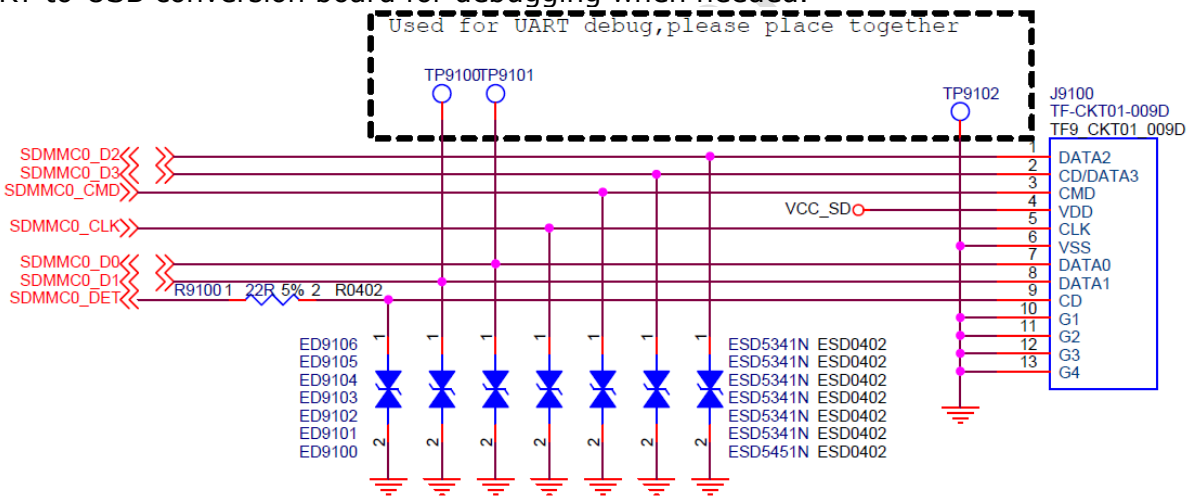


Figure 2-73 RK3326 UART2 Debug Point

Please select the port number of the board which is connected to PC, the baud rate selects 1.5M, and Flow control RTS/CTS doesn't need to select. If PC embedded DB-9 port doesn't support high speed mode, please use the USB-to-serial port conversion method.

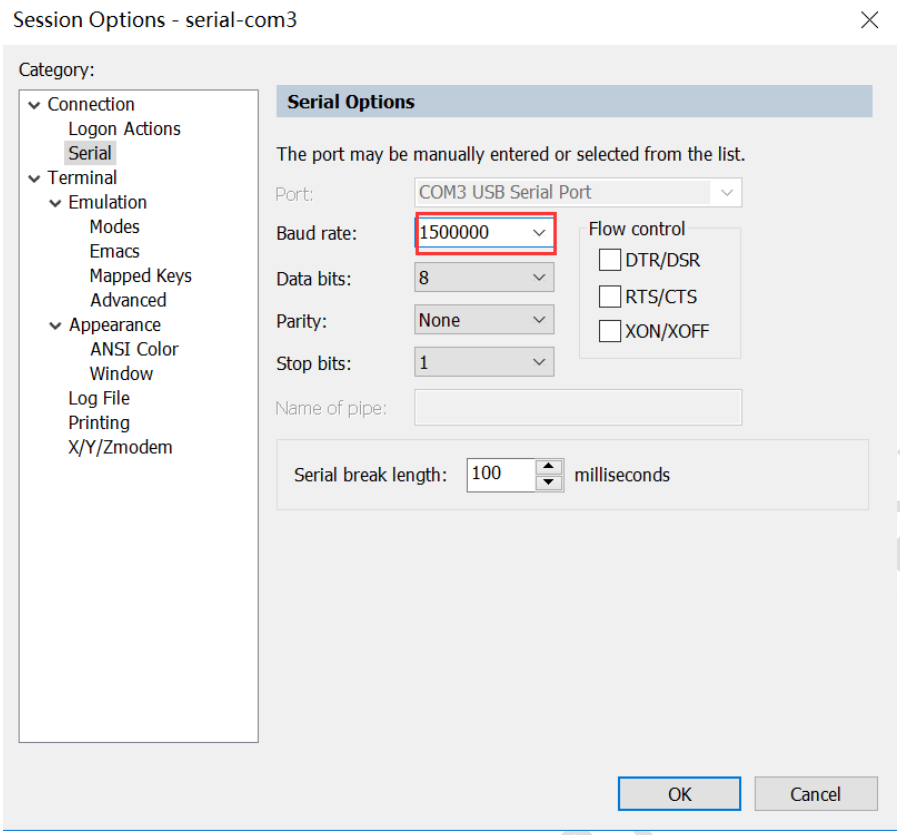


Figure 2-74 RK3326 Serial Port Configuration

3 Thermal Design Recommendation

3.1 Thermal Simulation

For RK3326 TFBGA418L package, we can get the thermal simulation report using the Finite Element Modeling (FEM) method based on EVB 4-layer PCB. This report is based on the JEDEC JESD51-2 standard; the system design and environment for the application may be different from the JEDEC JESD51-2 standard and need to do analysis according to the application conditions.

Note

Thermal resistance is the reference value of the PCB without the heat sink. The specific temperature is related to the board design, size, thickness, material and other physical factors.

3.1.1 Result Summaries

The thermal simulation result is shown as below:

Table 3-1 RK3326 Thermal Simulation Report

Package (EHS-FCBGA)	Power(W)	θ_{JA}(℃/W)	θ_{JB}(℃/W)	θ_{JC}(℃/W)
EVB PCB		25.4	NA	7.8

3.1.2 PCB Description

PCB structure used for thermal simulation is shown as below table:

Table 3-2 RK3326 Thermal Simulation PCB Sturcture

EVB PCB	PCB Dimension（L x W）	173.1 x 159.4mm
	PCB Thickness	1.6mm
	Number of Cu Layer	4-layers

3.1.3 Terminology

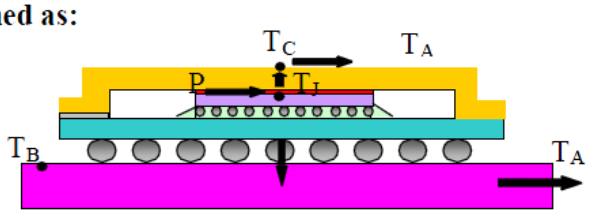
The terminologies in this chapter are explained as below:

- TJ: The maximum junction temperature;
- TA: The ambient or environment temperature;
- TC: The maximum compound surface temperature;
- TB: The maximum surface temperature of PCB bottom;
- P: Total input power

The thermal parameter can be define as following

1. *Junction to ambient thermal resistance,* θ_{JA}**, defined as:**

$$\theta_{JA} = \frac{T_J - T_A}{P} \quad ; \qquad (1)$$



Thermal Dissipation of EHS-FCBGA

Figure 3-1 θJA Definition

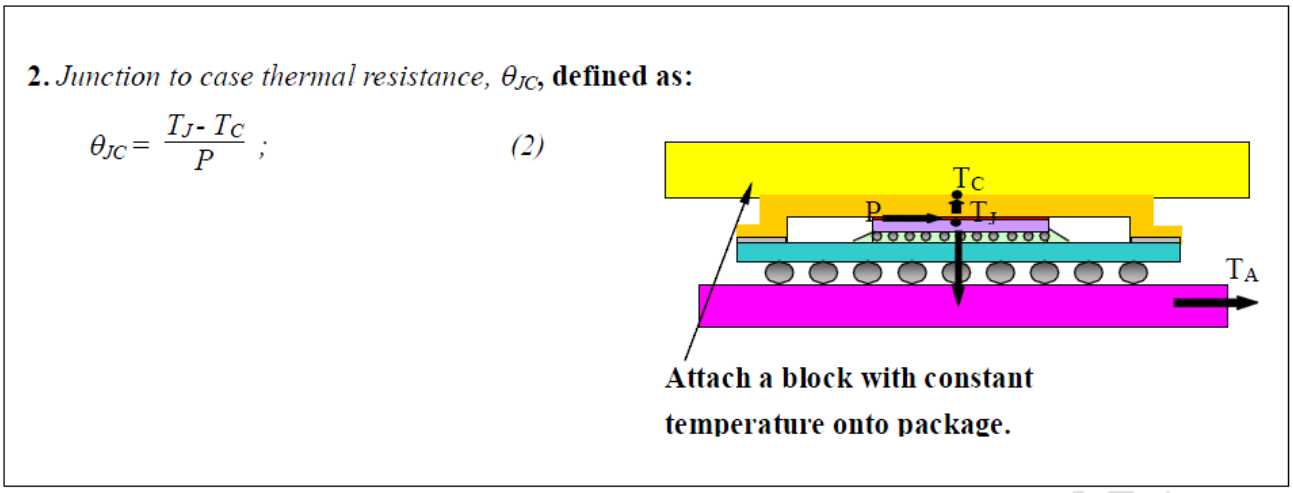


Figure 3-2 θJC Definition

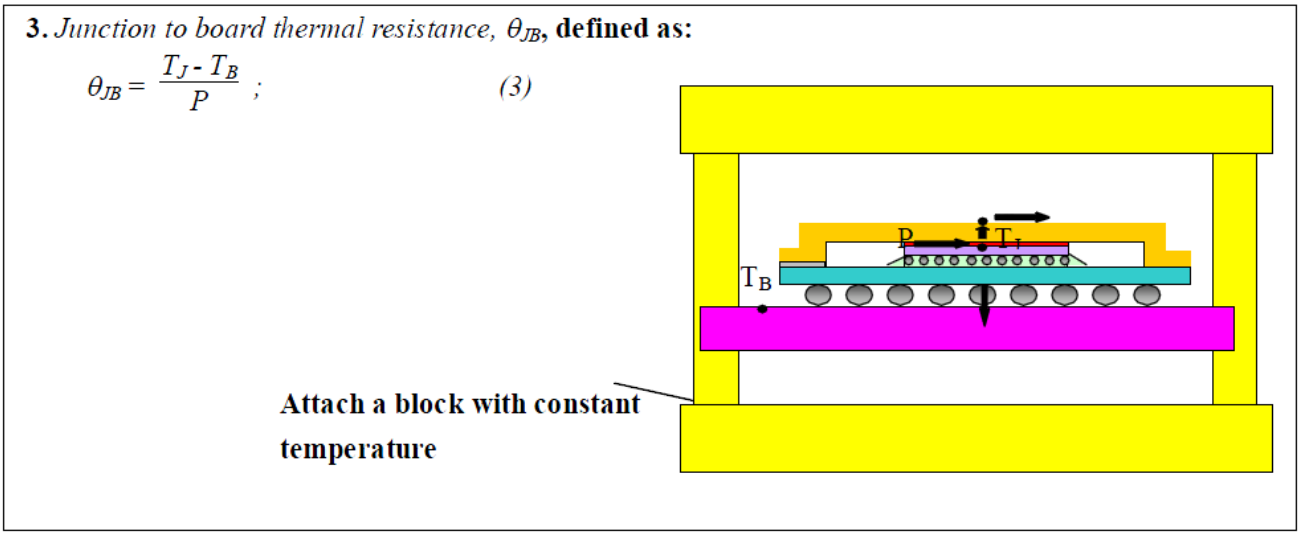


Figure 3-3 θJB Definition

3.2 SoC Internal Thermal Control Method

3.2.1 Thermal Control Strategy

In the Linux kernel, define a set of temperature control framework linux Generic Thermal System Drivers. It can control the temperature of the system through different strategies, and currently there are three commonly used strategies as below:

- Power-allocator: Introduce PID (proportional - integral - differential) control, according to current temperature, dynamically allocate power for the modules, and convert power into frequency, so as to achieve the effect of limiting the frequency according to the temperature.
- Step-wise: According to current temperature, limit the frequency step by step.
- Userspace: Do not limit the frequency.

RK3326 has embedded T-sensor to detect the chip temperature, the default policy is to use Power-allocator strategy, and the working state can be divided into the following cases:

- When the temperature exceeds the set value:
  - The temperature trend rises, start to decrease the frequency.
  - The temperature trend drops, start to increase the frequency.
- When the temperature drops to the set value:
  - The temperature trend rises, the frequency does not change.
  - The temperature trend drops, start to increase the frequency.
- When the frequency rises to the highest, but the temperature is still under the set

value, CPU frequency is no longer limited by thermal control, and changed to be controlled by system load.

- When the frequency is down, the chip is still over-temperature (such as poor heat dissipation) more than 95 degrees then the software will trigger a restart; If failure to restart due to deadlock or other reasons makes the chip temperature more than 100 ℃, it will trigger the chip internal OTP_OUT signal to PMIC for direct shutdown. Refer to Section 2.2.5.1 for specific actions.

Note

The temperature trend is obtained by comparing the two temperatures collected continuously. When the device temperature does not exceed the threshold, collect the temperature once every second. When the device temperature exceeds the threshold, collect the temperature once every 20ms and limit the frequency.

3.2.2 Thermal Control Configuration

RK3326 SDK can respectively provide temperature control strategy for CPU and GPU. For the specific configuration, please refer to 《Rockchip Thermal Development Guide》released by Rockchip.

4 ESD/EMI Protection Design

4.1 Overview

The chapter gives recommendations for ESD / EMI protection design in the RK3326 product design to help customers improve the anti-static and anti-electromagnetic interference levels of their products.

4.2 Terminology

The terminologies in this chapter are explained as below:

- ESD: Electro-Static discharge
- EMI: Electromagnetic Interference

4.3 ESD Protection

- To ensure a reasonable mold design; need to reserve ESD components for port and connector parts.
- PCB layout should do a good job in the protection and isolation for sensitive components.
- PCB layout should try to place RK3326 and the core components in the middle of the PCB, if it can not be placed in the middle of the PCB ,need to ensure that the shield is away from the PCB edge at least more than 2MM and can be reliably connected to GND.
- PCB layout should be designed according to the function module and the signal flow, the sensitive parts should be independent from each other, and the parts which are easy to be interfered should be isolated.
- Require to reasonably place ESD components, generally place them at the source, that is, ESD components should be placed in the position of interfaces or the electrostatic discharge area.
- The parts need to be placed away from the edge of the PCB and keep a certain distance from the connectors.
- The PCB surface must have a good GND loop, and the connectors must have a good GND connection loop on the surface layer. The shield should be connected with the surface GND, and need to add as many vias as possible to GND in the position of the shield cover welding. In order to do this, there should be no traces of connectors routing in the surface layer, and do not appear a wide range trace cutting off the copper.
- The PCB surface edge should have no traces and have as many vias as possible to GND.
- When it is necessary, do a good isolation between the signal and GND.
- Expose as much copper as possible, in order to enhance the electrostatic discharging effect, or add conductive cotton and other remedial measures.

4.4 EMI Protection

- There are three elements of electromagnetic interference: interference source, coupling channel and sensitive equipment. We can not deal with the sensitive equipment; so we can only deal with EMI through the interference source and the coupling channel. To solve the EMI problem, the best way is to eliminate the interference source, if it can not be eliminated, find the way to cut off the coupling channel or avoid the antenna effect.
- The PCB interference source is generally difficult to be completely eliminated, and can be dealt with through filter, ground, balance, impedance control or improve the signal quality (such as termination) and other methods. Generally various methods will be used synthetically, but good grounding is the most basic requirement.
- The commonly used material to deal with EMI includes the shielding cover, special

filters, resistors, capacitors, inductors, beads, common mode inductance / magnetic ring, absorbing materials, spread spectrum parts and so on.

- The filter selection principle: If the load (receiver) is high impedance (generally the single-ended signal interface is high impedance, such as SDIO, RBG, CIF, etc.), then select the capacitive filter parallel connected into the trace; if the load (receiver) is low impedance (such as power output interface), then select the inductive filter component series connected into the trace. The use of the filter should not make the signal quality beyond its SI permissible range. Differential interfaces usually use common mode choke to suppress EMI.
- The PCB shielding measures should be well-grounded otherwise it may cause radiation leakage or shielding measures to form the antenna effect. The connector shield should meet the relevant technical standards.
- RK3326 can use spread spectrum function by modules. The degree of the spread spectrum depends on the signal requirements of the relevant part. Refer to RK3326 spread spectrum description for the specific measures.
- The LAYOUT requirements of EMI are highly consistent with ESD. The above-mentioned layout requirements of ESD are mostly applicable for EMI protection. Besides, add the following requirements:
  - Ensure the signal integrity as much as possible.
  - The differential signal should do the isometric and tight coupling to ensure the differential signal symmetry; try to minimize the differential signal and the clock dislocation, to avoid conversion to the common mode signal which will cause EMI issues.
  - Plug-in electrolytic capacitors and other components with metal shell should avoid coupling the interference signal to produce radiation. Also need to avoid the interference signal of the components coupling from the shell to other signals.

5 Welding Process

5.1 Overview

RK3326 is the ROHS directive certification products, that is, Lead-free products. This chapter regulates the RK3326 SMT basic settings of the temperature for customers. It mainly introduces the process control when customers use RK3326 to do the re-flow solder: mainly lead-free process and mixed process.

5.2 Terminology

The terminologies in this chapter are explained as below:

- Lead-free: Lead-free process.
- Pb-free: Lead-free process; all components (mainboard, all IC, resistance, capacitors, etc.) are lead-free components, and use pure lead-free process with the lead-free solder paste.
- Reflow profile: Reflow soldering temperature curve.
- ROHS: Restriction of Hazardous Substances.
- SMT: Surface Mount Technology.
- Sn-Pb: Tin-lead mixed process; means to use lead solder paste and have both lead-free BGA and lead IC hybrid welding process.

5.3 Re-flow Solder Requirement

5.3.1 Solder Paste Ingredient Requirement

The proportion of solder alloy and flux is 90%: 10%; volume ratio: 50%: 50%, solder paste refrigerated temperature is 2 ~ 10 ℃, and should be put in room temperature to recover the temperature before using. It will take 3 ~ 4 hours to recover and need to make a record.

The solder paste needs to be stirred before brushing the board. Manually stir for 3-5 minutes or mechanically stir for 3 minutes. After stirring, it will present a natural vertical flow shape.

5.3.2 SMT Re-flow Profile

As RK3326 chip uses environmental protection material, recommend to use Pb-Free process. The reflow profile below is only the recommended value required by the JEDEC J-STD-020D process. Customers need to adjust according to the actual production situation.

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)*	See classification temp in Table 4.1	See classification temp in Table 4.2
Time (t_p)** within 5 °C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Figure 5-1 Reflow Profile Classification

Package Thickness	Volume mm³ <350	Volume mm³ 350 - 2000	Volume mm³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Figure 5-2 Lead-free Process Component Package Heat-Resistant Standard

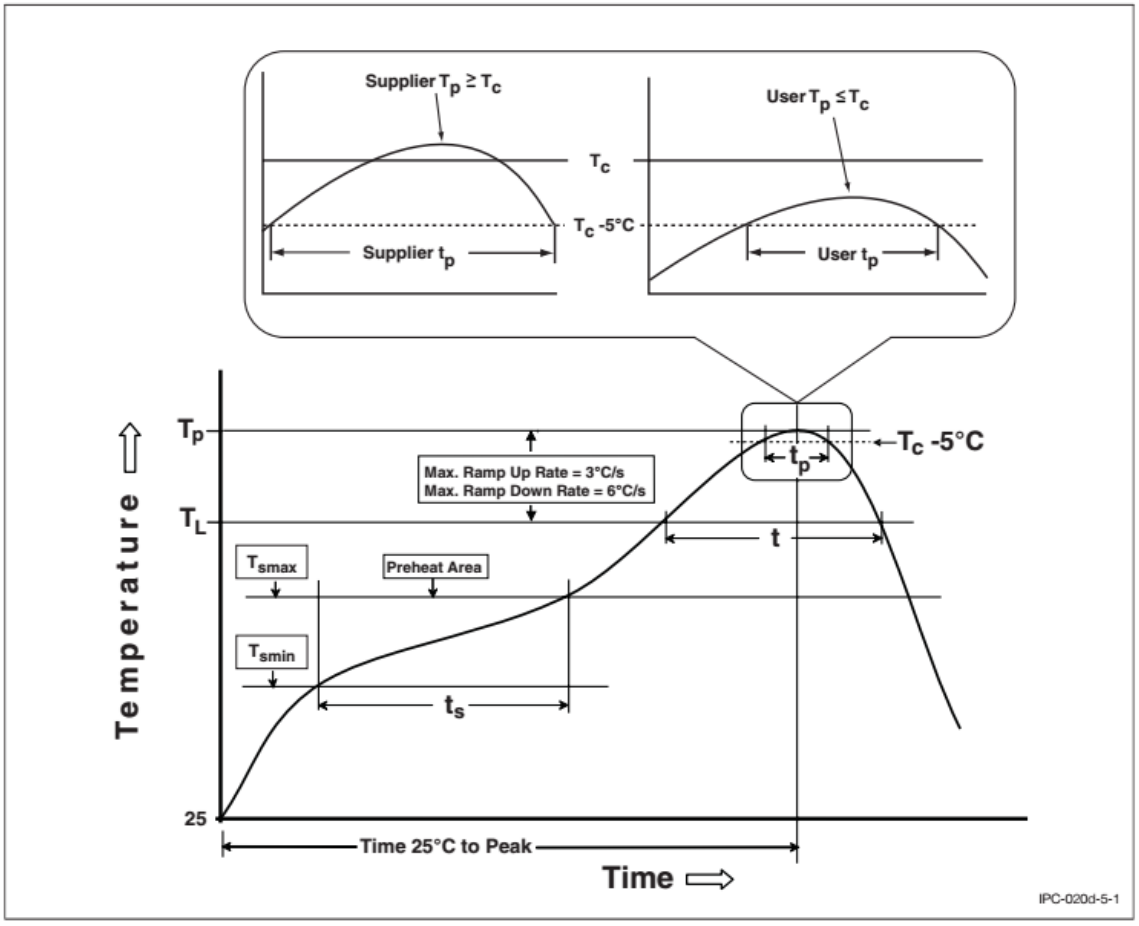


Figure 5-3 Pb-free Reflow Profile

5.3.3 SMT Recommended Reflow Profile

RK recommended SMT reflow profile is shown as Figure 5-4:

Step 1 Board Preheat	Step 2 Soak Time	Step 3 Peak Reflow & Time Above 220 °C	Step 4 Cool Down
Start with solder joint temp ≤ 40°C	After nozzle is lowered prior to peak reflow (Soak Time: Paste dependant; consult paste manufacturer)	Solder Joint Temp 230 – 250°C Above ≥217°C 60 – 90 sec Max delta-t of solder joint temperature at peak reflow ≤10°C	Substrate MAX Temperature ≤260°C Die Peak Temperature ≤300°C
Rising Ramp Rate 0.5 – 2.5° C/ Sec.	Solder Joint Temp: 200 to 220°C		Cooling Ramp Rate -0.5 to – 2.0°C/sec
Board Preheat Solder Joint Temp: 125 – 150°C	Critical Ramp Rate (205 to 215°C): 0.35 – 0.75°C/sec.	Peak Temp Range, and Time Above ≥217°C spec's met.	PCB land/pad temperature needs to be at 100 – 130°C ±5°C when removing board from rework machine bottom heater at end of component removal operation or ≤80°C when using stand alone PCB Pre-Heater for PCB land/pad site dress operation.
Preheat with bottom heater, before nozzle is lowered	Nozzle has lowered to reflow component	Nozzle is down during peak reflow	Nozzle raises to home position when solder joint reaches peak temp range

Figure 5-4 Pb-free Reflow Profile Recommended Parameter

6 Packaging And Storage Condition

6.1 Overview

The chapter regulates RK3326 storage and usage specification to ensure the safety and correct usage of the product.

6.2 Terminology

The terminologies in this chapter are explained as below:

- Desiccant: A material used to adsorb moisture.
- Floor life: The longest time allowing the product exposed in the environment, from unpacking the moisture barrier bag to SMT.
- HIC: Humidity Indicator Card.
- MSL: Moisture Sensitivity Level.
- MBB: Moisture Barrier Bag.
- Rebake: Bake again.
- Shell Life: The storage expiration.

6.3 Dry Vacuum Packaging

The dry vacuum packaging material of the product is as below:

- Desiccant
- HIC
- MBB, aluminum foil, silver opaque logo with moisture sensitivity level.

Figure 6-1 RK3326 Dry Vacuum Packaging

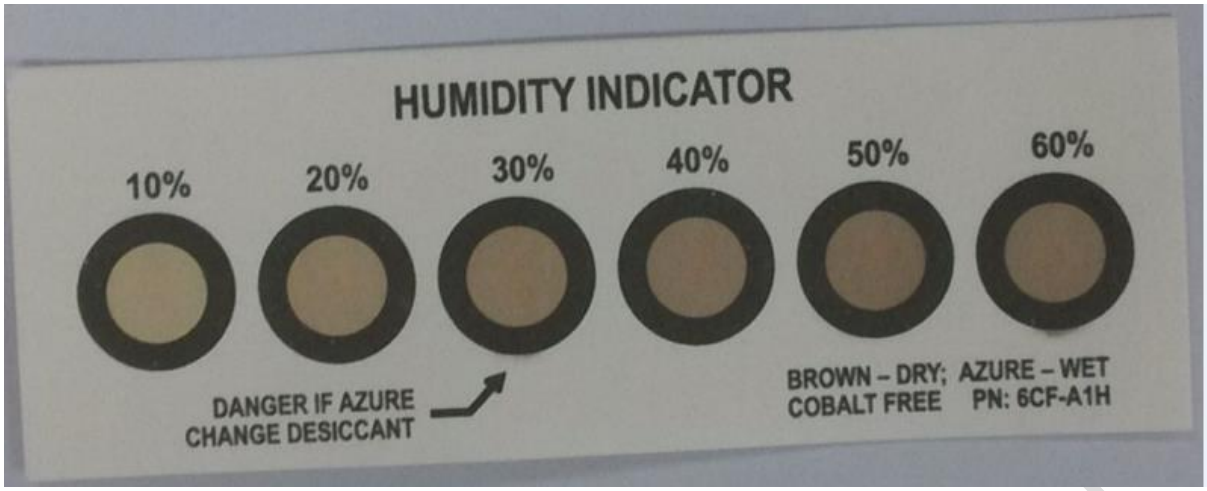


Figure 6-2 Humidity Indicator Card

6.4 Product Storage

6.4.1 Storage Environment

Product is vacuum packaged, and can be stored up to 12 months with environment temperature ≤ 40 ℃ and relative humidity ＜90%.

6.4.2 Exposure Time

Under ambient conditions <30 ° C and relative humidity 60%, please refer to below table 6-1.

RK3326 MSL level is 3, very sensitive to humidity. If the chip is not used for a long time after unpacking, and directly used in SMT without bake, chip failure will be likely to appear.

Table 6-1 Exposure Time Reference Table (MSL)

MSL Level	Exposure Time Factory environmental conditions:≦30 ℃ /60 %RH
1	Unlimited at ≤300 ℃/85 %RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use, and must be reflowed within the time limit specified on the label.

6.5 Moisture Sensitive Product Usage

The RK3326 must be baked after unpacking in the following cases:

- Continuous or accumulative exposure time is less than 168 hours, and the factory environment ≦ 30 ℃ / 60% RH.
- Stored in the <10% RH environment.

In below cases, RK3326 must be baked to eliminate the internal moisture to avoid the delamination and popcorn issues during reflow solder:

- The points > 10% of humidity indicator card already discolor at 23 ± 5 ℃. (Please refer to the humidity indicator card for color change).
- Not meet 2a or 2b standard.

Please refer to the following table 6-2 for RK3326 re-baking time:

Table 6-2 RK3326 Re-bake Reference Table

Package Body	MSL	High Temp Bake @125℃ +10/-0℃		Medium Temp Bake @90℃+8/-0℃		Low Temp Bake @40℃ +5/-0℃	
		Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h	Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h	Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h
Thickness ≤1.4mm	3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Note

The table shows the minimum baking time required after damp.
Re-base prefers to use low-temperature baking.