RK3399 Hardware Design Guide

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Foreword

➢ Overview

This document mainly introduces the main points of RK3399 hardware design and notes, aims to help RK customers shorten the design cycle, improve the design stability and reduce the failure rate. Please refer to the requirements of this guide for hardware design, and using the relevant core templates released by Rockchip as possible as you can. If it needs to be changed for special reasons, please according strictly to the design requirements of high speed digital circuit.

➢ SOC Type

- The document is only fit for RK3399

➢ Application Object

This document is mainly suitable for the following engineers:

- Hardware development & PCB layout engineers
- Field application engineers
- Embedded Software Development Engineers
- Test engineers

Revision History

Ver.	Modify by	Revision Date	Revision Description	Remark
1.0	Harebee	2017.4.20	Initial Release	
1.1	Harebee	2017.9.19	Update	
1.2	Harebee	2017.12.21	Update	

Acronym

Acronym includes the abbreviations of phases commonly used in this document.

DDR	Double Data Rate SDRAM	双倍速率同步动态随机存储器
DP	DisplayPort	外置显示频接口
eDP	Embedded DisplayPort	内置显示接口
eMMC	Embedded Multi Media Card	内置多媒体存储卡
HDMI	High Definition Multimedia Interface	高清晰度多媒体接口
I^2C	Inter-Integrated Circuit	内部整合电路(两线式串行通讯总线)
JTAG	Joint Test Action Group	联合测试行为组织定义的一种国际标准测试协议（IEEE 1149.1兼容）
LDO	Low Drop Out Linear Regulator	低压差线性稳压器
LVDS	Low-Voltage Differential Signaling	低电压差分信号，显示接口
MAC	Media Access Control	以太网媒体接入控制器
MIPI	Mobile Industry Processor Interface	移动产业处理器接口
PCIe	Peripheral Component Interconnect -express	外设组件互联标准
PMIC	Power Management IC	电源管理芯片
PMU	Power Management Unit	电源管理单元
RK	Fuzhou Rockchip Electronics Co.,Ltd.	福州瑞芯微电子股份有限公司
SD Card	Secure Digital Memory Card	安全数码卡
SDIO	Secure Digital Input and Output interface	安全数字输入输出接口
SDMMC	Secure Digital Multi Media Card	安全数字多媒体存储卡
SPDIF	Sony/Philips Digital Interface Format	SONY/PHILIPS数字音频接口
SPI	Serial Peripheral Interface	串行外设接口
TF Card	Micro SD Card(Trans-flash Card)	外置记忆卡
Type-C	USB Type-C interface	一种USB标准接口
USB	Universal Serial Bus	通用串行总线
VR	Virtual Reality	虚拟现实

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Chapter1 Introduction

1.1 Overview

RK3399 is a low power and high performance processor based on Big.Little architecture, which includes dual-core ARM cortex –A72 MPcore processor and quad-core ARM cortex-A53 MPcore processor with separate NEON coprocessor, can be applied to computers, mobile phones, personal mobile internet, digital multimedia equipment.

Many embedded powerful hardware engines provide optimized performance for high-end application. RK3399 supports high-quality JPEG encoder/decoder and pre-processing and post-processing of special image,and it also supports multi-format video decoders including H.264/H.265/VP9 up to 4Kx2K @60fps decoding,especially H.264/H.265 10bits decoding and H.264/MVC/VP8 1080p@30fps encoding.

Embedded 3D GPU makes RK3399 completely compatible with OpenGL ES1.1/2.0/3.0/3.1,OpenCL and DirectX 11.1. Special 2D hardware engine with MMU will maximize display performance and provide very smooth operation.

RK3399 has high-performance dual channel external memory interface (DDR3/DDR3L/LPDDR3/LPDDR4) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications.

1.2 Features

1.2.1 CPU

- Dual-core ARM Cortex-A72 MPCore processor and Quad-core ARM Cortex-A53 MPCore processor, both are high-performance, low-power and cached application processor
- 64 bits high performance CPU
- Built-in low power MCU Cortex-M0

1.2.2 GPU

- 4 cortex ARM Mali-T860MP4 high performance GPU
- Support OpenGL ES1.1/2.0/3.0/3.1、OpenVG1.1、OpenCL、DX11
- Support AFBC (Frame Buffer Compression)

1.2.3 Memory

- Dual channel DDR3/DDR3L/LPDDR3/LPDDR4
- Support eMMC 5.1,SDIO 3.0

1.2.4 Multi-media

- Support 4K VP9 and 4K 10bits H265/H264 video decoding,up to 60fps
- 1080P multi-format video decoding (WMV、MPEG-1/2/4、VP8)
- 1080P video decoding,support H.264,VP8 format
- Video post-production processor: deinterlacing, denoising, edge / detail / color optimization

1.2.5 Display

- Embedded dual VOP,support 4096x2160 AFBC and 2560x1600
- Embedded dual channels MIPI-DSI（4 lanes per chanel）
- Compliant with eDP 1.3（4 lanes,2.7Gbps）
- Compliant with HDMI 2.0 up to 4K 60fps, compliant with HDCP 1.4/2.2
- Compliant with DisplayPort V 1.2 (4 lanes,up to 4K 60Hz)
- Support Rec.2020/Rec.709

1.2.6 Camera

- Dual ISP pixel processing capacity up to 13MPix/s, Support dual camera data simultaneous input

1.2.7 Interface

- Embedded dual USB 2.0 OTG and dual USB 2.0 HOST
- Embedded dual USB 3.0 Type-C

- Compliant with PCI-Express 2.1
- Support 8 channels digital microphone array input

1.3 Block Diagram

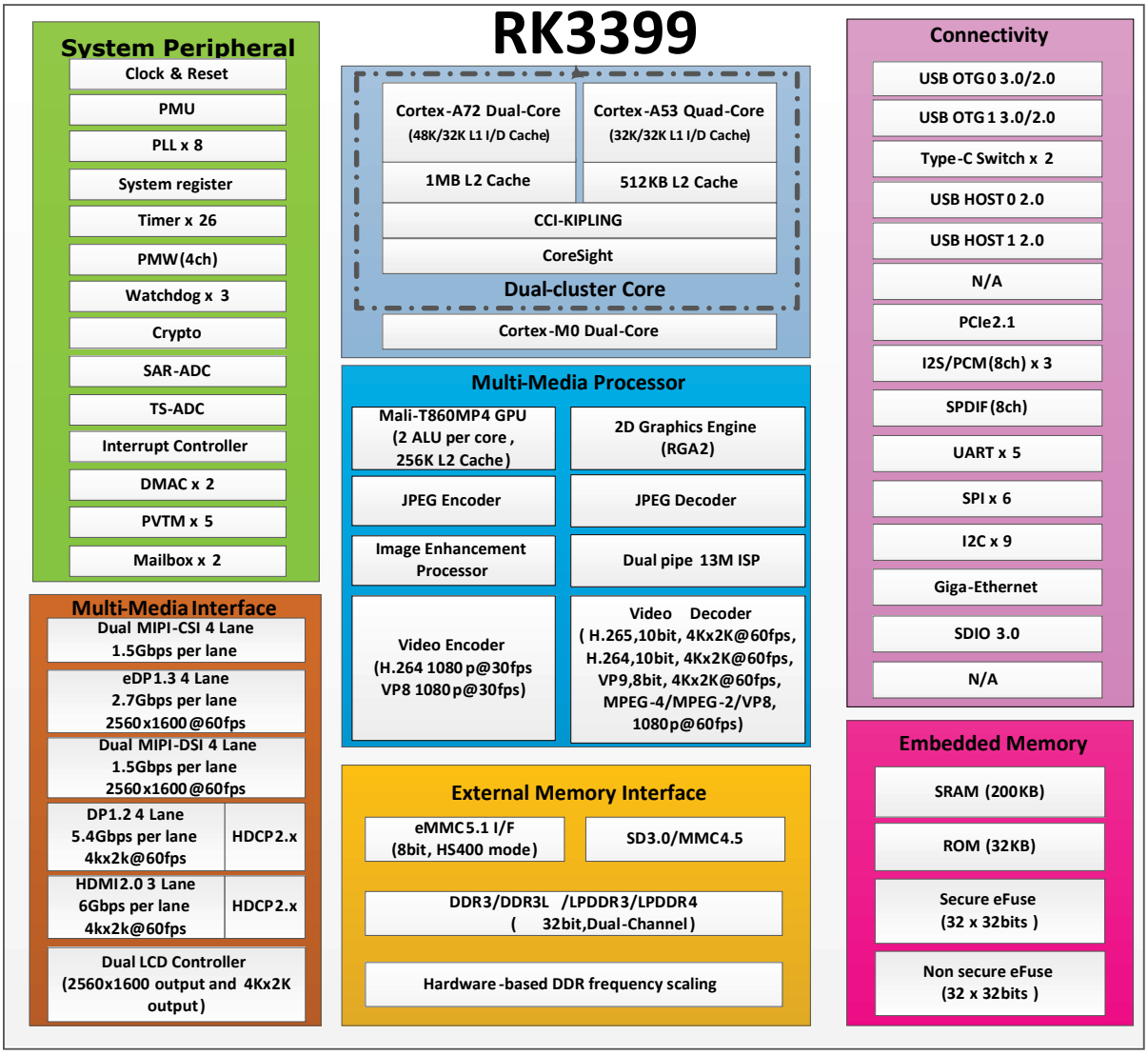


Figure 1-1 RK3399 Block Diagram

1.4 Application Block Diagram

1.4.1 NetBook Application Block Diagram

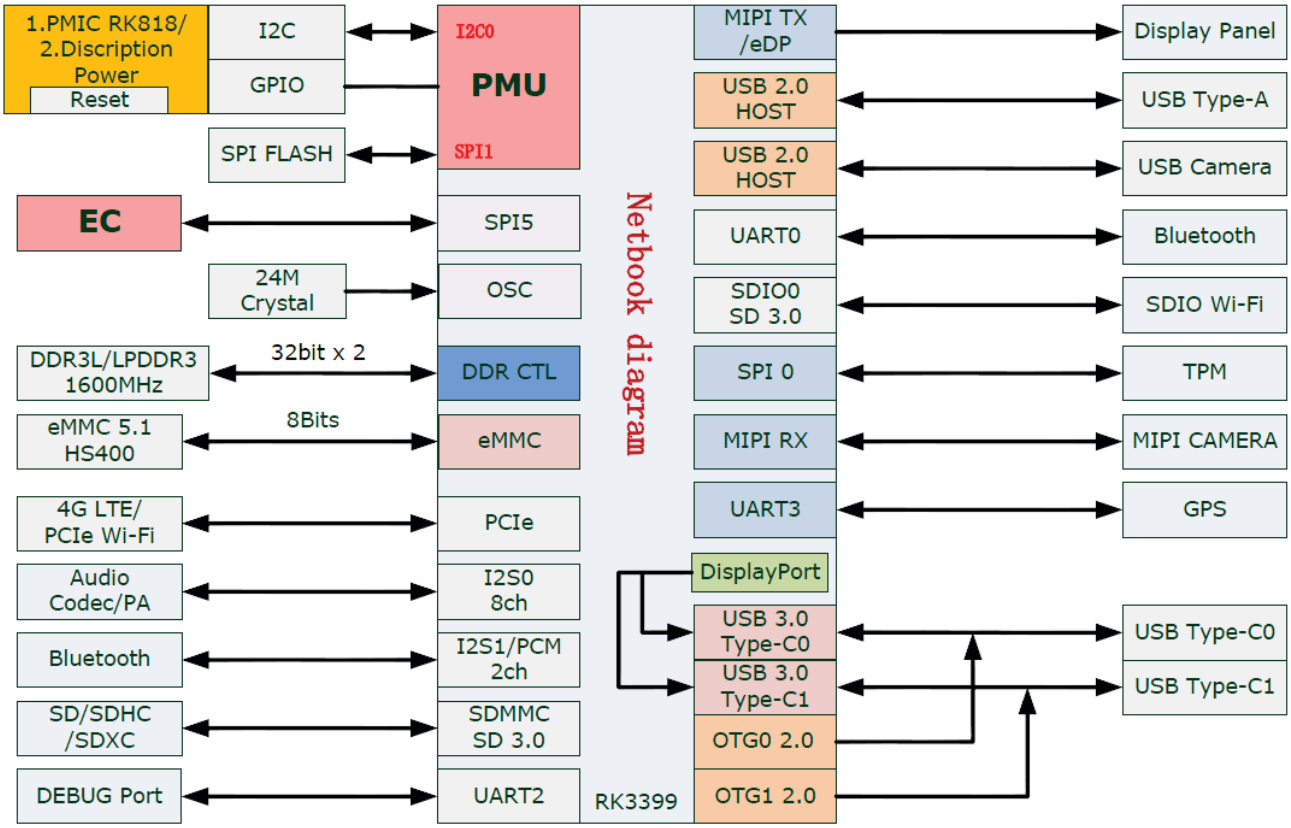


Figure 1-2 RK3399 NetBook Application Block Diagram

1.4.2 Box Application Block Diagram

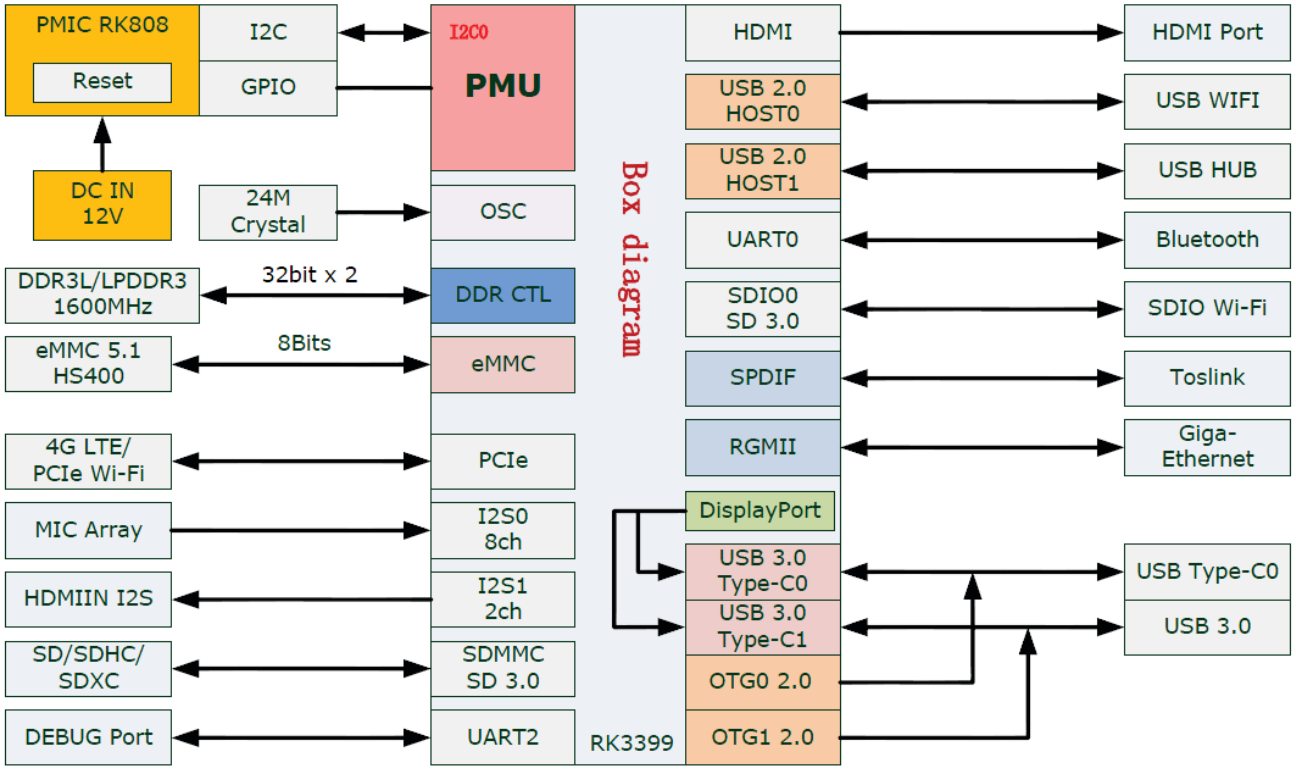


Figure 1-3 RK3399 Box Application Block Diagram

1.4.3 Tablet Application Block Diagram

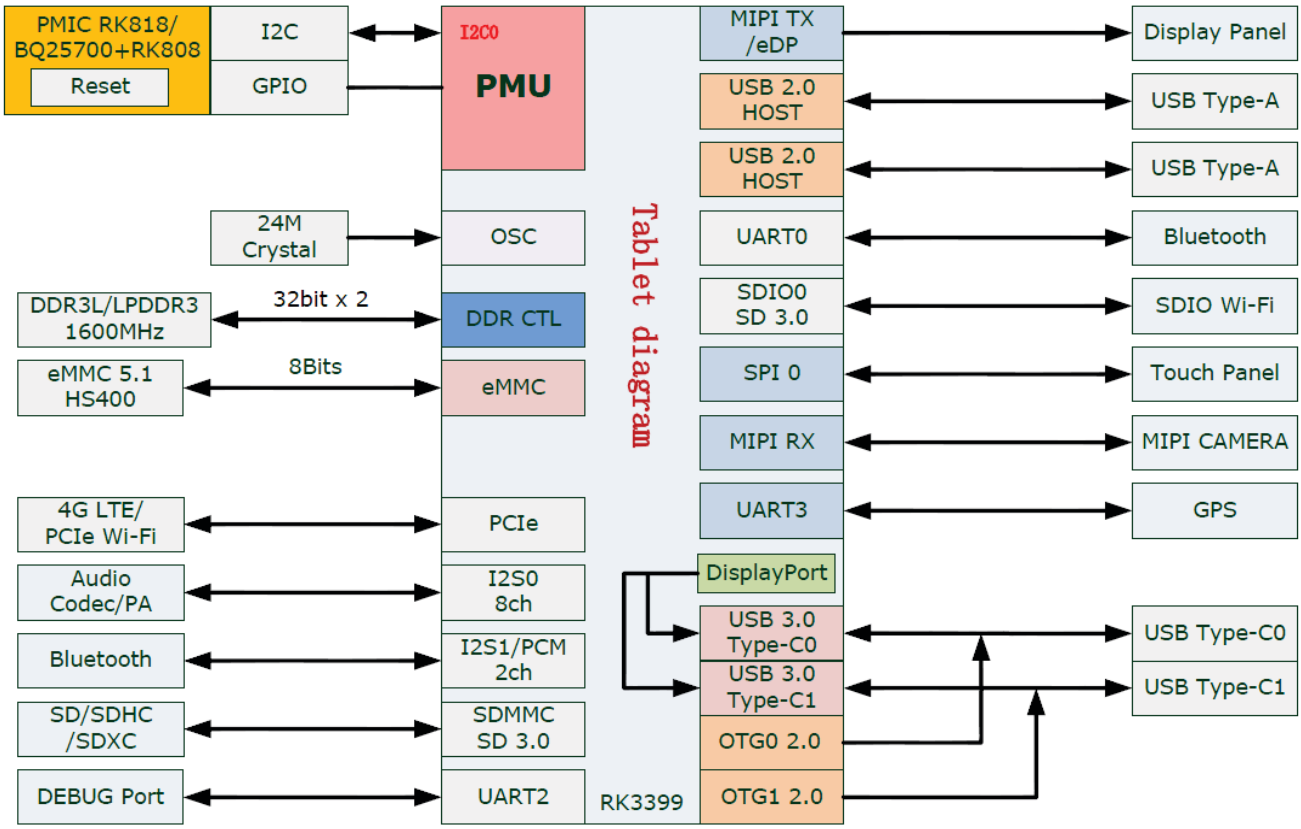


Figure 1-4 RK3399 Tablet Application Block Diagram

1.4.4 VR Application Block Diagram

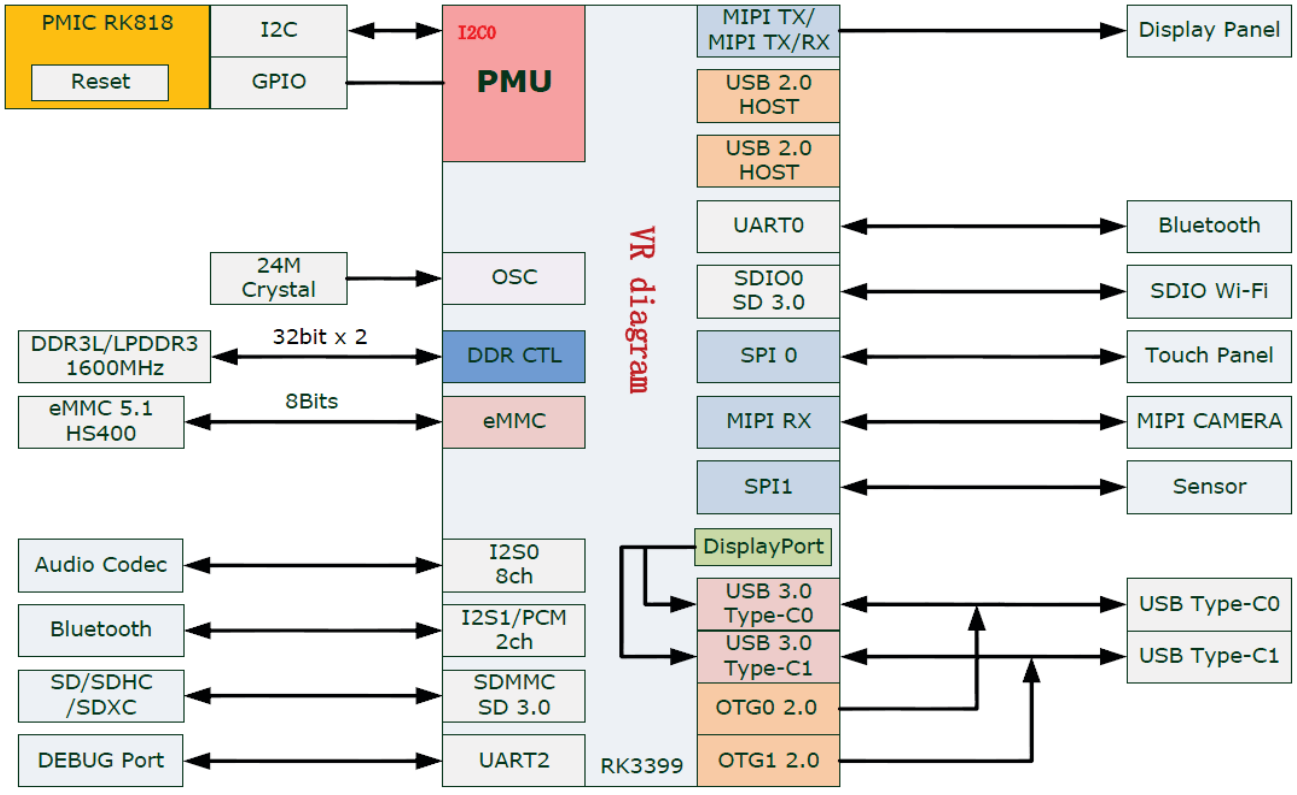


Figure 1-5 RK3399 VR Application Block Diagram

Notes:

The above figure is the application block diagram of RK3399; for the detail, please refer to the reference design document which released by Rockchip.

Chapter2 Package Information

2.1 Package

2.1.1 Information

Table 2-1 RK3399 Package Information

Orderable Device	RoHS Status	Package	Package Qty	Device special feature
RK3399	Pb-Free	FCBGA828	TBD	Cortex A72 + Cortex A53

2.1.2 Top Marking

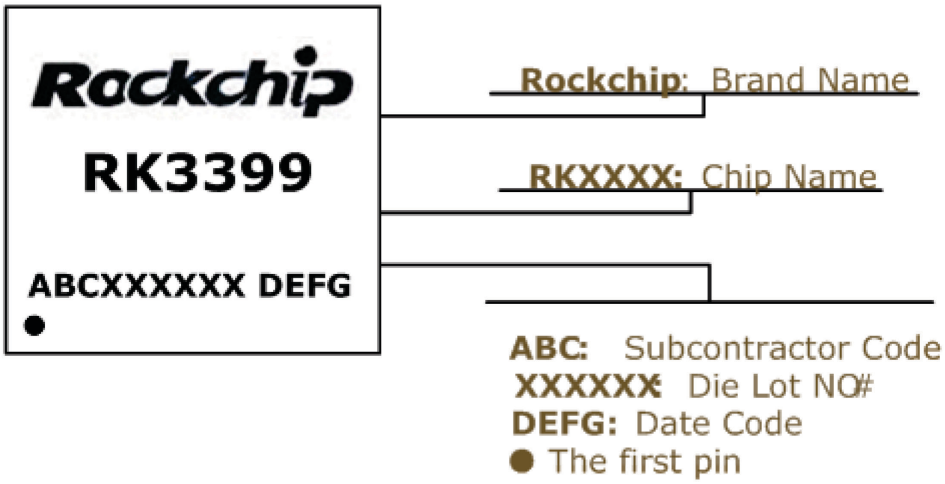


Figure 2-1 RK3399 top marking

2.1.3 Package Dimensions

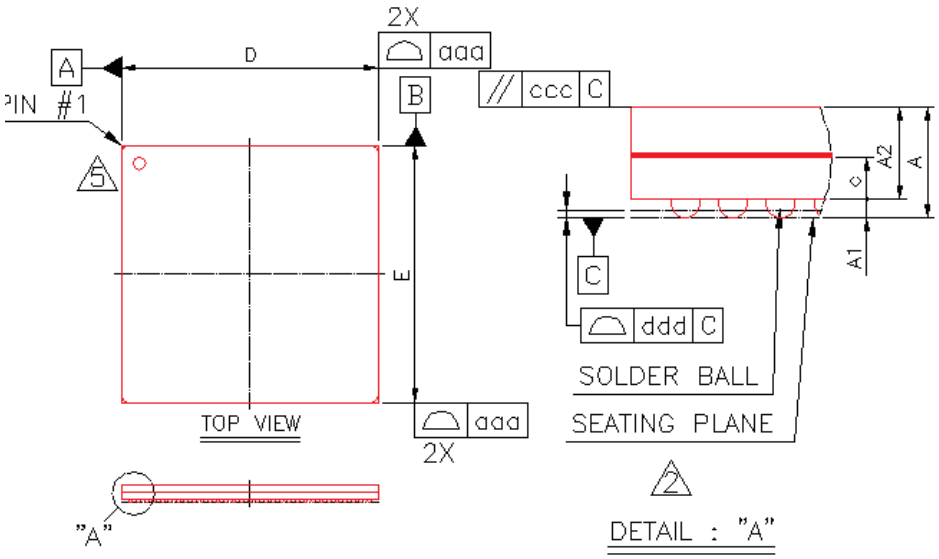


Figure 2-2 RK3399 package dimensions 1

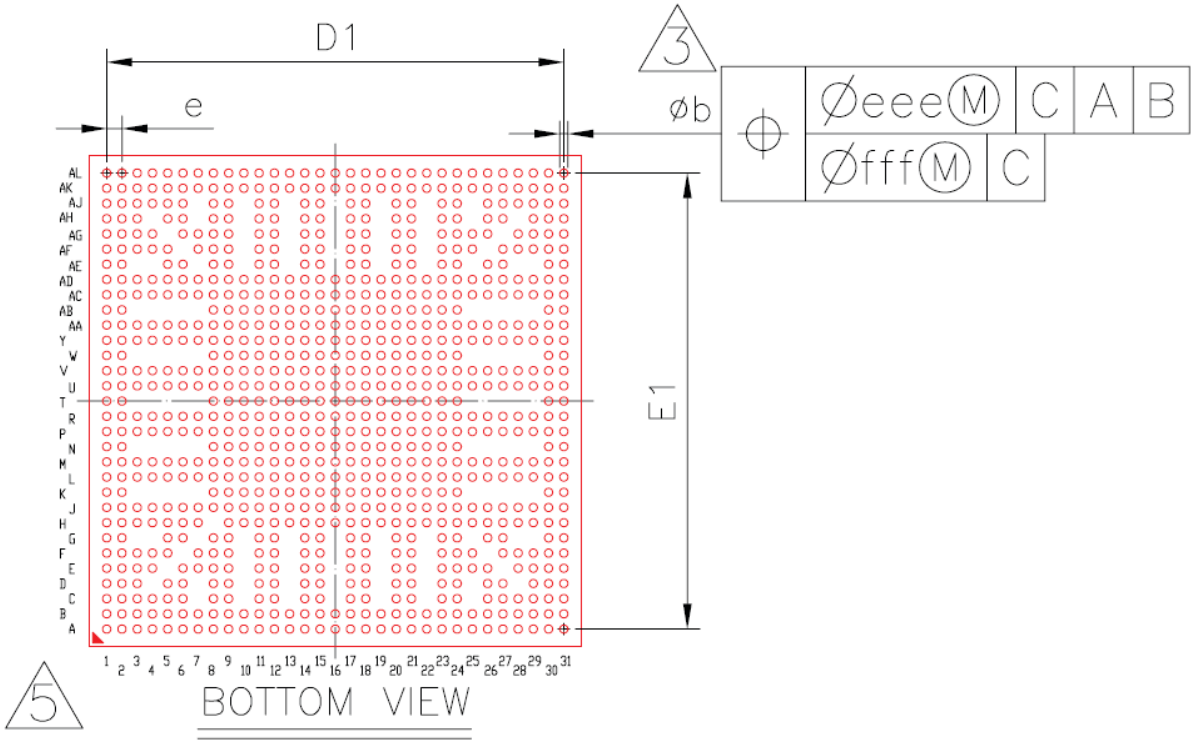


Figure 2-3 RK3399 package dimensions 2

Symbol	Dimension in mm			Dimension in inch		
	MIN	NORMAL	MAX	MIN	NORMAL	MAX
A	1.41	1.51	1.61	0.056	0.059	0.063
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	1.11	1.26	1.41	0.044	0.050	0.056
C	0.47	0.57	0.67	0.019	0.022	0.026
D	20.90	21.00	21.15	0.823	0.827	0.833
E	20.90	21.00	21.15	0.823	0.827	0.833
D1	---	19.50	---	---	0.768	---
E1	---	19.50	---	---	0.768	---
e	---	0.65	---	---	0.026	---
b	0.30	0.35	0.40	0.012	0.014	0.016
aaa	0.20			0.008		
ccc	0.25			0.010		
ddd	0.20			0.008		
eee	0.25			0.010		
fff	0.10			0.004		

Figure 2-4 RK3399 package dimensions 3

Notes:

1. *Controlling dimension: millimeter*
2. *Primary datum C and seating plane are defined by the spherical crowns of the solder balls*
3. *Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C*
4. *Special characteristics C class: A, ddd*
5. *The pattern of pin 1 fiducial is for reference only*
6. *The tilt of heat sink should be within 10mil(0.254mm) (vertical position)*

2.1.4 Ball Map

828	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	0
A	VSS_1	DDR1_CSN1	DDR1_A12	DDR1_A10	DDR1_CKE0	DDR1_A9	DDR1_A7	DDR1_A5	DDR1_A3	DDR1_A1	DDR1_DQ10	DDR1_DQ12	DDR1_DQ13	DDR1_DQ14	DDR1_DQ1	DDR1_DQ3	DDR1_DQ5	DDR1_DQ6	DDR1_DQ16	DDR1_DQ18	DDR1_DQ20	DDR1_DQ23	DDR1_DQ24	DDR1_DQ26	DDR1_DQ27	DDR1_DQ29	VSS_2	EDP_AUXN	EDP_TX0N	EDP_TX1N	VSS_3	A
B	DDR0_CSN1	DDR1_BA0	DDR1_CSN3	DDR1_A13	VSS_24	DDR1_A8	DDR1_A6	DDR1_A4	DDR1_A2	DDR1_A0	DDR1_DQ8	DDR1_DQ9	DDR1_DQ11	DDR1_DQ15	DDR1_DQ0	DDR1_DQ2	DDR1_DQ4	DDR1_DQ7	DDR1_DQ17	DDR1_DQ19	DDR1_DQ21	DDR1_DQ22	DDR1_DQ25	DDR1_DQ28	DDR1_DQ30	DDR1_DQ31	GPIO3_B7/MAC_CRS/UART3_TX/CIF_CLKOUTB	EDP_AUXP	EDP_TX0P	EDP_TX1P	EDP_AVSS_1	B
C	DDR0_A12	DDR0_CSN3	DDR0_BA0	DDR1_A14	DDR1_A11	DDR1_RASN		VSS_25	VSS_26		VSS_27	VSS_28		VSS_29	VSS_30		VSS_31	VSS_32		VSS_33	VSS_34		VSS_35	VSS_36		VSS_37	GPIO3_B1/MAC_RXDV	EDP_AVSS_2	EDP_AVSS_3	EDP_TX2P	EDP_TX2N	C
D	DDR0_A10	DDR0_A13	DDR0_A14		VSS_38	DDR1_BA1		DDR1_CLK0N	DDR1_CLK0P		DDR1_0D10	DDR1_BA2		DDR1_DQS1N	DDR1_DQS1P		DDR1_DQS0N	DDR1_DQS0P		DDR1_DQS2N	DDR1_DQS2P		DDR1_DQS3N	DDR1_DQS3P		GPIO3_A4/MAC_TXD0/SPI0_RXD	GPIO3_C0/MAC_COL/UART3_CTSN/SPI0_TX		EDP_AVSS_4	EDP_TX3P	EDP_TX3N	D
E	DDR0_CKE0	VSS_39	DDR0_A11	VSS_40		DDR1_CKE1	VSS_41	DDR1_CLK1N	DDR1_CLK1P		DDR1_ODT1	VSS_42		DDR1_DM1	VSS_43		DDR1_DM0	VSS_44		DDR1_DM2	VSS_45		DDR1_DM3	VSS_46	GPIO3_A3/MAC_RXD3/SPI4_CSN0	GPIO3_A6/MAC_RXD0/SPI0_CLK		GPIO3_C1/MAC_TXCLK/UART3_RTSN	GPIO3_B0/MAC_MDC/SPI0_CSN1	GPIO3_A2/MAC_RXD2/SPI4_CLK	VSS_47	E
F	DDR0_A1	DDR0_A0	DDR0_RASN	DDR0_BA1	DDR0_CKE1		DDR1_WEN	VSS_48	DDR1_CASN		DDR1_CSN2	DDR1_CSN0		DDR1_PLL_TESTOUT_P	VSS_49		DDR1_ATB0	VSS_50		VSS_51	VSS_52		GPIO3_B2/MAC_RXCLK/SPI4_CS5_SDA	GPIO3_A0/MAC_TX2D2/SPI4_RXD	GPIO3_B6/MAC_RXCLK/UART3_RX		GPIO3_A7/MAC_RXD1/SPI0_CSN0	GPIO2_A3/VOP_DO_CIF_D3	GPIO2_A5/VOP_DS_CIF_D5	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA	GPIO2_B4/SPI2_CSN0	F
G	DDR0_A2	DDR0_A3			VSS_53	DDR0_WEN		DDR1_A15	VSS_54		DDR1_RESETN	DDR1_CLK_VDD		DDR1_PLL_TESTOUT_N	DDR1_PZQ		DDR1_ATB1	VSS_55		EDP_DC_TP	EDP_REXT		GPIO3_A5/MAC_TXD0/SPI0_TXD	GPIO3_B3/MAC_AC_CLK/I2C5_SCL		GPIO3_B5/MAC_MDIO/UART1_TX	VSS_56			GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA	G
H	DDR0_A5	DDR0_A4	VSS_57	DDR0_CLK0P	DDR0_CLK1P	DDR0_CASN	DDR0_A15		VSS_58	VSS_59	VSS_60	VSS_61	VSS_62	DDR1PLL_AVDD_0V9	VSS_63	VSS_64	VSS_65	VSS_66	EDP_AVSS_5	EDP_AVDD_0V9	EDP_CLK24M_IN	GPIO3_B4/MAC_TXEN/UART1_RX	GPIO3_A1/MAC_TXD3/SPI4_TXD	GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C8_SCL	GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL	VSS_67	GPIO2_A6/VOP_D6/CIF_D6	GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	GPIO2_A4/VOP_D4/CIF_D4	GPIO2_A2/VOP_D2/CIF_D2	GPIO2_B3/SPI2_CLK/VOP_DEN/CIF_CLKOUTA	H
J	DDR0_A6	DDR0_A7	VSS_68	DDR0_CLK0N	DDR0_CLK1N	VSS_69	VSS_70	VSS_71	VSS_72	VSS_73	DDR1_VDD_1	DDR1_VDD_2	DDR1_VDD_3	DDR1_VDD_4	DDR1_VDD_5	DDR1_VDD_6	DDR1_VDD_7	DDR1_VDD_8	EDP_AVDD_1V8_1	EDP_AVDD_1V8_2	EDP_AVSS_6	APIO1_VDDPST	APIO2_VDDPST	APIO2_VDDPST	EMMC_D3	EMMC_D4	EMMC_D5	EMMC_D0	EMMC_D1	EMMC_D2	EMMC_CMD	J
K	DDR0_A9	DDR0_A8						VSS_74	VSS_75	VSS_76	DDR1_VDD_9	VSS_77	DDR1_VDD_10	VSS_78	DDR1_VDD_11	VSS_79	DDR1_VDD_12	VSS_80	BIGCPU_VDD_12	VSS_82	BIGCPU_VDD_13	VSS_84	APIO2_VDD	EMMC_VDD_1V8							EMMC_D7	EMMC_STRB	K
L	DDR0_DQ29	DDR0_DQ31	VSS_85	DDR0_ODT0	DDR0_ODT1	VSS_86	DDR0_RESETN	VSS_87	DDR0_VDD_1	DDR0_VDD_2	VSS_88	VSS_89	VSS_90	VSS_91	VSS_92	VSS_93	LOGIC_VDD_10	BIGCPU_VDD_8	BIGCPU_VDD_1	VSS_96	BIGCPU_VDD_2	VSS_97	BIGCPU_VDD_11	EMMC_CORE DLL_0V9	GPIO1_C6/ITCPD_VBUS_SOURCE0	GPIO1_D0/TCPD_VBUS_SOURCE2	VSS_99	EMMC_CLK	EMMC_CALI0	EMMC_TP	EMMC_D6	L
M	DDR0_DQ27	DDR0_DQ30	VSS_100	DDR0_BA2	DDR0_CSN2	DDR0_CSN0	DDR0_CLK_VDD	VSS_101	DDR0_VDD_3	VSS_102	CENTERLOGIC_VDD_1	CENTERLOGIC_VDD_2	CENTERLOGIC_VDD_3	CENTERLOGIC_VDD_4	CENTERLOGIC_VDD_5	VSS_103	LOGIC_VDD_9	BIGCPU_VDD_3	BIGCPU_VDD_4	BIGCPU_VDD_5	BIGCPU_VDD_6	BIGCPU_VDD_7	VSS_104	GPIO1_B5	GPIO1_B6/PWM3B_IR	GPIO1_B7/SPI3_RXD/I2C9_SDA	GPIO1_C1/SPI3_CLK	GPIO1_C3/PWM2	GPIO1_C4/I2C8_SDA	GPIO1_C5/I2C8_SCL	GPIO1_C7/TCPD_VBUS_SOURCE1	M
N	DDR0_DQ26	DDR0_DQ28						VSS_105	DDR0_VDD_4	DDR0_VDD_5	CENTERLOGIC_VDD_6	CENTERLOGIC_VDD_7	VSS_108	VSS_109	VSS_110	VSS_111	VSS_94	BIGCPU_VDD_COM	VSS_83	BIGCPU_VDD_10	VSS_98	BIGCPU_VDD_9	PMUIO2_VDDPST	GPIO9_A2/WIFI_26MHZ							GPIO1_C0/SPI3_TXD/I2C0_SCL	GPIO1_C2/SPI3_CSN0	N
P	DDR0_DQ24	DDR0_DQ25	VSS_112	DDR0_DQS3P	DDR0_DM3	VSS_113	VSS_114	VSS_115	DDR0_VDD_6	VSS_116	VSS_106	VSS_107	CENTERLOGIC_VDD_8	CENTERLOGIC_VDD_9	CENTERLOGIC_VDD_10	VSS_117	PLL_AVSS	PLL_AVDD_1V8	VSS_119	LITCPU_VDD_1	VSS_121	LITCPU_VDD_4	PMUIO2_VDD	GPIO0_B5/TCPD_VBUS_FDIS/TCPD_VBUS_SOURCE3	GPIO0_A6/PWM3A_IR	GPIO1_A6/IS ADC_INT	GPIO1_A7/SPI1_RXD/UART4_RX	GPIO1_B1/SPI1_CLK/PMU_JTAG_TC	GPIO1_B2/SPI1_CSN0/PMU_JTAG_TMS	GPIO1_B4/I2C4_SCL	GPIO1_B3/I2C4_SDA	P
R	DDR0_DQ23	DDR0_DQ22	VSS_123	DDR0_DQS3N	VSS_124	VSS_125	DDR0_PZQ	DDRPLL_AVDD_0V9	DDR0_VDD_7	DDR0_VDD_8	GPU_VDD_8	GPU_VDD_9	GPU_VDD_13	VSS_129	VSS_130	VSS_131	PLL_AVDD_0V9	VSS_165	LITCPU_VDD_2	LITCPU_VDD_3	VSS_120	LITCPU_VDD_7	VSS_133	PMUIO1_VDD_1V8	GPIO1_A0/ISP0_SHUTTER_EN/ISP1_SHUTTER_LN/TCPD_VBUS_S	GPIO1_A2/ISP0_FLASHTRIGOUT/ISP1_FLASHTRIGOUT/TCPD_CC1_VC	GPIO1_A3/ISP0_FLASHTRIGOUT/ISP1_FLASHTRIGOUT	GPIO1_A4/ISP0_PRELIGHT_TRIG/ISP1_PRELIGHT_TRIG	GPIO0_A1/DDRIO_PWRO FF/TCPD_CC DB_EN	GPIO1_A5/APWRONF#	GPIO1_B0/SPI1_TXD/IAR4_TX	R
T	DDR0_DQ20	DDR0_DQ21						VSS_134	DDR0_VDD_9	VSS_135	GPU_VDD_10	GPU_VDD_11	GPU_VDD_12	GPU_VDD_14	GPU_VDD_17	VSS_138	LOGIC_VDD_11	VSS_168	VSS_122	LITCPU_VDD_6	VSS_139	LITCPU_VDD_5	SDMMC0_VDD	PMU_VDD_0V9							NPOR	GPIO1_A1/ISP0_SHUTTER_TRIG/ISP1_SHUTTER_TRIG/TCPD_C	T
U	DDR0_DQ18	DDR0_DQ19	VSS_141	DDR0_DQS2P	DDR0_DM2	DDR0_ATB1	DDR0_ATB0	VSS_142	DDR0_VDD_10	DDR0_VDD_11	VSS_126	VSS_127	GPU_VDD_7	VSS_137	VSS_143	VSS_144	LOGIC_VDD_8	LOGIC_VDD_7	VSS_146	LOGIC_VDD_12	VSS_147	VSS_149	AVSS_49	USB_AVDD_1V8	PMU_VDD_1V8	SDMMC0_VDDPST	GPIO4_B3/SDMMC0_D3	GPIO0_B0/SDMMC0_WRPRI/TEST_CLKOUT2	VSS_150	GPIO0_B3	GPIO0_A0/TEST_CLKOUT0/CLK32K_IN	U
V	DDR0_DQ16	DDR0_DQ17	VSS_151	DDR0_DQS2N	VSS_152	DDR0_PLL_TESTOUT_P	DDR0_PLL_TESTOUT_N	VSS_153	DDR0_VDD_12	VSS_154	GPU_VDD_15	GPU_VDD_16	GPU_VDD_6	GPU_VDD_5	GPU_VDD_4	GPU_VDD_COM	VSS_148	LOGIC_VDD_5	LOGIC_VDD_4	LOGIC_VDD_3	LOGIC_VDD_2	LOGIC_VDD_1	AVSS_50	USB_AVDD_0V9	GPIO4_B5/SDMMC0_CMD/MCU/TAG_TMS	GPIO0_B4/TCPD_VBUS_BDIS	GPIO0_A5/EMMC_PWRON	GPIO0_A7/SDMMC0_DET	GPIO4_B4/SDMMC0_CLK OUT/MCU/TAG_TCK	GPIO0_B1/PMUIO2_VDLSEL	GPIO0_A3/SDIO0_WRPT	V
W	DDR0_DQ6	DDR0_DQ7						VSS_161	VSS_162	GPU_VDD_20	GPU_VDD_1	GPU_VDD_2	VSS_128	GPU_VDD_3	GPU_VDD_19	GPU_VDD_18	VSS_159	AVSS_1	VSS_167	LOGIC_VDD_6	VSS_81	VSS_158	AVSS_60	PCIE_AVDD_0V9							VSS_160	GPIO0_B2	W
Y	DDR0_DQ5	DDR0_DQ4	VSS_8	DDR0_DQS0P	DDR0_DM0	GPIO4_A2/I2C1_SCL	GPIO3_D3/I2S0_SDI0	APIO5_VDD	VSS_166	VSS_15	VSS_155	VSS_136	VSS_164	VSS_156	VSS_157	VSS_118	VSS_95	TYPEC0_AVDD_0V9_2	TYPEC0_AVDD_0V9_1	AVSS_2	TYPEC1_AVDD_0V9_1	AVSS_3	TYPEC1_AVDD_0V9_2	PCIE_AVDD_1V8	USB_AVDD_3V3	GPIO4_B1/SDMMC0_D1/UART2A_TX	GPIO4_B0/SDMMC0_D0/UART2A_RX	GPIO4_B2/SDMMC0_D2	AVSS_59	XOUT_OSC	XIN_OSC	Y
AA	DDR0_DQ3	DDR0_DQ2	VSS_4	DDR0_DQS0N	VSS_5	GPIO3_D5/I2S0_SDI2SDO2	GPIO4_A4/I2S1_LRCK_RX	APIO5_VDDPST	VSS_6	VSS_10	VSS_11	VSS_163	VSS_12	VSS_132	VSS_13	VSS_145	VSS_140	TYPEC0_AVDD_1V8	NC_8	NC_9	TYPEC1_AVDD_1V8	NC_11	AVSS_4	DFT_JTAG_TMS	GPIO0_A4/SDIO0_INTN	AVSS_6	PCIE_TX2_P	PCIE_TX2_N	AVSS_7	USB1_DP	USB1_DN	AA
AB	DDR0_DQ1	DDR0_DQ0						APIO3_VDD_1V8	VSS_9	VSS_7	AVSS_8	MIPI_TX0_AVDD_1V8	AVSS_9	MIPI_RX0_AVDD_1V8	HDMI_AVDD_0V9_1	VSS_14	AVSS_51	TYPEC0_AVDD_3V3	AVSS_52	NC_10	TYPEC1_AVDD_3V3	NC_12	AVSS_5	DFT_JTAG_TRSTN							USB0_DP	USB0_DN	AB
AC	DDR0_DQ14	DDR0_DQ15	VSS_16	DDR0_DQS1P	DDR0_DM1	GPIO4_A7/I2S1_SDO0	GPIO4_A0/I2S_CLK	APIO4_VDDPST	APIO4_VDD	MIPI_TX1/RX1_AVDD_1V8	AVSS_57	NC_14	AVSS_58	NC_13	HDMI_AVDD_0V9_2	AVSS_10	NC_7	AVSS_11	TYPEC1_U3VBUSDET	AVSS_12	AVSS_13	AVSS_53	ADC_AVDD	AVSS_19	AVSS_55	AVSS_14	PCIE_RX2_P	PCIE_RX2_N	AVSS_15	USB1_RBIAS	USB0_RBIAS	AC
AD	DDR0_DQ13	DDR0_DQ11	VSS_17	DDR0_DQS1N	VSS_18	GPIO4_A6/I2S1_SDI0	GPIO4_C7/HDMI_CECINOUT/EDP_HOTPLUG	GPIO2_C4/SDIO0_D0/SPI5_RXD	GPIO2_D3/SDIO0_PWREN	VSS_19	NC_2	NC_3	NC_4	NC_5	NC_6	NC_15	AVSS_16	TYPEC0_RCLKM	TYPEC0_U3VBUSDET	TYPEC1_RCLKM	AVSS_17	AVSS_18	EFUSE	USIC_AVDD_1V2	USIC_AVDD_0V9	AVSS_54	PCIE_TX3_P	PCIE_TX3_N	AVSS_20	PCIE_RCLK_100M_N	PCIE_RCLK_100M_P	AD
AE	DDR0_DQ12	DDR0_DQ9			GPIO3_D4/I2S0_SDI1SDO3	GPIO4_D0/PCIE_CLKREQNB		GPIO2_C7/SDIO0_D3/SPI5_CSN0	GPIO2_C0/UART0_RX		AVSS_21	AVSS_22		AVSS_23	HDMI_HPD		AVSS_24	TYPEC0_RCLKP		TYPEC1_RCLKP	NC_1		NC_16	TYPEC1_AUXP_PD_PU		TYPEC1_ID	AVSS_25			PCIE_TX0_P	PCIE_TX0_N	AE
AF	DDR0_DQ10	DDR0_DQ8	GPIO4_A3/I2S1_SCLK	GPIO3_D1/I2S0_LRCK_RX	GPIO4_C2/PWM0/VOP0_PWM/VOP1_PWM		GPIO2_D1/SDIO0_CLKOUT/TEST_CLKOUT1	GPIO2_D4/SDIO0_BKPWR	VSS_20		MIPI_TX1/RX1_REXT	MIPI_TX0_REXT		MIPI_RX0_REXT	HDMI_REXT		HDMI_AVDD_1V8	AVSS_26		AVSS_27	TYPEC1_CC2		TYPEC1_REXT	TYPEC1_AUXM_PU_PD	AVSS_56		PCIE_RX3_P	PCIE_RX3_N	AVSS_28	PCIE_RX0_P	PCIE_RX0_N	AF
AG	GPIO4_A1/I2C1_SDA	VSS_21	GPIO3_D0/I2S0_SCLK	GPIO4_D6		GPIO4_C0/I2C3_SDA/UART2B_RX	GPIO2_C6/SDIO0_D2/SPI5_CLK	GPIO2_C2/UART0_CTSN	MIPI_TX0_D_3P		MIPI_TX0_D_2P	MIPI_TX0_C_LKP		MIPI_TX0_D_1P	MIPI_TX0_D_0P		TYPEC0_AUXM_PU_PD	TYPEC0_REXT		TYPEC0_REXT_CC	TYPEC1_REXT_CC		TYPEC0_DP	TYPEC1_DP	ADC_IN2	ADC_IN0		ADC_IN3	AVSS_29	PCIE_TX1_P	PCIE_TX1_N	AG
AH	GPIO3_D7/I2S0_SDO0	GPIO3_D6/I2S0_SDI3SDO1	GPIO4_D2		GPIO4_D4	GPIO2_D0/SDIO0_CMD		GPIO2_C1/UART0_TX	MIPI_TX0_D_3N		MIPI_TX0_D_2N	MIPI_TX0_C_LKN		MIPI_TX0_D_1N	MIPI_TX0_D_0N		TYPEC0_AUXP_PD_PU	TYPEC0_CC1		TYPEC0_CC2	TYPEC1_CC1		TYPEC0_DN	TYPEC1_DN		ADC_IN1	ADC_IN4		AVSS_30	PCIE_RX1_P	PCIE_RX1_N	AH
AJ	GPIO4_A5/I2S1_LRCK_TX	GPIO3_D2/I2S0_LRCK_TX	GPIO4_D5	GPIO4_C4/UART2C_TX	VSS_22	AVSS_31		AVSS_32	AVSS_33		AVSS_34	AVSS_35		AVSS_36	AVSS_37		AVSS_38	AVSS_39		AVSS_40	AVSS_41		AVSS_42	AVSS_43		AVSS_44	AVSS_45	AVSS_46	AVSS_47	USIC_STROBE	USIC_DATA	AJ
AK	GPIO4_C5/SPDIF_TX	GPIO4_C3/UART2C_RX	GPIO4_D3	GPIO4_D1/DP_HOTPLUG	GPIO2_C5/SDIO0_D1/SPI5_TXD	MIPI_TX1/RX1_D0P	MIPI_TX1/RX1_D1P	MIPI_TX1/RX1_CLKP	MIPI_TX1/RX1_D2P	MIPI_TX1/RX1_D3P	MIPI_RX0_D_3P	MIPI_RX0_D_2P	MIPI_RX0_C_LKP	MIPI_RX0_D_1P	MIPI_RX0_D_0P	HDMI_TCP	HDMI_TX0P	HDMI_TX1P	HDMI_TX2P	TYPEC0_AUXP	TYPEC0_RX1P	TYPEC0_TX1M	TYPEC0_RX2P	TYPEC0_TX2M	TYPEC1_RX1P	TYPEC1_TX1M	TYPEC1_RX2P	TYPEC1_TX2M	TYPEC1_AUXP	TYPEC0_U2VBUSDET	TYPEC1_U2VBUSDET	AK
AL	VSS_23	GPIO4_C1/I2C3_SCL/UART2B_TX	GPIO4_C6/PWM1	GPIO2_D2/SDIO0_DETN/PCIE_CLKREQN	GPIO2_C3/UART0_RTSN	MIPI_TX1/RX1_D0N	MIPI_TX1/RX1_D1N	MIPI_TX1/RX1_CLKN	MIPI_TX1/RX1_D2N	MIPI_TX1/RX1_D3N	MIPI_RX0_D_3N	MIPI_RX0_D_2N	MIPI_RX0_C_LKN	MIPI_RX0_D_1N	MIPI_RX0_D_0N	HDMI_TCN	HDMI_TX0N	HDMI_TX1N	HDMI_TX2N	TYPEC0_AUXM	TYPEC0_RX1M	TYPEC0_TX1P	TYPEC0_RX2M	TYPEC0_TX2P	TYPEC1_RX1M	TYPEC1_TX1P	TYPEC1_RX2M	TYPEC1_TX2P	TYPEC1_AUXM	TYPEC0_ID	AVSS_48	AL
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

Figure 2-5 RK3399 Ball Map

2.2 Ball Pin List

2.2.1 Function Pin Descriptions

Table 2-2 RK3399 Function Pin Descriptions

	Pin Name	Function 1	Function 2	Function 3	Function 4	Type	Def	PD/PU	Default	INT
PMUIO1（1.8V only）										
Y31	XIN_OSC					I	I			
Y30	XOUT_OSC					O	O			
T30	NPOR					I	I	up		
U31	GPIO0_A0/TESTCLKOUT0/CLK32K_IN	gpio0_a[0]	testclkout0	clk32k_in		I/O	I	up	5mA	√
R29	GPIO0_A1/DDRIO_PWROFF/TCPD_CCDB_EN	gpio0_a[1]	ddrio_pwroff	tcpd_ccdb_en		I/O	I	up	5mA	√
N24	GPIO0_A2/WIFI_26MHZ	gpio0_a[2]	wifi_26m			I/O	I	down	5mA	√
V31	GPIO0_A3/SDIO0_WRPT	gpio0_a[3]	sdio0_wrpt			I/O	I	down	5mA	√
AA25	GPIO0_A4/SDIO0_INTN	gpio0_a[4]	sdio0_intn			I/O	I	down	5mA	√
V27	GPIO0_A5/EMMC_PWRON	gpio0_a[5]	emmc_pwren			I/O	I	up	5mA	√
P25	GPIO0_A6/PWMA3_IR	gpio0_a[6]	pwma3_ir			I/O	I	down	5mA	√
V28	GPIO0_A7/SDMMC0_DET	gpio0_a[7]	sdmmc0_dectn			I/O	I	up	5mA	√
U28	GPIO0_B0/SDMMC0_WRPRT/TEST_CLKOUT2	gpio0_b[0]	sdmmc0_wrprt	test_clkout2		I/O	I	up	5mA	√
V30	GPIO0_B1/PMUIO2_1833_VOLSEL	gpio0_b[1]	pmuio2_1833_volsel			I/O				
	GPIO0_B2					I/O	I	down	5mA	√

U30	GPIO0_B3	gpio0_b[3]				I/O	I	down	5mA	√
V26	GPIO0_B4/TCPD_VBUS_BDIS	gpio0_b[4]	tcpd_vbus_bdis			I/O	I	down	5mA	√
P24	GPIO0_B5/TCPD_VBUS_FDIS/TCPD_VBUS_SOURCE3	gpio0_b[5]	tcpd_vbus_fdis	tcpd_vbus_source3		I/O	I	down	5mA	√
PMUIO2（1.8V OR 3.0V）										
R25	GPIO1_A0/ISP_SHUTTER_EN/TCPD_VBUS_SINK_EN	gpio1_a[0]	isp0_shutter_en	isp1_shutter_en	tcpd_vbus_sink_en	I/O	I	down	3mA	√
T31	GPIO1_A1/ISP_SHUTTER_TRIG/TCPD_CC0_VCONN_EN	gpio1_a[1]	isp0_shutter_trig	isp1_shutter_trig	tcpd_cc0_vconn_en	I/O	I	down	3mA	√
R26	GPIO1_A2/ISP_FLASHTRIGIN/TCPD_CC1_VCONN_EN	gpio1_a[2]	isp0_flashtrigin	isp1_flashtrigin	tcpd_cc1_vconn_en	I/O	I	down	3mA	√
R27	GPIO1_A3/ISP_FLASHTRIGOUT	gpio1_a[3]	isp0_flashtrigout	isp1_flashtrigout		I/O	I	down	3mA	√
R28	GPIO1_A4/ISP_PRELIGHT_TRIG	gpio1_a[4]	isp0_prelight_trig	isp1_prelight_trig		I/O	I	down	3mA	√
R30	GPIO1_A5/AP_PWROFF	gpio1_a[5]	ap_pwroff			I/O	I	down	3mA	√
P26	GPIO1_A6/TSADC_INT	gpio1_a[6]	tsadc_int			I/O	I	high-z	3mA	√
P27	GPIO1_A7/PMCU_UART4DBG_RX/SPI1_RXD	gpio1_a[7]	pmcu_uart4dbg_rx	spi1_rxd		I/O	I	up	6mA	√
R31	GPIO1_B0/PMCU_UART4DBG_TX/SPI1_TXD	gpio1_b[0]	pmcu_uart4dbg_tx	spi1_txd		I/O	I	up	6mA	√
P28	GPIO1_B1/SPI1_CLK/PMCU_JTAG_TCK	gpio1_b[1]	pmcu_jtag_tck	spi1_clk		I/O	I	up	6mA	√
P29	GPIO1_B2/SPI1_CSN0/PMCU_JTAG_TMS	gpio1_b[2]	pmcu_jtag_tms	spi1_csn0		I/O	I	up	6mA	√
P31	GPIO1_B3/I2C4_SDA	gpio1_b[3]	i2c4_sda				I	up	3mA	√
P30	GPIO1_B4/I2C4_SCL	gpio1_b[4]	i2c4_scl				I	up	3mA	√
M24	GPIO1_B5	gpio1_b[5]					I	down	3mA	√
M25	GPIO1_B6/PWMB3_IR	gpio1_b[6]	pwmb3_ir				I/O	down	3mA	√
M26	GPIO1_B7/SPI3_RXD/I2C0_SDA	gpio1_b[7]	spi3_rxd	i2c0_sda			I/O	up	3mA	√
N30	GPIO1_C0/SPI3_TXD/I2C0_SCL	gpio1_c[0]	spi3_txd	i2c0_scl			I/O	up	3mA	√
M27	GPIO1_C1/SPI3_CLK	gpio1_c[1]	spi3_clk			I/O	I	down	3mA	√
N31	GPIO1_C2/SPI3_CSN0	gpio1_c[2]	spi3_csn0			I/O	I	up	3mA	√
M28	GPIO1_C3/PWM2	gpio1_c[3]	pwm2			I/O	I	down	3mA	√

M29	GPIO1_C4/I2C8_SDA	gpio1_c[4]	i2c8_sda			I/O	I	up	3mA	√
M30	GPIO1_C5/I2C8_SCL	gpio1_c[5]	i2c8_scl			I/O	I	up	3mA	√
L25	GPIO1_C6/DFTJTAG_TDI/TCPD_VBUS_SOURCE0	gpio1_c[6]	dftjtag_tdi	tcpd_vbus_source0		I/O	I	down	6mA	√
M31	GPIO1_C7/DFTJTAG_TDO/TCPD_VBUS_SOURCE1	gpio1_c[7]	dftjtag_tdo	tcpd_vbus_source1		I/O	I	down	6mA	√
L26	GPIO1_D0/DFTJTAG_CLK/TCPD_VBUS_SOURCE2	gpio1_d[0]	dftjtag_clk	tcpd_vbus_source2		I/O	I	down	6mA	√
AA24	TESTJTAG_TMS	Testjtag_tms						Fup		
AB24	TESTTAG_TRSTN	Testjtag_trstn						Fdown		
APIO2 (1.8V OR 3.0V)										
G31	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA	gpio2_a[0]	vop_data[0]	io_cif_data0	i2c2_sda	I/O	I	up	3mA	√
H25	GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL	gpio2_a[1]	vop_data[1]	io_cif_data1	i2c2_scl	I/O	I	up	3mA	√
H30	GPIO2_A2/VOP_D2/CIF_D2	gpio2_a[2]	vop_data[2]	io_cif_data2		I/O	I	down	3mA	√
F28	GPIO2_A3/VOP_D3/CIF_D3	gpio2_a[3]	vop_data[3]	io_cif_data3		I/O	I	down	3mA	√
H29	GPIO2_A4/VOP_D4/CIF_D4	gpio2_a[4]	vop_data[4]	io_cif_data4		I/O	I	down	3mA	√
F29	GPIO2_A5/VOP_D5/CIF_D5	gpio2_a[5]	vop_data[5]	io_cif_data5		I/O	I	down	3mA	√
H27	GPIO2_A6/VOP_D6/CIF_D6	gpio2_a[6]	vop_data[6]	io_cif_data6		I/O	I	down	3mA	√
G30	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA	gpio2_a[7]	vop_data[7]	io_cif_data7	i2c7_sda	I/O	I	up	3mA	√
H28	GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	gpio2_b[0]	vop_clk	io_cif_vsync	i2c7_scl	I/O	I	up	3mA	√
F30	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA	gpio2_b[1]	spi2_rxd	io_cif_href	i2c6_sda	I/O	I	up	3mA	√
H24	GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL	gpio2_b[2]	spi2_txd	io_cif_clkin	i2c6_scl	I/O	I	up	3mA	√
H31	GPIO2_B3/SPI2_CLK/VOP_DEN/CIF_CLKOUT	gpio2_b[3]	spi2_clk	io_cif_clkout	vop_den	I/O	I	up	3mA	√
F31	GPIO2_B4/SPI2_CSN0	gpio2_b[4]	spi2_csn0			I/O	I	up	3mA	√
APIO3 (1.8V only)										
AE9	GPIO2_C0/UART0_RX	gpio2_c[0]	uart0_rx			I/O	I	up	5mA	√
AH8	GPIO2_C1/UART0_TX	gpio2_c[1]	uart0_tx			I/O	I	up	5mA	√
AG8	GPIO2_C2/UART0_CTSN	gpio2_c[2]	uart0_ctsn			I/O	I	up	5mA	√
AL5	GPIO2_C3/UART0_RTSN	gpio2_c[3]	uart0_rtsn			I/O	I	up	5mA	√

AD8	GPIO2_C4/SDIO0_D0/SPI5_RXD	gpio2_c[4]	sdio0_data0	spi5_rxd		I/O	I	up	5mA	√
AK5	GPIO2_C5/SDIO0_D1/SPI5_TXD	gpio2_c[5]	sdio0_data1	spi5_txd		I/O	I	up	5mA	√
AG7	GPIO2_C6/SDIO0_D2/SPI5_CLK	gpio2_c[6]	sdio0_data2	spi5_clk		I/O	I	up	5mA	√
AE8	GPIO2_C7/SDIO0_D3/SPI5_CSN0	gpio2_c[7]	sdio0_data3	spi5_csn0		I/O	I	up	5mA	√
AH6	GPIO2_D0/SDIO0_CMD	gpio2_d[0]	sdio0_cmd			I/O	I	up	5mA	√
AF7	GPIO2_D1/SDIO0_CLKOUT/TEST_CLKOUT1	gpio2_d[1]	sdio0_clkout	test_clkout1		I/O	I	up	5mA	√
AL4	GPIO2_D2/SDIO0_DETN/PCIE_CLKREQN	gpio2_d[2]	sdio0_detect_n	pcie_clkreqn		I/O	I	up	5mA	√
AD9	GPIO2_D3/SDIO0_PWREN	gpio2_d[3]	sdio0_pwren			I/O	I	down	5mA	√
AF8	GPIO2_D4/SDIO0_BKPWR	gpio2_d[4]	sdio0_bkpwr			I/O	I	down	5mA	√
APIO1 (3.3V ONLY)										
F24	GPIO3_A0/MAC_TXD2/SPI4_RXD	gpio3_a[0]	mac_txd2	spi4_rxd	trace_data12	I/O	I	down	4mA	√
H23	GPIO3_A1/MAC_TXD3/SPI4_TXD	gpio3_a[1]	mac_txd3	spi4_txd	trace_data13	I/O	I	down	4mA	√
E30	GPIO3_A2/MAC_RXD2/SPI4_CLK	gpio3_a[2]	mac_rxd2	spi4_clk	trace_data14	I/O	I	up	4mA	√
E25	GPIO3_A3/MAC_RXD3/SPI4_CSN0	gpio3_a[3]	mac_rxd3	spi4_csn0	trace_data15	I/O	I	up	4mA	√
D26	GPIO3_A4/MAC_TXD0/SPI0_RXD	gpio3_a[4]	mac_txd0	spi0_rxd		I/O	I	down	4mA	√
G23	GPIO3_A5/MAC_TXD1/SPI0_TXD	gpio3_a[5]	mac_txd1	spi0_txd		I/O	I	down	4mA	√
E26	GPIO3_A6/MAC_RXD0/SPI0_CLK	gpio3_a[6]	mac_rxd0	spi0_clk		I/O	I	up	4mA	√
F27	GPIO3_A7/MAC_RXD1/SPI0_CSN0	gpio3_a[7]	mac_rxd1	spi0_csn0		I/O	I	up	4mA	√
E29	GPIO3_B0/MAC_MDC/SPI0_CSN1	gpio3_b[0]	mac_mdc	spi0_csn1		I/O	I	up	4mA	√
C27	GPIO3_B1/MAC_RXDV	gpio3_b[1]	mac_rxdv			I/O	I	down	4mA	√
F23	GPIO3_B2/MAC_RXER/I2C5_SDA	gpio3_b[2]	mac_rxer	i2c5_sda		I/O	I	up	4mA	√
G24	GPIO3_B3/MAC_CLK/I2C5_SCL	gpio3_b[3]	mac_clk	i2c5_scl		I/O	I	up	4mA	√
H22	GPIO3_B4/MAC_TXEN/UART1_RX	gpio3_b[4]	mac_txen	uart1_rx		I/O	I	up	4mA	√
G26	GPIO3_B5/MAC_MDIO/UART1_TX	gpio3_b[5]	mac_mdio	uart1_tx		I/O	I	up	4mA	√
F25	GPIO3_B6/MAC_RXCLK/UART3_RX	gpio3_b[6]	mac_rxclk	uart3_rx		I/O	I	up	4mA	√
B27	GPIO3_B7/MAC_CRS/UART3_TX/CIF_CLKOUTB	gpio3_b[7]	mac_crs	uart3_tx	cif_clkoutb	I/O	I	up	4mA	√
D27	GPIO3_C0/MAC_COL/UART3_CTSN/SPDIF_	gpio3_c[0]	mac_col	uart3_ctsn	spdif_tx	I/O	I	up	4mA	√

	TX									
E28	GPIO3_C1/MAC_TXCLK/UART3_RTSN	gpio3_c[1]	mac_txclk	uart3_rtsn		I/O	I	up	4mA	√
APIO5 (1.8V OR 3V)										
AG3	GPIO3_D0/I2S0_SCLK	gpio3_d[0]	i2s0_sclk	trace_data0		I/O	I	down	3mA	√
AF4	GPIO3_D1/I2S0_LRCK_RX	gpio3_d[1]	i2s0_lrck_rx	trace_data1		I/O	I	down	3mA	√
AJ2	GPIO3_D2/I2S0_LRCK_TX	gpio3_d[2]	i2s0_lrck_tx	trace_data2		I/O	I	down	3mA	√
Y7	GPIO3_D3/I2S0_SDI0	gpio3_d[3]	i2s0_sdi0	trace_data3		I/O	I	down	3mA	√
AE5	GPIO3_D4/I2S0_SDI1SDO3	gpio3_d[4]	i2s0_sdi1sdo3	trace_data4		I/O	I	down	3mA	√
AA6	GPIO3_D5/I2S0_SDI2SDO2	gpio3_d[5]	i2s0_sdi2sdo2	trace_data5		I/O	I	down	3mA	√
AH2	GPIO3_D6/I2S0_SDI3SDO1	gpio3_d[6]	i2s0_sdi3sdo1	trace_data6		I/O	I	down	3mA	√
AH1	GPIO3_D7/I2S0_SDO0	gpio3_d[7]	i2s0_sdo0	trace_data7		I/O	I	down	3mA	√
AC7	GPIO4_A0/I2S_CLK	gpio4_a[0]	i2s_clk	trace_ctl		I/O	I	down	3mA	√
AG1	GPIO4_A1/I2C1_SDA	gpio4_a[1]	i2c1_sda	trace_clk		I/O	I	up	3mA	√
Y6	GPIO4_A2/I2C1_SCL	gpio4_a[2]	i2c1_scl	trace_data8		I/O	I	up	3mA	√
AF3	GPIO4_A3/I2S1_SCLK	gpio4_a[3]	i2s1_sclk	trace_data9		I/O	I	down	3mA	√
AA7	GPIO4_A4/I2S1_LRCK_RX	gpio4_a[4]	i2s1_lrck_rx	trace_data10		I/O	I	down	3mA	√
AJ1	GPIO4_A5/I2S1_LRCK_TX	gpio4_a[5]	i2s1_lrck_tx	trace_data11		I/O	I	down	3mA	√
AD6	GPIO4_A6/I2S1_SDI0	gpio4_a[6]	i2s1_sdi0			I/O	I	down	3mA	√
AC6	GPIO4_A7/I2S1_SDO0	gpio4_a[7]	i2s1_sdo0			I/O	I	down	3mA	√
SDMMC0 (1.8V OR 3V AUTO)										
Y27	GPIO4_B0/SDMMC0_D0/UART2DBG_RX	gpio4_b[0]	sdmmc0_data0	uart2dbg_rx		I/O	I	up	6mA	√
Y26	GPIO4_B1/SDMMC0_D1/UART2DBG_TX	gpio4_b[1]	sdmmc0_data1	uart2dbg_tx	hdcpjtag_trstn	I/O	I	up	6mA	√
Y28	GPIO4_B2/SDMMC0_D2/APJTAG_TCK	gpio4_b[2]	sdmmc0_data2	ap_jtag_tck	hdcpjtag_tdi	I/O	I	up	6mA	√
U27	GPIO4_B3/SDMMC0_D3/APJTAG_TMS	gpio4_b[3]	sdmmc0_data3	ap_jtag_tms	hdcpjtag_tdo	I/O	I	up	6mA	√
V29	GPIO4_B4/SDMMC0_CLKOUT/MUCJTAG_TCK	gpio4_b[4]	sdmmc0_clkout	mcujtag_tck	hdcpjtag_tck	I/O	I	down	6mA	√
V25	GPIO4_B5/SDMMC0_CMD/MCUJTAG_TMS	gpio4_b[5]	sdmmc0_cmd	mcujtag_tms	hdcpjtag_tms	I/O	I	up	6mA	√

APIO4 (1.8V OR 3.0V)										
AG6	GPIO4_C0/I2C3_SDA_HDMI/UART2DBG_RX	gpio4_c[0]	i2c3_sda_hdmi	uart2dbg_rx		I/O	I	up	3mA	√
AL2	GPIO4_C1/I2C3_SCL_HDMI/UART2DBG_TX	gpio4_c[1]	i2c3_scl_hdmi	uart2dbg_tx		I/O	I	up	3mA	√
AF5	GPIO4_C2/PWM0/VOP0_PWM/VOP1_PWM	gpio4_c[2]	pwm0	vop0_pwm	vop1_pwm	I/O	I	down	3mA	√
AK2	GPIO4_C3/UART2DBG_RX/UARTHDCP_RX	gpio4_c[3]	uart2dbg_rx	uarthdcp_rx		I/O	I	up	3mA	√
AJ4	GPIO4_C4/UART2DBG_TX/UARTHDCP_TX	gpio4_c[4]	uart2dbg_tx	uarthdcp_tx		I/O	I	up	3mA	√
AK1	GPIO4_C5/SPDIF_TX	gpio4_c[5]	spdif_tx			I/O	I	down	3mA	√
AL3	GPIO4_C6/PWM1	gpio4_c[6]	pwm1			I/O	I	down	3mA	√
AD7	GPIO4_C7/HDMI_CECINOUT/EDP_HOTPLUG	gpio4_c[7]	hdmi_cecinout	edp_hotplug		I/O	I	up	3mA	√
AE6	GPIO4_D0/PCIE_CLKREQN	gpio4_d[0]	pcie_clkreqn			I/O	I	up	3mA	√
AK4	GPIO4_D1/DP_HOTPLUG	gpio4_d[1]	dp_hotplug			I/O	I	down	3mA	√
AH3	GPIO4_D2	gpio4_d[2]				I/O	I	down	3mA	√
AK3	GPIO4_D3	gpio4_d[3]				I/O	I	down	3mA	√
AH5	GPIO4_D4	gpio4_d[4]				I/O	I	down	3mA	√
AJ3	GPIO4_D5	gpio4_d[5]				I/O	I	down	3mA	√
AG4	GPIO4_D6	gpio4_d[6]				I/O	I	down	3mA	√
ADC INTERFACE										
AG26	ADC_IN0									
AH26	ADC_IN1									
AG25	ADC_IN2									
AG28	ADC_IN3									
AH27	ADC_IN4									
EDP INTERFACE										
B29	EDP_TX0P									
A29	EDP_TX0N									
B30	EDP_TX1P									
A30	EDP_TX1N									
C30	EDP_TX2P									

C31	EDP_TX2N									
D30	EDP_TX3P									
D31	EDP_TX3N									
B28	EDP_AUXP									
A28	EDP_AUXN									
G21	EDP_REXT									
G20	EDP_DC_TP									
H21	EDP_CLK24M_IN									
HDMI INTERFACE										
AK17	HDMI_TX0P									
AL17	HDMI_TX0N									
AK18	HDMI_TX1P									
AL18	HDMI_TX1N									
AK19	HDMI_TX2P									
AL19	HDMI_TX2N									
AK16	HDMI_TCP									
AL16	HDMI_TCN									
AF15	HDMI_REXT									
AE15	HDMI_HPD									
PCIe INTERFACE										
AE30	PCIE_TX_0P									
AE31	PCIE_TX_0N									
AF30	PCIE_RX_0P									
AF31	PCIE_RX_0N									
AG30	PCIE_TX_1P									
AG31	PCIE_TX_1N									
AH30	PCIE_RX_1P									
AH31	PCIE_RX_1N									

AA27	PCIE_TX_2P									
AA28	PCIE_TX_2N									
AC27	PCIE_RX_2P									
AC28	PCIE_RX_2N									
AD27	PCIE_TX_3P									
AD28	PCIE_TX_3N									
AF27	PCIE_RX_3P									
AF28	PCIE_RX_3N									
AD31	PCIE_RCLK_100M_P									
AD30	PCIE_RCLK_100M_N									
MIPI TX/RX GROUP INTERFACE										
AK6	MIPI_TX1/RX1_D0P									
AL6	MIPI_TX1/RX1_D0N									
AK7	MIPI_TX1/RX1_D1P									
AL7	MIPI_TX1/RX1_D1N									
AK9	MIPI_TX1/RX1_D2P									
AL9	MIPI_TX1/RX1_D2N									
AK10	MIPI_TX1/RX1_D3P									
AL10	MIPI_TX1/RX1_D3N									
AK8	MIPI_TX1/RX1_CLKP									
AL8	MIPI_TX1/RX1_CLKN									
AF11	MIPI_TX1/RX1_REXT									
MIPI TX GROUP INTERFACE										
AG15	MIPI_TX0_D0P									
AH15	MIPI_TX0_D0N									
AG14	MIPI_TX0_D1P									
AH14	MIPI_TX0_D1N									
AG11	MIPI_TX0_D2P									

AH11	MIPI_TX0_D2N									
AG9	MIPI_TX0_D3P									
AH9	MIPI_TX0_D3N									
AG12	MIPI_TX0_CLKP									
AH12	MIPI_TX0_CLKN									
AF12	MIPI_TX0_REXT									
MIPI RX GROUP INTERFACE										
AK15	MIPI_RX_D0P									
AL15	MIPI_RX_D0N									
AK14	MIPI_RX_D1P									
AL14	MIPI_RX_D1N									
AK12	MIPI_RX_D2P									
AL12	MIPI_RX_D2N									
AK11	MIPI_RX_D3P									
AL11	MIPI_RX_D3N									
AK13	MIPI_RX_CLKP									
AL13	MIPI_RX_CLKN									
AF14	MIPI_RX_REXT									
USIC INTERFACE										
AJ31	USIC_DATA									
AJ30	USIC_STROBE									
USB2.0 INTERFACE										
AB30	USB0_DP	HOST0_DP								
AB31	USB0_DN	HOST0_DN								
AA30	USB1_DP	HOST1_DP								
AA31	USB1_DN	HOST1_DN								
AG23	TYPEC0_DP	OTG0_DP								
AH23	TYPEC0_DN	OTG0_DM								

AG24	TYPEC1_DP	OTG1_DP								
AH24	TYPEC1_DN	OTG1_DM								
AL30	TYPEC0_ID									
AE26	TYPEC1_ID									
AC31	USB0_RBIAS									
AC30	USB1_RBIAS									
AK30	TYPEC0_U2VBUSDET									
AK31	TYPEC1_U2VBUSDET									
TYPE C0 INTERFACE										
AK21	TYPEC0_RX1P									
AL21	TYPEC0_RX1M									
AL22	TYPEC0_TX1P									
AK22	TYPEC0_TX1M									
AK23	TYPEC0_RX2P									
AL23	TYPEC0_RX2M									
AL24	TYPEC0_TX2P									
AK24	TYPEC0_TX2M									
AE18	TYPEC0_RCLKP									
AD18	TYPEC0_RCLKM									
AH18	TYPEC0_CC1									
AH20	TYPEC0_CC2									
AK20	TYPEC0_AUXP									
AL20	TYPEC0_AUXM									
AH17	TYPEC0_AUXP_PD_PU									
AG17	TYPEC0_AUXM_PU_PD									
AG18	TYPEC0_REXT									
AG20	TYPEC0_REXT_CC									
AD19	TYPEC0_U3VBUSDET									

TYPE C1 INTERFACE										
AK25	TYPEC1_RX1P									
AL25	TYPEC1_RX1M									
AL26	TYPEC1_TX1P									
AK26	TYPEC1_TX1M									
AK27	TYPEC1_RX2P									
AL27	TYPEC1_RX2M									
AL28	TYPEC1_TX2P									
AK28	TYPEC1_TX2M									
AE20	TYPEC1_RCLKP									
AD20	TYPEC1_RCLKM									
AH21	TYPEC1_CC1									
AF21	TYPEC1_CC2									
AK29	TYPEC1_AUXP									
AL29	TYPEC1_AUXM									
AE24	TYPEC1_AUXP_PD_PU									
AF25	TYPEC1_AUXM_PU_PD									
AE21	TYPEC1_REXT									
AG21	TYPEC1_REXT_CC									
AC19	TYPEC1_U3VBUSDET									
EMMC INTERFACE										
J28	EMMC_D0									
J29	EMMC_D1									
J30	EMMC_D2									
J25	EMMC_D3									
J26	EMMC_D4									
J27	EMMC_D5									
L31	EMMC_D6									

K30	EMMC_D7									
K31	EMMC_STRB									
L28	EMMC_CLK									
J31	EMMC_CMD									
L29	EMMC_CALIO									
L30	EMMC_TP									
DDR0 GROUP INTERFACE										
AB2	DDR0_DQ0									
AB1	DDR0_DQ1									
AA2	DDR0_DQ2									
AA1	DDR0_DQ3									
Y2	DDR0_DQ4									
Y1	DDR0_DQ5									
W1	DDR0_DQ6									
W2	DDR0_DQ7									
AF2	DDR0_DQ8									
AE2	DDR0_DQ9									
AF1	DDR0_DQ10									
AD2	DDR0_DQ11									
AE1	DDR0_DQ12									
AD1	DDR0_DQ13									
AC1	DDR0_DQ14									
AC2	DDR0_DQ15									
V1	DDR0_DQ16									
V2	DDR0_DQ17									
U1	DDR0_DQ18									
U2	DDR0_DQ19									
T1	DDR0_DQ20									

T2	DDR0_DQ21									
R2	DDR0_DQ22									
R1	DDR0_DQ23									
P1	DDR0_DQ24									
P2	DDR0_DQ25									
N1	DDR0_DQ26									
M1	DDR0_DQ27									
N2	DDR0_DQ28									
L1	DDR0_DQ29									
M2	DDR0_DQ30									
L2	DDR0_DQ31									
Y5	DDR0_DM0									
AC5	DDR0_DM1									
U5	DDR0_DM2									
P5	DDR0_DM3									
Y4	DDR0_DQS0P									
AA4	DDR0_DQS0N									
AC4	DDR0_DQS1P									
AD4	DDR0_DQS1N									
U4	DDR0_DQS2P									
V4	DDR0_DQS2N									
P4	DDR0_DQS3P									
R4	DDR0_DQS3N									
F2	DDR0_A0									
F1	DDR0_A1									
G1	DDR0_A2									
G2	DDR0_A3									
H2	DDR0_A4									

H1	DDR0_A5									
J1	DDR0_A6									
J2	DDR0_A7									
K2	DDR0_A8									
K1	DDR0_A9									
D1	DDR0_A10									
E3	DDR0_A11									
C1	DDR0_A12									
D2	DDR0_A13									
D3	DDR0_A14									
H7	DDR0_A15									
U6	DDR0_ATB0									
U7	DDR0_ATB1									
H4	DDR0_CK0P									
J4	DDR0_CK0N									
H5	DDR0_CK1P									
J5	DDR0_CK1N									
M6	DDR0_CSN0									
B1	DDR0_CSN1									
M5	DDR0_CSN2									
C2	DDR0_CSN3									
E1	DDR0_CKE0									
F5	DDR0_CKE1									
V7	DDR0_PLL_TESTOUT_N									
V6	DDR0_PLL_TESTOUT_P									
C3	DDR0_BA0									
F4	DDR0_BA1									

M4	DDR0_BA2									
U6	DDR0_ATB0									
U7	DDR0_ATB1									
R7	DDR0_PZQ									
L4	DDR0_ODT0									
L5	DDR0_ODT1									
H6	DDR0_CASN									
F3	DDR0_RASN									
G6	DDR0_WEN									
L7	DDR0_RESETN									
DDR1 GROUP INTERFACE										
B15	DDR1_DQ0									
A15	DDR1_DQ1									
B16	DDR1_DQ2									
A16	DDR1_DQ3									
B17	DDR1_DQ4									
A17	DDR1_DQ5									
A18	DDR1_DQ6									
B18	DDR1_DQ7									
B11	DDR1_DQ8									
B12	DDR1_DQ9									
A11	DDR1_DQ10									
B13	DDR1_DQ11									
A12	DDR1_DQ12									
A13	DDR1_DQ13									
A14	DDR1_DQ14									

B14	DDR1_DQ15									
A19	DDR1_DQ16									
B19	DDR1_DQ17									
A20	DDR1_DQ18									
B20	DDR1_DQ19									
A21	DDR1_DQ20									
B21	DDR1_DQ21									
B22	DDR1_DQ22									
A22	DDR1_DQ23									
A23	DDR1_DQ24									
B23	DDR1_DQ25									
A24	DDR1_DQ26									
A25	DDR1_DQ27									
B24	DDR1_DQ28									
A26	DDR1_DQ29									
B25	DDR1_DQ30									
B26	DDR1_DQ31									
E17	DDR1_DM0									
E14	DDR1_DM1									
E20	DDR1_DM2									
E23	DDR1_DM3									
D18	DDR1_DQS0P									
D17	DDR1_DQS0N									
D15	DDR1_DQS1P									
D14	DDR1_DQS1N									
D21	DDR1_DQS2P									
D20	DDR1_DQS2N									
D24	DDR1_DQS3P									

D23	DDR1_DQS3N									
B10	DDR1_A0									
A10	DDR1_A1									
B9	DDR1_A2									
A9	DDR1_A3									
B8	DDR1_A4									
A8	DDR1_A5									
B7	DDR1_A6									
A7	DDR1_A7									
B6	DDR1_A8									
A6	DDR1_A9									
A4	DDR1_A10									
C5	DDR1_A11									
A3	DDR1_A12									
B4	DDR1_A13									
C4	DDR1_A14									
G8	DDR1_A15									
F17	DDR1_ATB0									
G17	DDR1_ATB1									
D9	DDR1_CK0P									
D8	DDR1_CK0N									
E9	DDR1_CK1P									
E8	DDR1_CK1N									
F12	DDR1_CSN0									
A2	DDR1_CSN1									
F11	DDR1_CSN2									
B3	DDR1_CSN3									
A5	DDR1_CKE0									

E6	DDR1_CKE1									
G14	DDR1_PLL_TESTOUT_N									
F14	DDR1_PLL_TESTOUT_P									
B2	DDR1_BA0									
D6	DDR1_BA1									
D12	DDR1_BA2									
F17	DDR1_ATB0									
G17	DDR1_ATB1									
G15	DDR1_PZQ									
D11	DDR1_ODT0									
E11	DDR1_ODT1									
F9	DDR1_CASN									
C6	DDR1_RASN									
F7	DDR1_WEN									
G11	DDR1_RESETN									

Notes:

Pad types: I=input, O=output, I/O=input/output (bidirectional)
Output Drive strength is configurable, it's the suggested value in this table. Unit is mA, only digital IO has drive value
Reset state (def): I = input without any pull resistor O = output
PD/PU: PU=pull up; PD=pull down
INT: "✓" support int function

2.2.2 Power Pin Descriptions

Table 2-3 RK3399 Power Pin Descriptions

Group	Ball Number	Descriptions
VSS	A1,A27,A31,AA10,AA13,AA3,AA5,AA9,AB19,AB9,AC18,AC20,AC21,AC22,AC3,AD10,AD21,AD22,AD3,AD5,AE23,AF18,AF20,AF9,AG2,AJ20,AJ21,AJ23,AJ24,AJ26,AJ27,AJ28,AJ5,AL1,AL31,B5,C11,C12,C14,C15,C17,	Internal Logic Ground and Digital IO Ground
BIGCPU_VDD	K19,K21,L18,L19,L21,L23,M18,M19,M20,M21,M22,N18,N20,N22	Internal BIG CPU A72 Power
LITCPU_VDD	P20,P22,R19,R20,R22,T20,T22	Internal LITTLE CPU A53 Power
GPU_VDD	R11,R12,R13,T11,T12,T13,T14,T15,U13,V11,V12,V13,V14,V15,V16,W10,W11,W12,W14,W15,W16	Internal GPU power
LOGIC_VDD	L17,M17,T17,U17,U18,U20,V18,V19,V20,V21,V22,W20	Internal Logic Power
CENTERLOGIC_VDD	M11,M12,M13,M14,M15,N11,N12,P13,P14,P15	Internal Center Logic Power
DDR0_VDD	L9,L10,M9,N9,N10,P9,R9,R10,T9,U9,U10,V9	DDR0 Digital IO Power
DDR0_CLK_VDD	M7	DDR0Clock IO Power
DDR0PLL_AVDD_0V9	R8	DDR0 PHY PLL power
DDR1_VDD	J11,J12,J13,J14,J15,J16,J17,J18,K11,K13,K15,K17	DDR0 Digital IO Power
DDR1_CLK_VDD	G12	DDR0Clock IO Power
DDR1PLL_AVDD_0V9	H14	DDR0 PHY PLL power
PMU_VDD_0V9	T24	Internal PMU Domain Power
PMU_VDD_1V8	U25	
PMUIO1_VDD_1V8	R24	PMUIO1 Domain IO Power
PMUIO2_VDDPST	N23	PMUIO2 Domain IO Power
PMUIO2_VDD	P23	PMUIO2 Domain IO Power
APIO1_VDD	J23	GPIO group 1 Digital Power
APIO1_VDDPST	J22	GPIO group1 Bias
APIO2_VDD	K23	GPIO group 2 Digital Power
APIO2_VDDPST	J24	GPIO group 2 Bias
APIO3_VDD_1V8	AB8	GPIO group 3 Digital Power
APIO4_VDD	AC9	GPIO group 4 Digital Power
APIO4_VDDPST	AC8	GPIO group4 Bias
APIO5_VDD	Y8	GPIO group 5 Digital Power
APIO5_VDDPST	AA8	GPIO group5 Bias
SDMMC0_VDD	T23	SDMMC Digital IO Power
SDMMC0_VDDPST	,U26	SDMMC Digital IO Power
AVSS	AA11,AA12,AA14,AA15,AA23,AA26,AA29,AB10,AB11,AB13,AB15,AB16,AB17,AB23,AC11,AC13,AC15,AC16,AC17,AC23,AC25,AC26,AC29,AD13,AD17,AD26,AD29,AE11,AE12,AE14,AE17,AE27,AF17,AF23,AF24,AF29,AG29,AH29,AJ6,AJ8,AJ9,AJ11,AJ12,AJ14	Analog Ground

Group	Ball Number	Descriptions
PLL_AVDD_0V9	R17	PLL 0.9V Analog Power
PLL_AVDD_1V8	P18	PLL 1.8V Analog Power
PLL_AVSS	P17	PLL Analog Ground
ADC_AVDD	AC24	SAR-ADC/TSADC Power
EMMC_COREDLL_0V9	L24	EMMC Core Power
EMMC_VDD_1V8	K24	EMMC Digital Power
USB_AVDD_0V9	V24	USB 2.0 Digital Power
USB_AVDD_1V8	U24	USB 2.0 Analog Power
USB_AVDD_3V3	Y25	USB 2.0 Analog Power
TYPEC0_AVDD_0V9	Y18,Y19	Type-C Digital Power
TYPEC0_AVDD_1V8	AA18	Type-C Analog Power
TYPEC0_AVDD_3V3	AB18	Type-C Analog Power
TYPEC1_AVDD_0V9	Y21,Y22	Type-C Digital Power
TYPEC1_AVDD_1V8	AA21	Type-C Analog Power
TYPEC1_AVDD_3V3	AB21	Type-C Analog Power
EFUSE	AD23	eFuse IO Digital Power
USIC_VDD_1V2	AD24	USIC 1.2V Power Supply
USIC_VDD_0V9	AD25	USIC 0.9V Power Supply
EDP_AVDD_0V9	H20	eDP0.9V Power Supply
EDP_AVDD_1V8	J19,J20	eDP 1.8V Power Supply
EDP_AVSS	B31,C28,C29,D29,H19,J21	eDP Analog Ground
HDMI_AVDD_0V9	AA16,AA17	HDMI 0.9V Power Supply
HDMI_AVDD_1V8	AD16	HDMI 1.8V Power Supply
MIPI_RX0_AVDD_1V8	AB14	MIPI RX 1.8V Power Supply
MIPI_TX0_AVDD_1V8	AB12	MIPI TX 1.8V Power Supply
MIPI_TX1/RX1_AVDD_1V8	AC10	MIPI TX/RX 1.8V Power Supply
PCIE_AVDD_0V9	W24	PCIE 0.9V Analog Power
PCIE_AVDD_1V8	Y24	PCIE 1.8V Analog Power

2.3 GPIO Type

2.3.1 GPIO Type

RK3399 has four GPIO types:

- 1.8V only,Fixed 1.8V
- 3.3V only,Fixed 3.3V
- 1.8V/3.0V,configurable 1.8V or 3.0V
- 1.8V/3.0V auto,configurable 1.8V or 3.0V

2.3.2 GPIO`s Drive Capability

RK3399 GPIO`s drive capability shown as Table 2-4.

Table 2-4 RK3399 GPIO`s Drive Capability

Power Domain	GPIO Type	I/O Frequency @1.8V	I/O Frequency @3.xV	Drive Strength
PMUIO1	1.8V only	150MHz	N/A	5mA,10mA,15mA,20mA
APIO3	1.8V only	150MHz	N/A	5mA,10mA,15mA,20mA
APIO1	3.3V only	N/A	125MHz	4mA,7mA,10mA,13mA,16mA,19mA,22mA,26mA
PMUIO2	1.8V/3.0V	150MHz	50MHz	3mA,6mA,9mA,12mA
APIO2	1.8V/3.0V	150MHz	50MHz	3mA,6mA,9mA,12mA
APIO4	1.8V/3.0V	150MHz	50MHz	3mA,6mA,9mA,12mA
APIO5	1.8V/3.0V	150MHz	50MHz	3mA,6mA,9mA,12mA
SDMMC0	1.8V/3.0V auto	150MHz	50MHz	4mA,6mA,8mA,10mA,12mA,14mA,16mA,18mA

The following two types GPIO in Table 2-4 default drive strength is the second gear, and other type GPIO default drive strength is the first gear. Please adjust the software according to the actual requirements.

- Boot IO,such as SPI1,SDMMC0
  Pin P27:GPIO1_A7/SPI1_RXD/UART4_RX
  Pin R31:GPIO1_B0/SPI1_TXD/UART4_TX
  Pin P28:GPIO1_B1/SPI1_CLK/PMCU_JTAG_TCK
  Pin P29:GPIO1_B2/SPI1_CSn0/PMCU_JTAG_TMS
  Pin Y27:GPIO4_B0/SDMMC0_D0/UART2A_RX
  Pin Y26: GPIO4_B1/SDMMC0_D1/UART2A_TX
  Pin Y28: GPIO4_B2/SDMMC0_D2/APJTAG_TCK
  Pin U27: GPIO4_B3/SDMMC0_D3/APJTAG_TMS
  Pin V29: GPIO4_B4/SDMMC0_CLKOUT/MUCJTAG_TCK
  Pin V25: GPIO4_B5/SDMMC0_CMD/MCUJTAG_TMS
- Debug IO,such as JTAG：
  Pin L25:GPIO1_C6/TESTJTAG_TDI/TCPD_VBUS_SOURCE0
  Pin M31:GPIO1_C7/TESTJTAG_TDO/TCPD_VBUS_SOURCE1
  Pin L26:GPIO1_D0/TESTJTAG_CLK/TCPD_VBUS_SOURCE2

2.3.3 GPIO Power Pin Descriptions

Table 2-5 RK3399 GPIO Power Pin Descriptions

Power domain	GPIO Type	Pin name	Pin descriptions
PMUIO1	1.8V only	PMUIO1_VDD_1V8	1.8V power for this domain (group of) GPIO.
APIO3	1.8V only	APIO3_VDD_1V8	1.8V power for this domain (group of) GPIO.
APIO1	3.3V only	APIO1_VDD	3.3V power for this domain (group of) GPIO.
		APIO1_VDDPST	1.8V Post drive.
PMUIO2	1.8V/3.0V	PMUIO2_VDD	1.8V or 3.0V power for this domain (group of) GPIO.
		PMUIO2_VDDPST	1.8V or 1.5V post drive for this domain (group of) GPIO.
APIO2	1.8V/3.0V	APIO2_VDD	1.8V or 3.0V power for this domain (group of) GPIO.
		APIO2_VDDPST	1.8V or 1.5V post drive for this domain (group of) GPIO.
APIO4	1.8V/3.0V	APIO4_VDD	1.8V or 3.0V power for this domain (group of) GPIO.
		APIO4_VDDPST	1.8V or 1.5V post drive for this domain (group of) GPIO.
APIO5	1.8V/3.0V	APIO5_VDD	1.8V or 3.0V power for this domain (group of) GPIO.
		APIO5_VDDPST	1.8V or 1.5V post drive for this domain (group of) GPIO.

SDMMC0	1.8V/3.0V auto	SDMMC0_VDD	1.8V or 3.0V power for this domain (group of) GPIO.
		SDMMC0_VDDPST	Internal post drive for this domain (group of) GPIO.

For different applications, please follow the next power rules:

- 1.8V Only (PMUIO1 and APIO3 Power Domain)

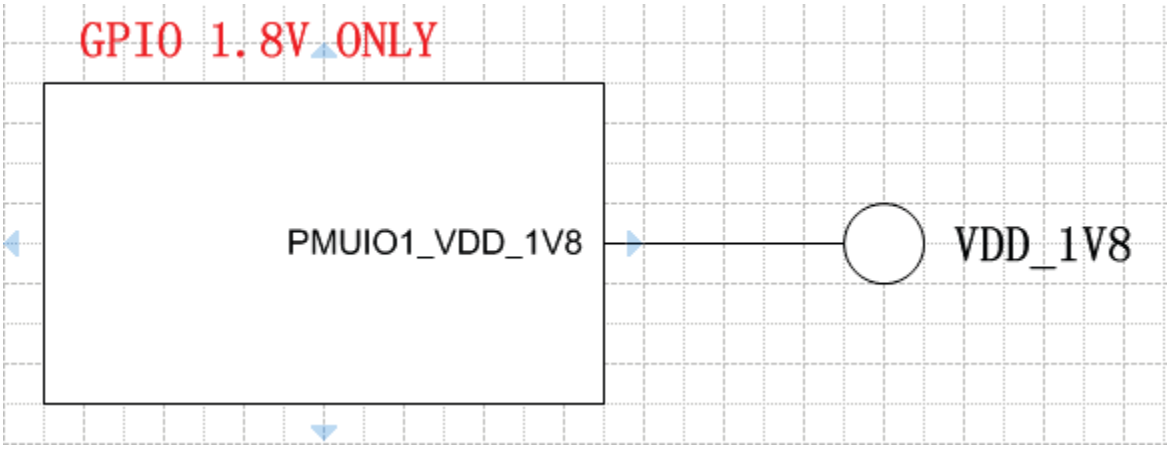


Figure 2-6 RK3399 GPIO 1.8V Only

- 3.3V Only (APIO1 Power Domain)

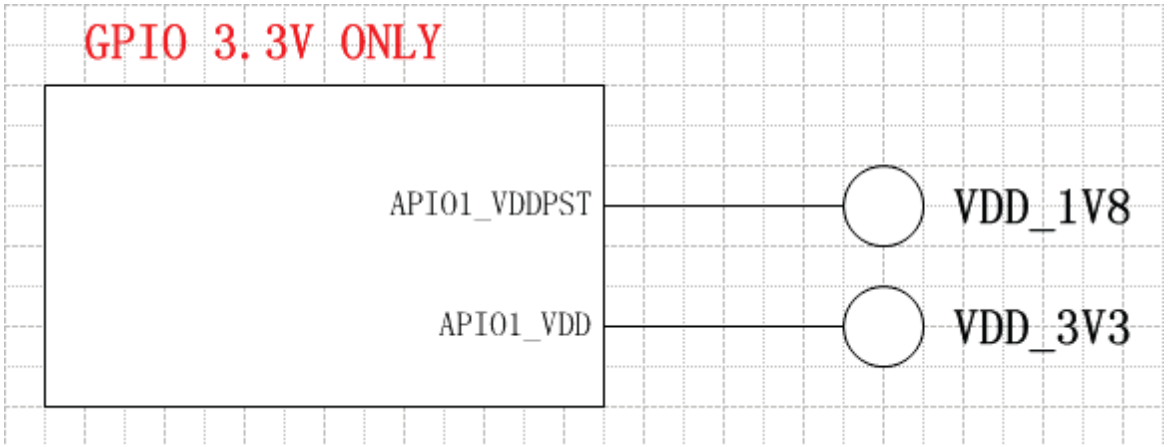


Figure 2-7 RK3399 GPIO 3.3V Only

- 1.8V/3.0V at 1.8V mode(PMUIO2、APIO2、APIO4 and APIO5 Power Domain)

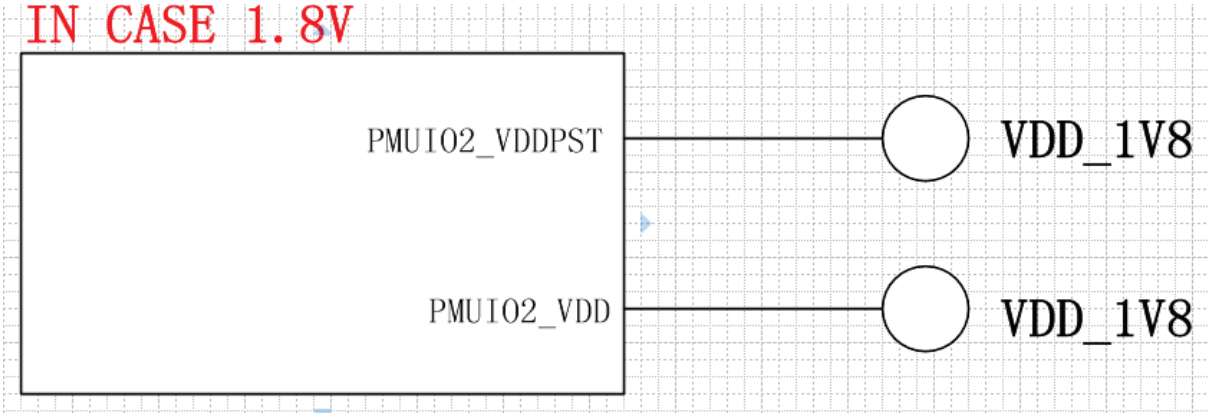


Figure 2-8 RK3399 GPIO 1.8V/3.0V -1.8V Mode

- 1.8V/3.0V at 3.0V mode(PMUIO2、APIO2、APIO4 and APIO5 Power Domain)

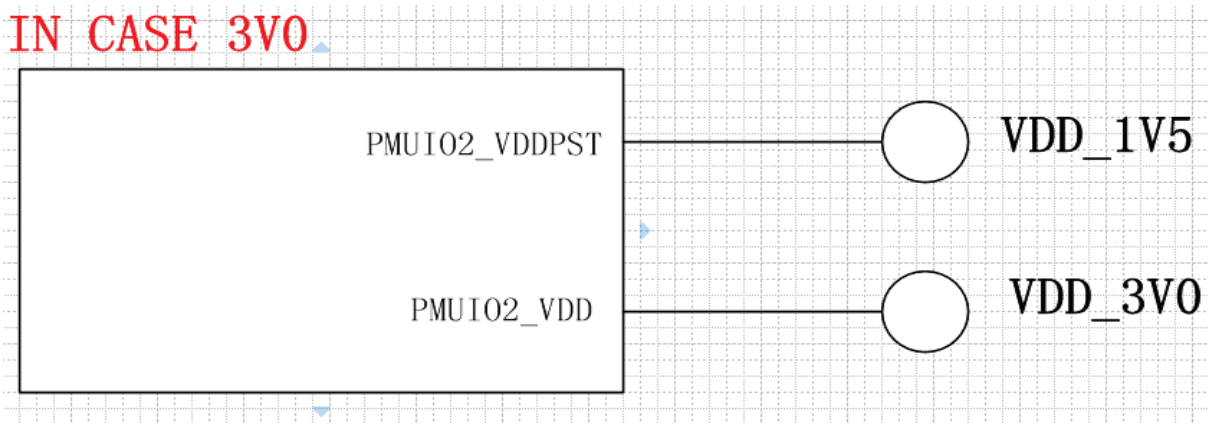


Figure 2-9 RK3399 GPIO 1.8V/3.0V -3.0V Mode

- 1.8V/3.0V Auto (SDMMC0 Power Domain)

SD/MMC card should always be supplied 3.0V, and RK3399 SD/MMC interface default level is 3.0V. When the SD/MMC card is inserted, the signal communication level of the SDMMC0 is based on 3.0V. After communicate negotiation, if the SD/MMC card is a SD3.0, which can support USH-I high speed protocol, RK3399 will adjust the SD/MMC card interface level value to 1.8V through adjusting the PMIC output.

RK3399 built-in VDDPST circuit, shows as Figure 2-10. There are a LDO and a power switch embedded in the SDMMC. When the SDMMC works in 3.0 mode, LDO works and generates a 1.5V voltage for VDDPST. When the SDMMC works in the 1.8 mode, power switch works, VDDPST power is provided by SDMMC0_VDD.

The LDO and power switch are controlled automatically by RK3399. Only a 1uF decoupling capacitor is required on the SDMMC0_VDDPST power pin.

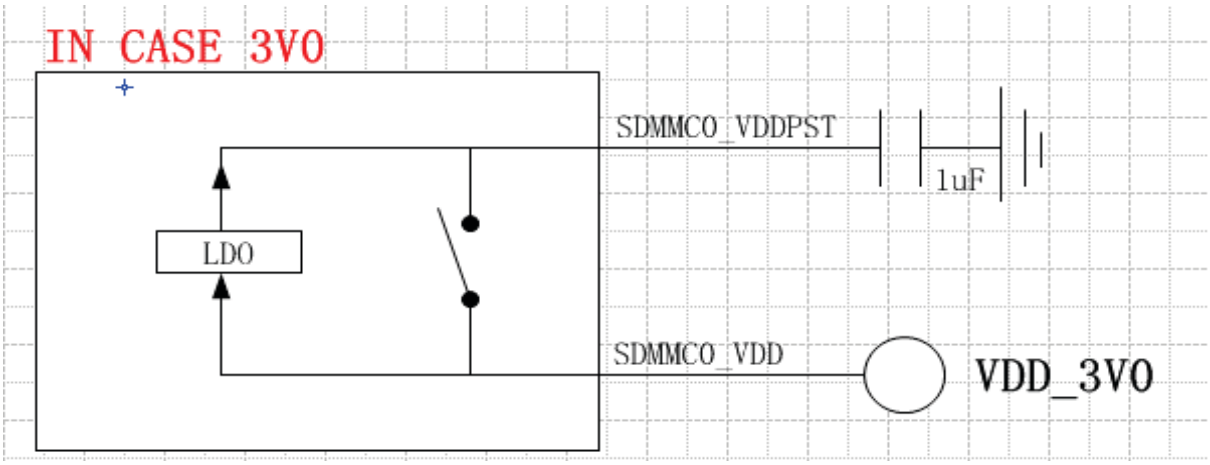


Figure 2-10 RK3399 GPIO 1.8V/3.0V Auto -3.0V Mode

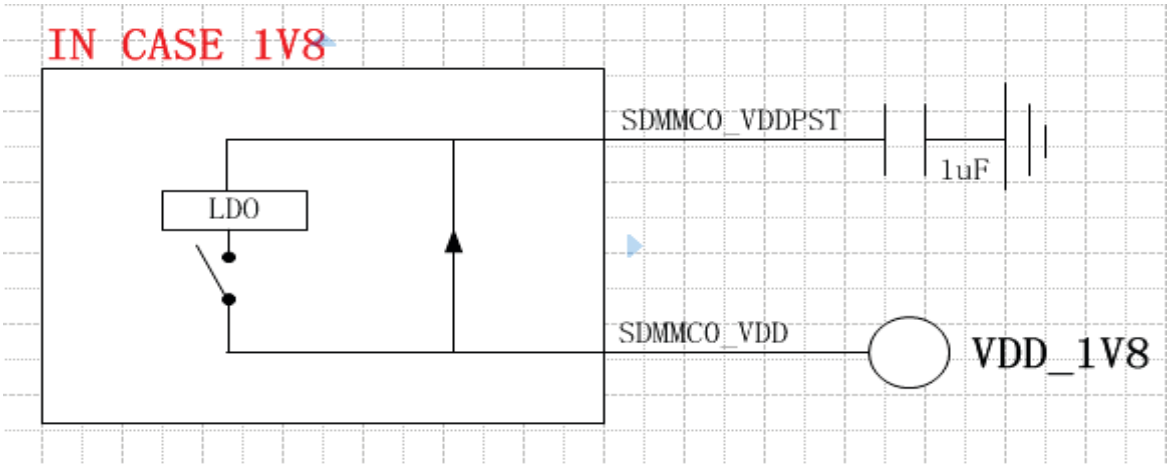


Figure 2-11 RK3399 GPIO 1.8V/3.0V Auto -1.8V Mode

Chapter3 Schematic Design

3.1 Minimum System Design

3.1.1 Clock Circuit

RK3399 needs an external 24 MHz crystal to provide the system clock, shown as Figure 3-1.

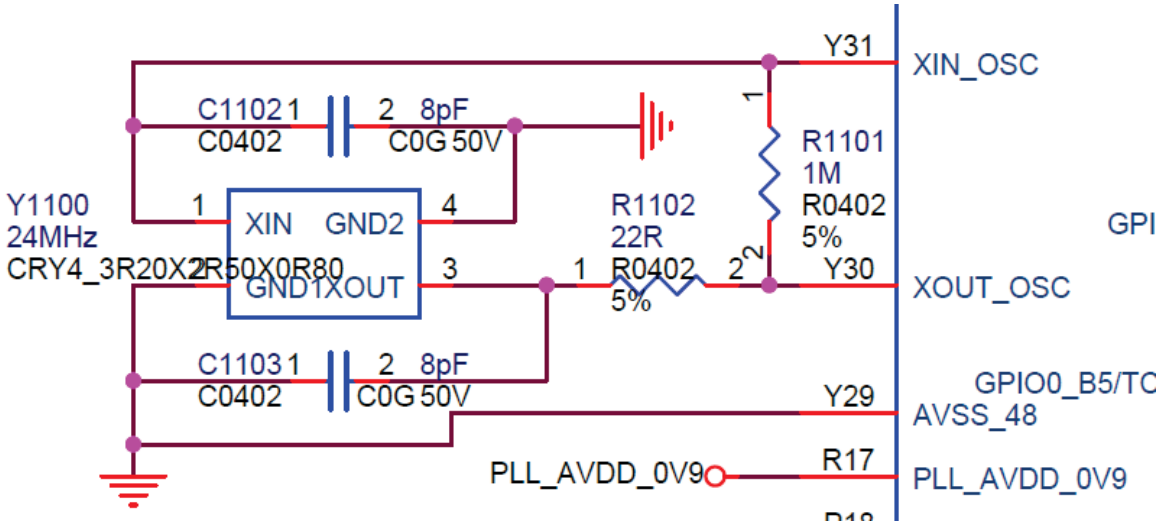


Figure 3-1 RK3399 Clock Circuit

Notes:

The value of capacitor C1102 and C1103 need to be selected according to the actual nominal load capacity of crystal.

In addition, the system clock can also be directly generated by the external crystal clock circuit, input to the Xin_OSC pin. The clock requirement is shown as Table 3-1.

Table 3-1 RK3399 24MHz Clock Requirement

Items	Parameters			Description
	Min.	Max.	Units	
Frequency	24.000000		MHz	
Freq. Offset	+/-20		ppm	Frequency tolerance
Work Temp.	-20	70	℃	
ESR	/	40	Ohm	

When RK3399 is in sleep mode, the internal clock will switch to the external 32.768 KHz coming from PMIC or RTC, to reduce the system power consumption.Show as Figure 3-2.

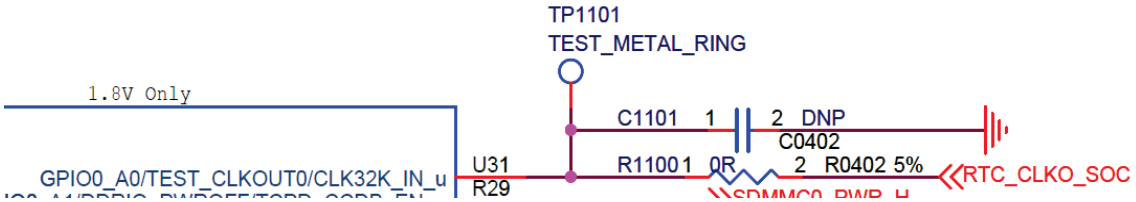


Figure 3-2 RK3399 Sleep Mode Clock Input

External 32.768 KHz RTC Clock requirement is shown as Table 3-2.

Table 3-2 RK3399 32.768KHz Clock Requirement

Items	Parameters			Description
	Min.	Max	Units	
Frequency	32.768000		kHz	
Freq. Offset	±30		ppm	Frequency tolerance
Work Temp.	-20	70	℃	
Clock Duty	50		%	

3.1.2 Reset Circuit

RK3399 embedded POR (Power on Reset) circuit, active on low level. C1100 is used to eliminate jitter.Show as Figure 3-3.In order to ensure OSC work stably, the minimum reset time required is 100 clock cycles of 24MHz, that means 4 us at least.

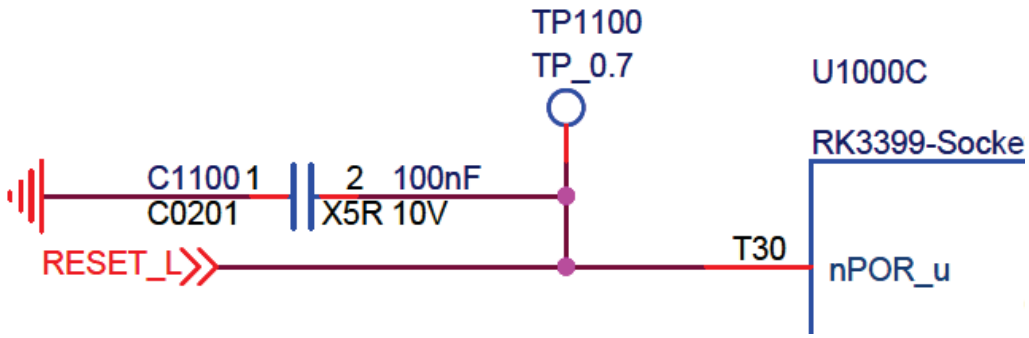


Figure 3-3 RK3399 Reset Input

3.1.3 System Boot Sequence

System boot sequency, priority from high to low.

- SPI FALSH
- eMMC FLASH
- SDMMC CARD

3.1.4 System Initialization Configuration

RK3399 PMUIO2 is PMU domain and IO voltage could be configured.So when system starts, the default drive strength can not be adjusted by reading the register status, and needs to be configured through the set pin.

RK3399 JTAG and SDMMC function is reused together, need the set pin to select output function, default is SD insertion detect pin.

Configuration description is shown as Table 3-3.

Table 3-3 RK3399 Initialization Configuration Description

Signals	Pull Up/Down	Description
PMUIO2_VOLSEL	Pull Down	PMUIO2 power supply configuration,valid only at power-up 0: IO level configuration 1.8V（default） 1: IO level configuration 3.0V
SDMMC0_DET	Pull Up	JTAG or SDMMC select pin 0: Detected low level,set SDMMC/JATG/UAR as SDMMC function 1: Detected high level,set SDMMC/JATG/UAR as JTAG/UART function（default）

3.1.5 JTAG Debug Interface

RK3399 JTAG interface compliant with IEEE1149.1 protocol. PC can be connected with DSTREAM emulator by SWD (Two-line mode) mode to debug A53/A72 core. Or connect with J-link/U-link/Realview-ICE/DSTREAM emulator to debug M0 core.

Before the emulator is connected, make ensure that the SDMMC0_DET pin is at a high level; otherwise it could not enter into JTAG debug mode.The interface is shown as Table 3-4.

Table 3-4 RK3399 JTAG Debug Interface

Signals	Description
APJTAG_TCK	AP JTAG clock inout,recommend pull down
APJTAG_TMS	AP JTAG mode select input, recommend pull up
MUCJTAG_TCK	MCU JTAG clock inout,recommend pull down
MUCJTAG_TMS	MCU JTAG mode select input, recommend pull up
PMCUJTAG_TCK	PMCU JTAG clock inout,recommend pull down
PMCUJTAG_TMS	PMCU JTAG mode select input, recommend pull up

3.1.6 DDR Controller

- 3.1.6.1 DDR Controller Introduction

RK3399 DDR controller supports DDR3/DDR3L/LPDDR3/LPDDR4 SDRAM; the controller has the following characteristics:

- Support 2 channels, each channel is 16 or 32bits data width
- Support up to 2 ranks (chip select) for each channel; totally 4GB (max) address space. Maximum address space of one rank in a channel is also 4GB, which is configurable in software.
- 32bits/64bits data width is software programmable
- Support power-sleep, self-refresh low power consumption mode

- 3.1.6.2 DDR Topological Structure And Connection Mode

RK3399 SDRAM topological structure is shown as Figure 3-4, Taking LPDDR3 as an example.

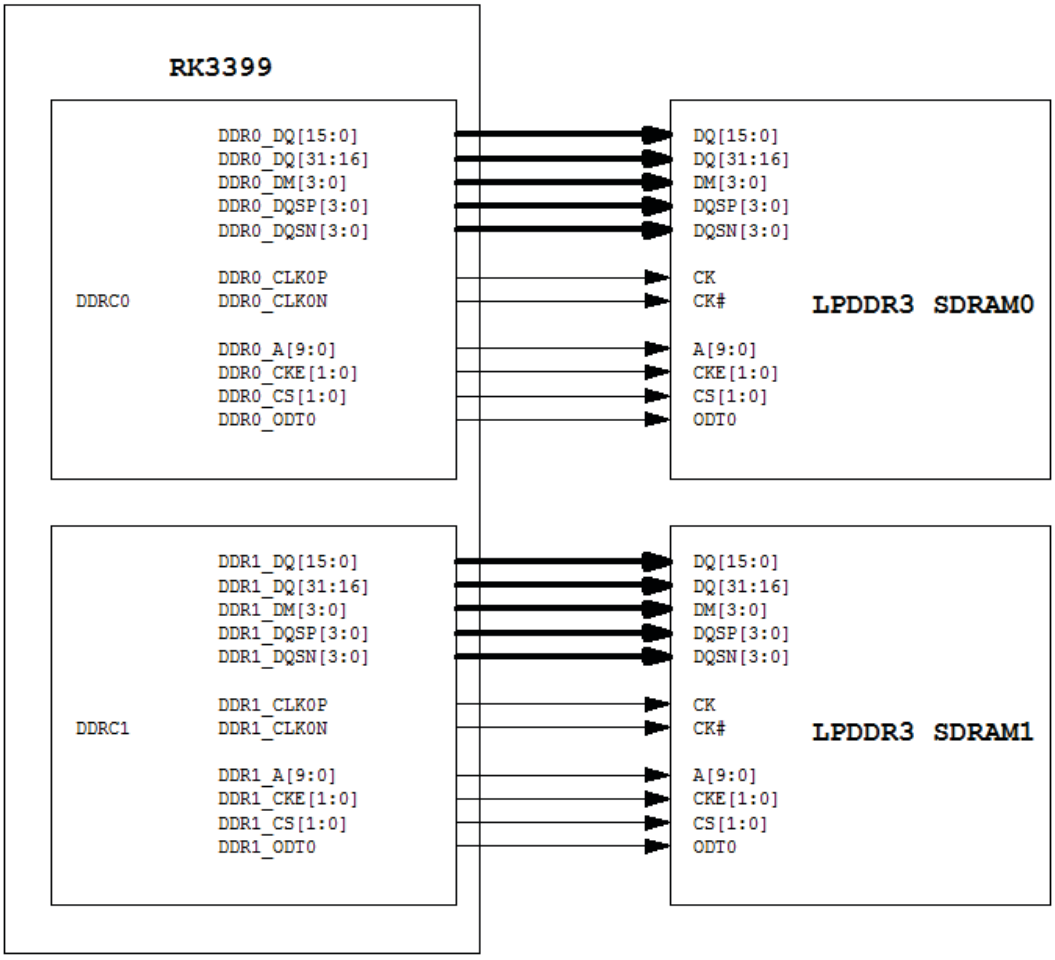


Figure 3-4 RK3399 SDRAM Topological Structure

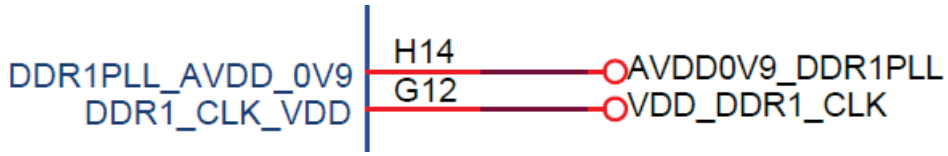


Figure 3-5 RK3399 DDR Controller Power Supply

- 3.1.6.3 DDR Power-up Sequencing

RK3399 DDR controller has three groups power supply:

- DDR_VDD：Power for DDR controller Core, IO, Buffer
- DDRx_CLK_VDD：Power for DDR controller clock, it is necessary consistented with VCC_DDR, it is recommended be powered from VCC_DDR and be routed separately.
- DDRxPLL_AVDD_0V9：Power for DDR controller PLL, recommended supply from LDO to ensure a clean power.

RK3399 DDR power-up sequencing should follow below steps:

- DDRx_CLK_VDD and DDR_VDD power supply from the same power
- DDR_VDD and DDRxPLL_AVDD_0V9 could power-up at the same time.However, for better ESD, it is recommended that low voltage DDRxPLL_AVDD_0V9 shall be powered on first.

The SDRAM power supply power-up sequencing please refer to the JEDEC protocol, LPDDR3 power supply power-up sequencing is shown as Figure 3-6.

After...	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2}—200mV
	V_{DD1} and V_{DD2} must be greater than V_{DDCA}—200mV
	V_{DD1} and V_{DD2} must be greater than V_{DDQ}—200mV
	V_{Ref} must always be less than all other supply voltages

Figure 3-6 LPDDR3 DRAM Power-up Sequencing

- 3.1.6.4 DDR Support List

RK3399 DDR compatible with DDR3/LPDDR3 up to 800MHz,DDR support list please refer to"RK DDR Support List" released by ROCK-CHIP.

3.1.7 eMMC Controller

- 3.1.7.1 eMMC Controller Introduction

RK3399 eMMC controller compatible with eMMC 5.1 protocol has the following characteristics:

- Support one channel eMMC,8 bits mode
- Compatible with eMMC 5.1 protocol,support HS400 mode

- 3.1.7.2 eMMC Interface

Please follow Table 3-5 to design.

Table 3-5 RK3399 eMMC Interface

Signals	Internal Pull-up/down	Series Resistance	Description（For SOC）
eMMC_DQ[7:0]	Pull-up	NO	eMMC data
eMMC_CLK	NA	22ohm (recommended)	eMMC clock
eMMC_CMD	Pull-up	NO	eMMC command
eMMC_STRB	Pull-down	NO	In HS400 mode,Byte data store instruction

- 3.1.7.3 eMMC Power-up Sequencing

RK3399 eMMC control has two groups power supply:

- VCC0V9_EMMC：Power for eMMC control core
- VCC1V8_EMMC：Power for eMMC control I/O

RK3399 eMMC power-up sequencing refer to Figure 3-7.

- VCC0V9_EMMC and VCC1V8_EMMC can be powered on at the same time, however, for better ESD protection, it is recommended that low voltage VCC0V9_EMMC shall be powered on first.

Figure 3-7 RK3399 eMMC Power-up Sequencing

The eMMC part power-up sequencing refer to the JEDEC protocol.

- VCC and VCCQ can be powered on at the same time
- VCC and VCCQ must be powered-up before CMD sent out,and the power supply must work stably
- After eMMC part is in sleep,the power supply could be powered off to reduce the power consumption
- VCC must be powered on and work stably before eMMC part be resumed

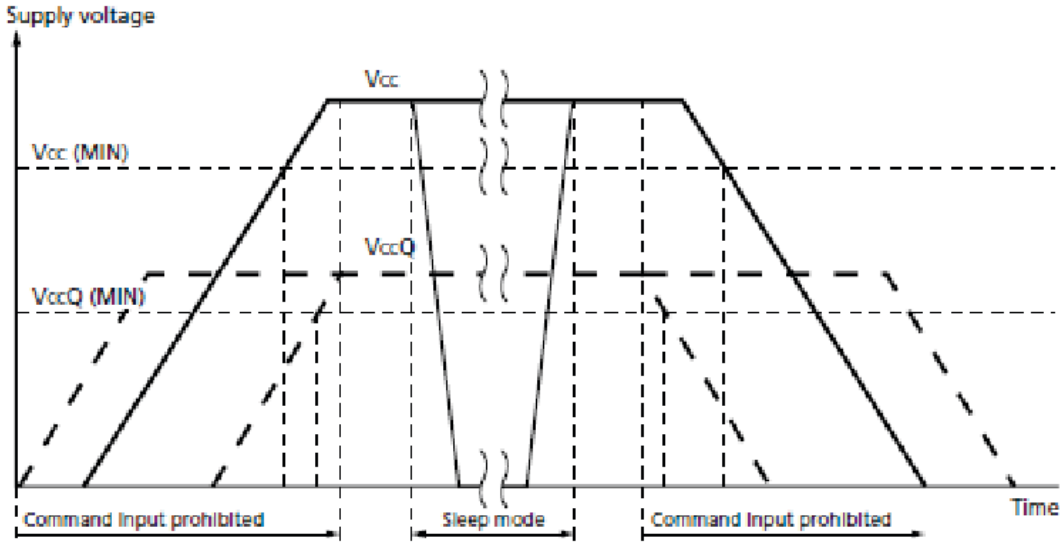


Figure 3-8 eMMC Device Power-up Sequencing

- 3.1.7.4 eMMC Support List

RK3399 eMMC support HS400 mode, support list please refer to"RK eMMCSupportList" released by ROCK-CHIP.

3.1.8 SPI Interface

- 3.1.8.1 SPI Controller Introduction

RK3399 has 6 SPI controllers. Be care for SPI1 is only used for SPI Flash boot, could not be connected to any other SPI devices.

- 3.1.8.2 SPI Interface

SPI interface design follow Table 3-6 for reference.

Table 3-6 RK3399 SPI Interface

Pin Name	Internal Pull-up/down	Series Resistance	Description（For SOC）
SPI1_TXD（MOSI）	Pull-up	NO	SPI data transmission
SPI1_RXD（MISO）	Pull-up	NO	SPI data receive
SPI1_CLK	Pull-up	22ohm (recommended)	SPI clock output
SPI1_CSn0	Pull-up	NO	SPI chip select

- 3.1.8.3 SPI Power-up Sequencing

  These are no requirements for power-up sequencing.

3.2 System Power

3.2.1 Minimum System Description

- 3.2.1.1 Power supply Demand
  - PLL：PLL_AVDD_0V9、PLL_AVDD_1V8、PMU_VDD_0V9、PMU_VDD_1V8、DDRPLL_AVDD_0V9
  - CPU：VDD_CPU_L、VDD_CPU_B
  - GPU：VDD_GPU
  - LOGIC：VDD_LOG、VDD_CENTER
  - DDR: VCC_DDR、VCC_DDRC
  - GPIO：PMUIO1_VDD_1V8

- 3.2.1.2 Power-up Sequencing

The low voltage is powered on at first in the same IP, The same voltage in one IP could be powered on at the same time, and there are no requirements between different IP.

Recommended power-up sequencing:

PLL_AVDD_0V9&PMU_VDD_0V9--->VDD_LOG--->PLL_AVDD_1V8&PMU_VDD_1V8&PMUIO1_VDD_1V8--->VDD_GPU&VCC_CPU_B---> VCC_DDR&VCC_DDRC---> VCC_CPU_L--->VDD_CENTER

3.2.2 System Power Design

- 3.2.2.1 System Power Supply in Standby

RK3399 system power supply is divided into two parts, constant power supply and power-off in standby. Show as Figure 3-9.

In standby mode, power-off is controlled by SOC via I2C and GPIO.The following power supply must be always on in standby:

- DDR：VCC_DDR、DDRx_CLK_VDD,power for DDR self-refresh
- GPIO：PMUIO1_VDD_1V8,power for PMUIO1 IO
- CORE：PMU_VDD_0V9,power for PMUIO1 PLL
- PLL：PMU_VDD_1V8,power for PMUIO1 PLL and OSC

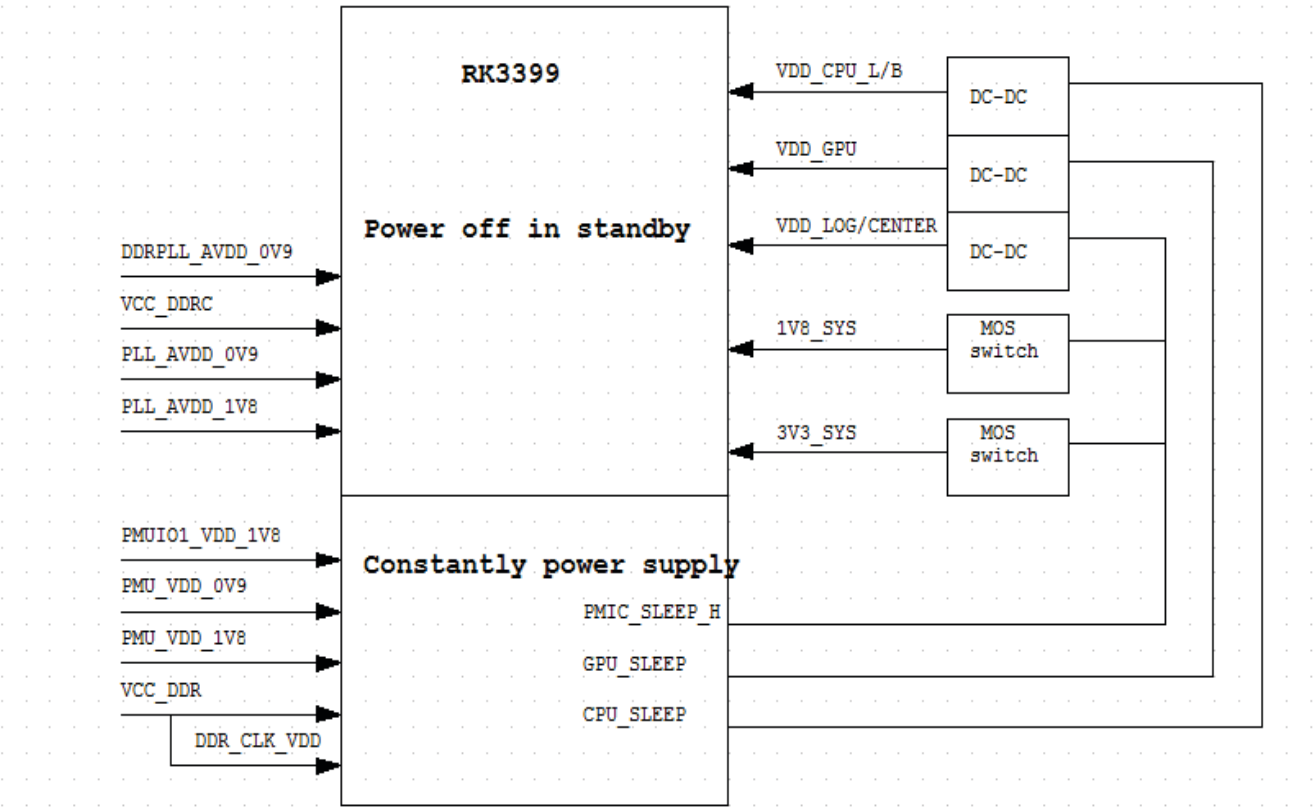


Figure 3-9 RK3399 System Power Supply in Standby

- 3.2.2.2 PLL Power Supply

RK3399 is integrated 10 PLL, show as Table 3-7.

Table 3-7 RK3399 PLL Introduction

Items	Number	Power Pin	In Standby
PMU/OSC	1	PMU_VDD_0V9、PMU_VDD_1V8	Always power-on
DDR Controller	2	DDR0PLL_AVDD_0V9、DDR1PLL_AVDD_0V9	Can power-off
PLL	7	PLL_AVDD_0V9，PLL_AVDD_1V8	Can power-off

It is recommended to use a LDO as a separate power supply for PLL, it can work more stable at high frequency.The decoupling capacitor should be placed close to power supply pin.

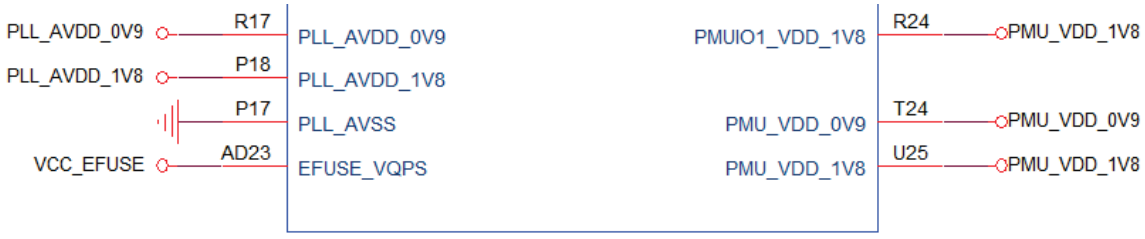


Figure 3-10 RK3399 PLL Power 1

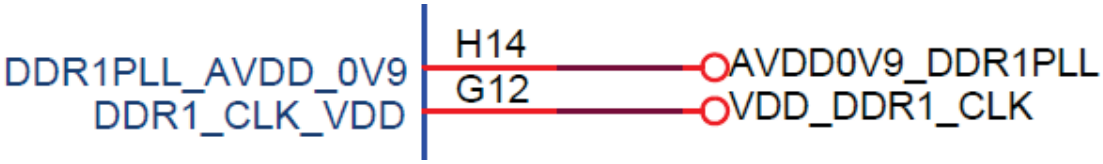


Figure 3-11 RK3399 PLL Power 2

- 3.2.2.3 CPU Power Supply

RK3399 has Big CPU and Little CPU, there are different power domain, VDD_CPU_B for Big core A72, VDD_CPU_L for Little core A53.Both of them support DVFS (Dynamic Volt Frequency Scaling) function.Use two separate BUCK IC to supply to each other.The Big CPU peak current could be up to 4.3A, so please do not reduce the capacitors number as require in the reference design. For layout, the high-capacity capacitors should be placed close to CPU power pins, which recommended to place on the RK3399 opposite, to ensure the power ripple is controlled within 100mV.Shown as Figure 3-12&3-13.

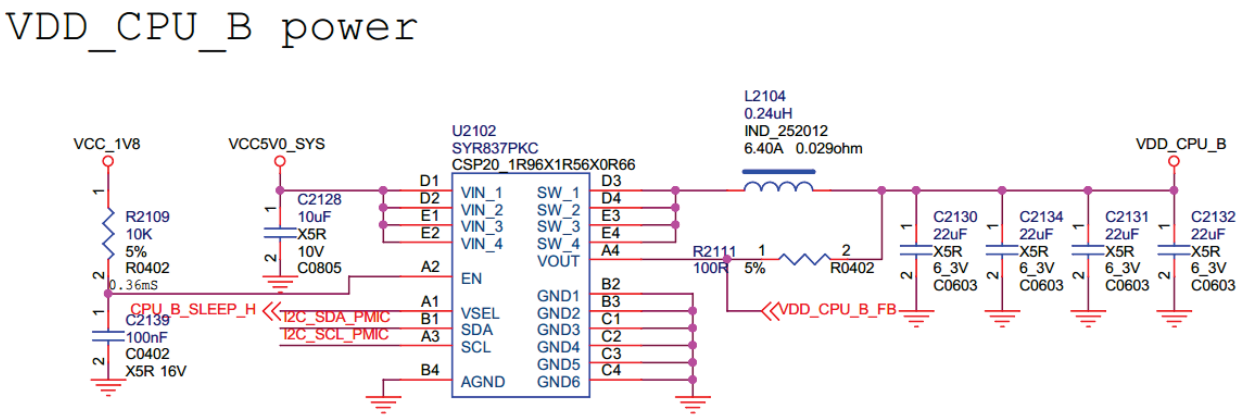


Figure 3-12 RK3399 VDD_CPU Power Supply

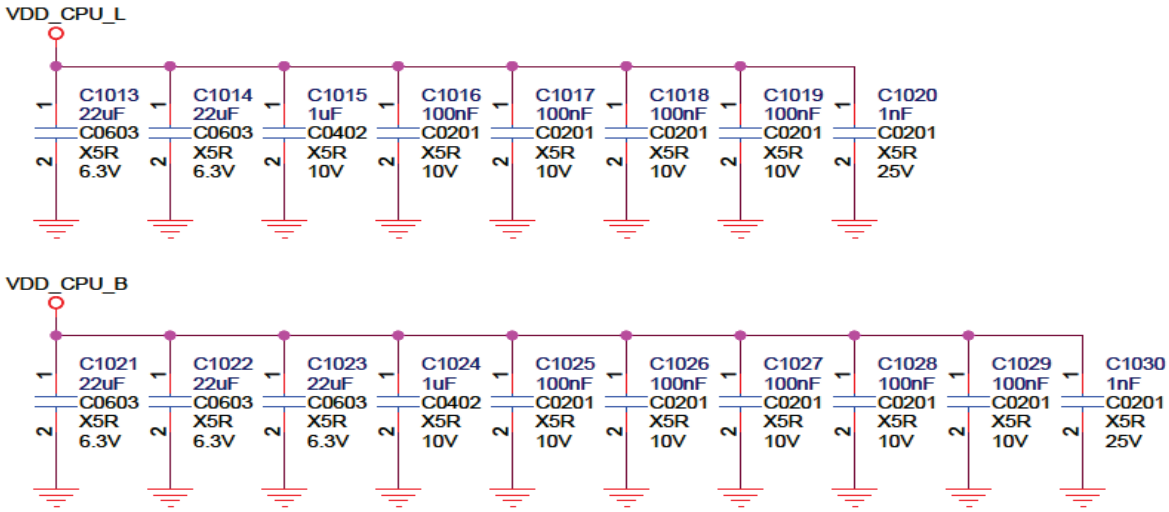


Figure 3-13 RK3399 VDD_CPU Power Filter Capacitances

BIGCPU_VDD_COM is VDD_CPU_B power feedback pin, it should be connected to FB of BUCK IC, which can compensate the loss of PCB power traces impedance, and improve the real-time of dynamic adjustment power supply.

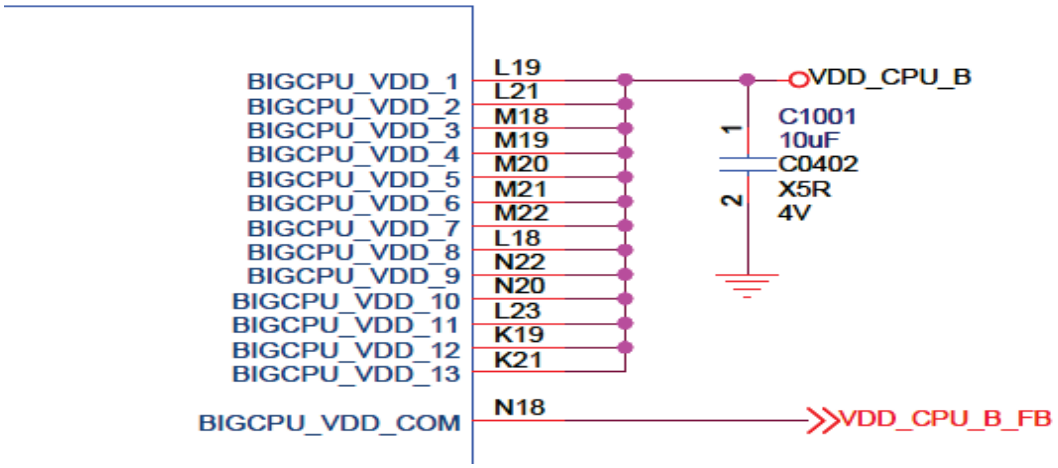


Figure 3-14 RK3399 VDD_CPU_COM Power Feedback

- 3.2.2.4 GPU Power Supply

Use a separate BUCK power supply for RK3399 GPU, support DVFS(Dynamic Volt Frequency Scalling).The GPU peak current would be up to 4.0A,so please do not reduce the capacitors number in the required in reference design. For layout, the high-capacity capacitors should be placed close to CPU power pin, which is recommended to place on the RK3399 opposite, to ensure the power ripple is controlled within 100mV.Shown as Figure 3-15&3-16.

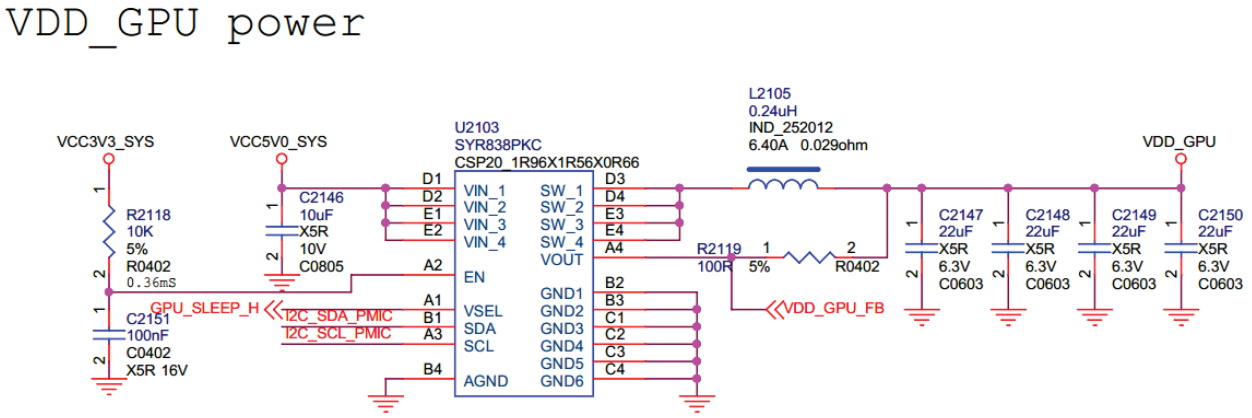


Figure 3-15 RK3399 VDD_GPU Power Supply

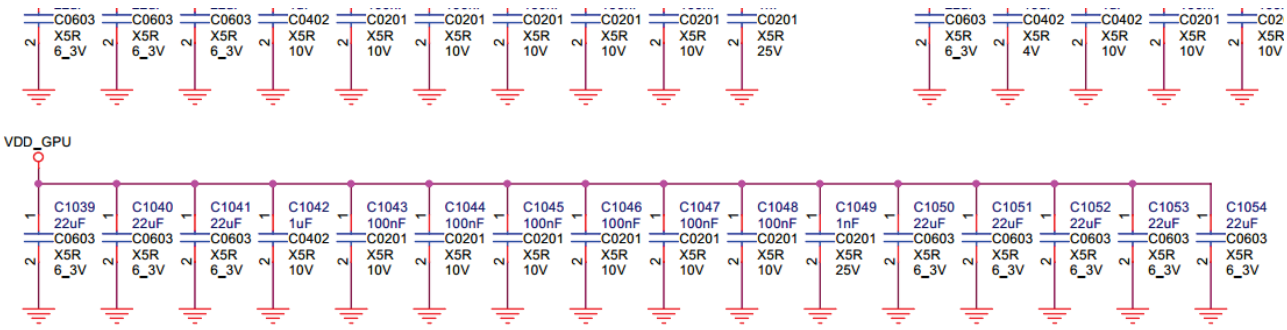


Figure 3-16 RK3399 VDD_GPU Power Filter Capacitors

GPU_VDD_COM is GPU_VDD power feedback pin, it should be connected to FB of BUCK IC, which can compensate the loss of PCB power traces impendance, and improve the real-time of dynamic adjustment power supply.

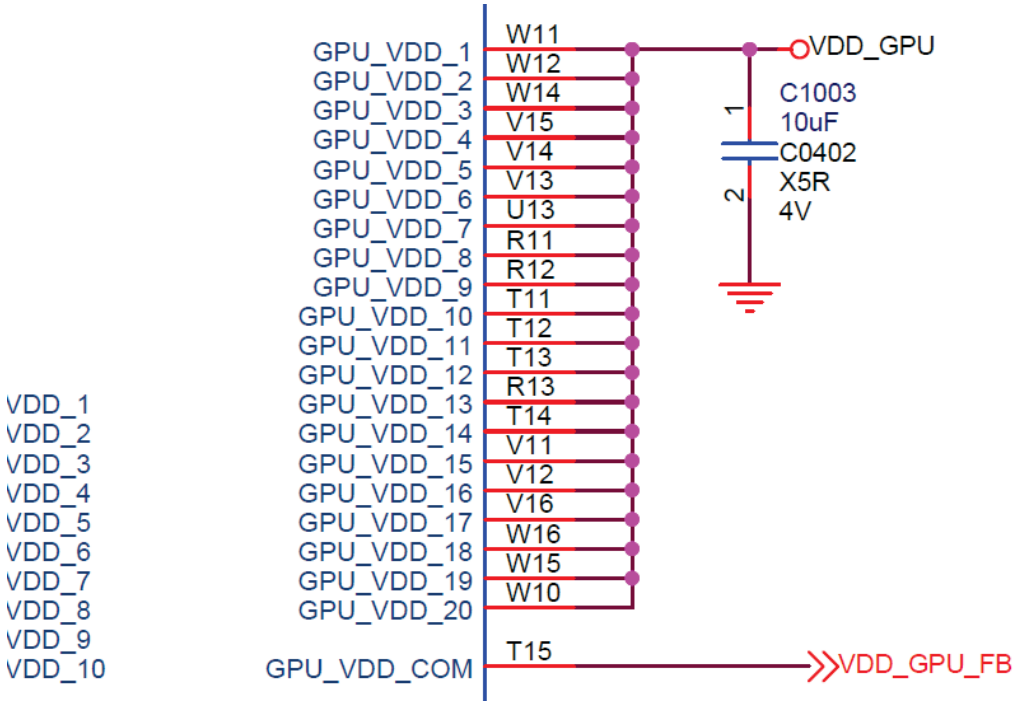


Figure 3-17 RK3399 VDD_GPU_COM Power Feedback

- 3.2.2.5 LOGIC Power Supply

RK3399 has two digital logic parts; LOGIC and CENTLOGIC.They are independent power domain, VDD_LOGIC power for LOGIC, and VDD_CENTERLOGIC power for CENTERLOGIC. The power domains include the following logical sections.

VD_LOGIC	PD_ALIVE	CRU, PLL, GRF, TIMER, WDT, GPIO, INTR_ARB
	PD_PERI_LP	NOC, EFUSE, SRAM, ROM, CRYPTO, GIC, DMAC, DCF, I2S_8CH, SPDIF, UART, I2C, MAILBOX, SPI, SARADC, TSADC, Cortex-M0
	PD_PERI_HP	USB2, SD/MMC, SDIO, PCIe
	PD_EMMC	eMMC
	PD_GMAC	GMAC
	PD_USB3	USB3.0/2.0
	PD_EDP	eDP
	PD_VIO	MIPI
	PD_ISP0	ISP0
	PD_ISP1	ISP1
	PD_VOPB	VOP_BIG
	PD_VOPL	VOP_LIT
	PD_HDCP	HDCP2.2, HDMI, DP, Gasket
VD_CENTER	PD_CENTER	DDRC, Memory Scheduler, DFI_MONITOR, CIC
	PD_VDU	RKDEC
	PD_VCODEC	VCODEC
	PD_IEP	IEP
	PD_RGA	RGA

Figure 3-18 RK3399 Digital Logic Parts

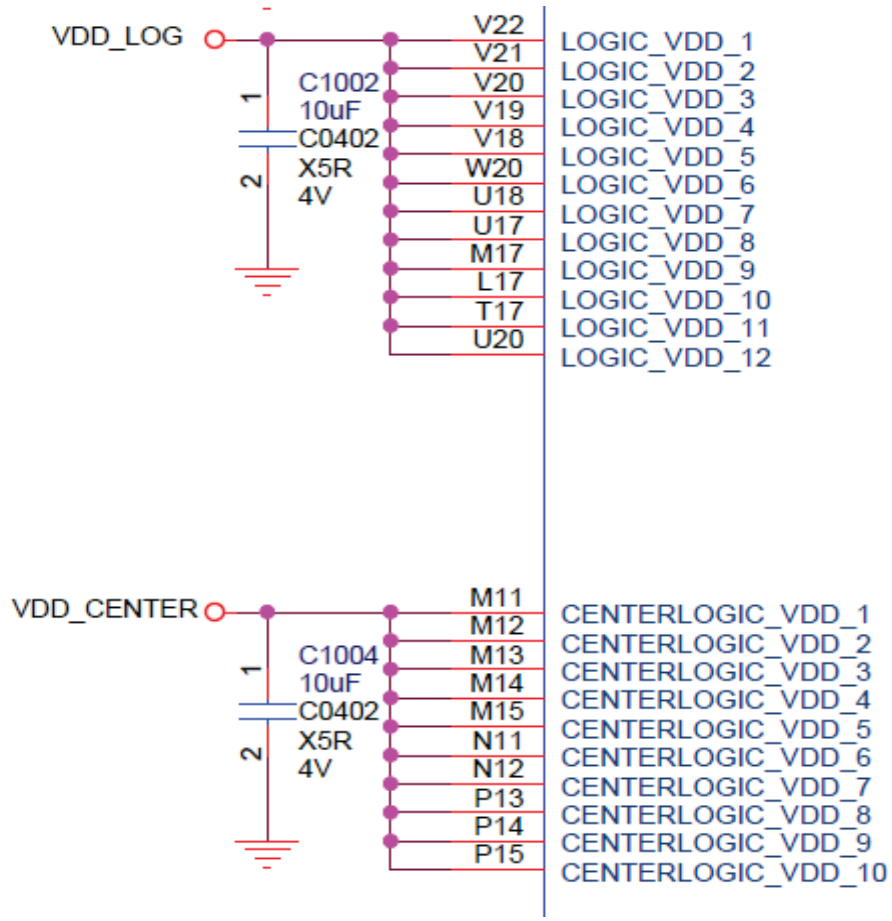


Figure 3-19 RK3399 Digital Logic Power Supply

According to the different GPIO level values (1.8 v / 3.0 v) in the pmuio2 power domain, the parameters of the PWM circuit devices in the vdd _ log power supply design corresponding to log_DVS_PWM are different, and should be paid attention to in the design, shown in figure 3 – 20&3 - 21.

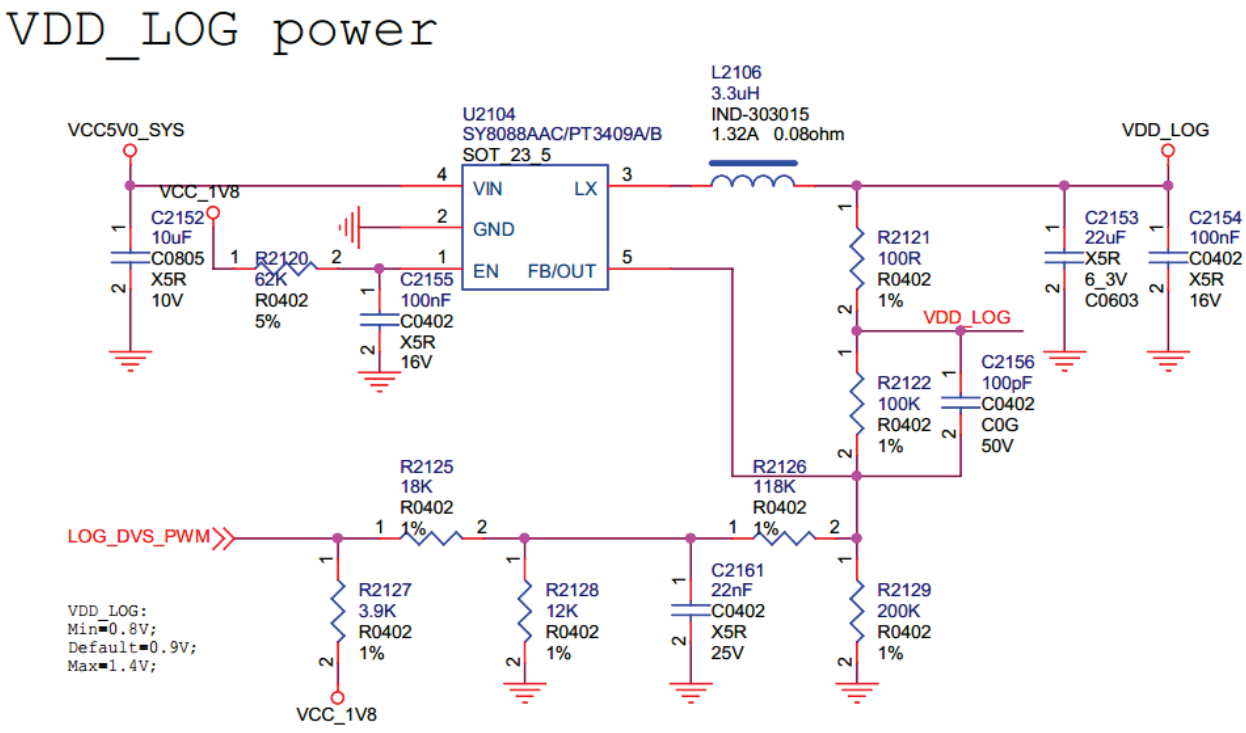


Figure 3-20 RK3399 VDD_LOG Power Supply at 1.8V mode

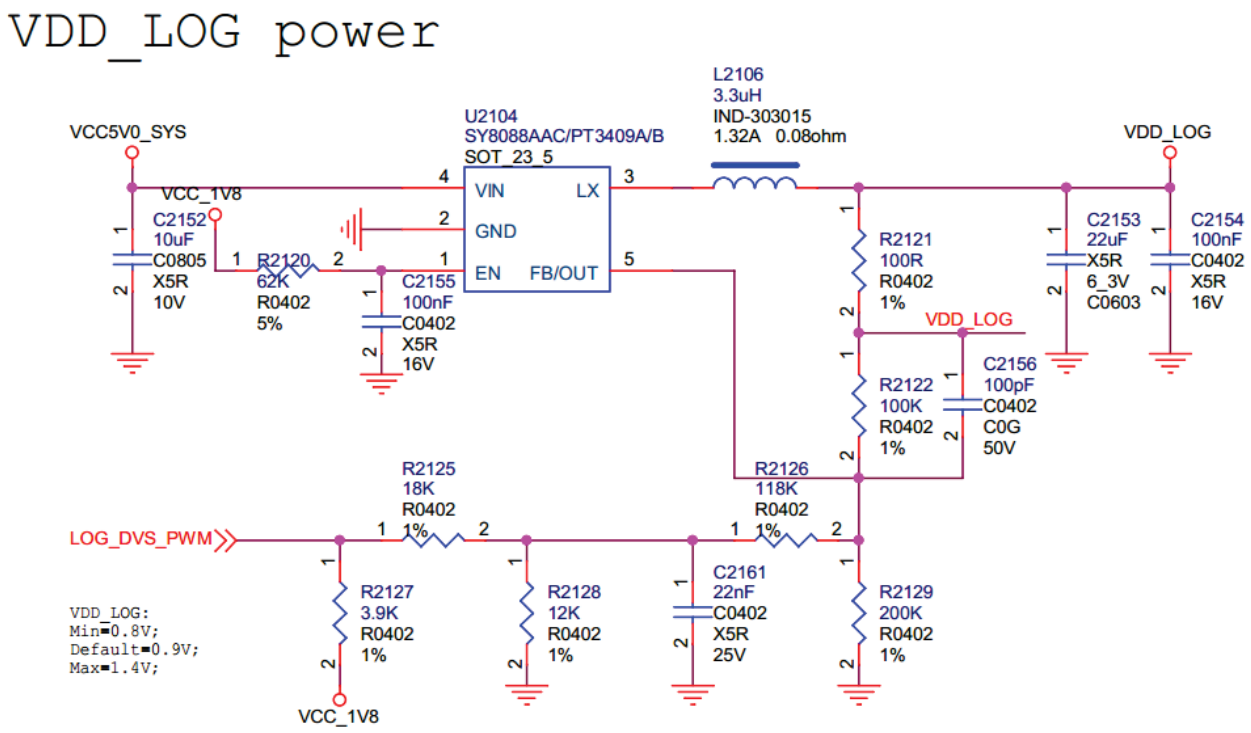


Figure 3-21 RK3399 VDD_LOG Power Supply at 3.0V mode

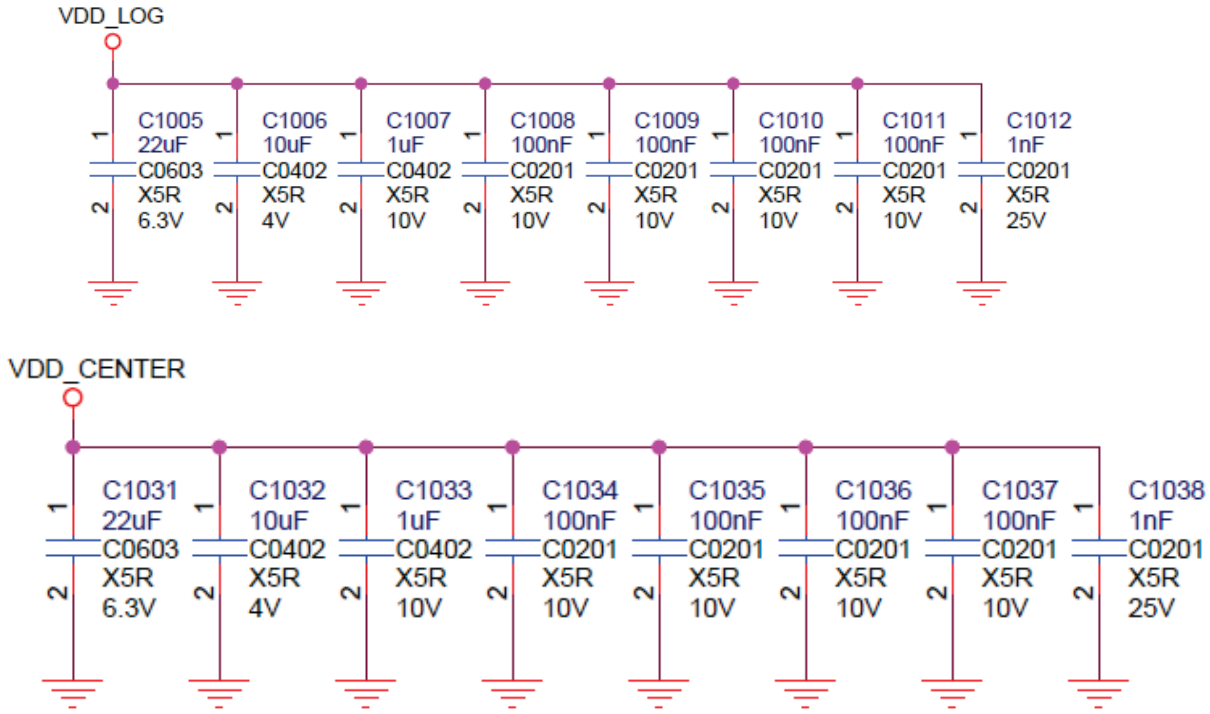


Figure 3-22 RK3399 Logic Power Filter Capacitors

- 3.2.2.6 DDR Power Supply

RK3399 DDR controller compatible with DDR3/LPDDR3/LPDDR4 protocol.Embedded Vref circuit generates the reference voltage VCCDDR/2.

The Vref of LPDDR3 DRAM can be adjusted according to the ODT value and the drive strength.

E.g.:

At 800MHz frequency,RK3399 DDR controller drive strength is 34.3ohm, DRAM ODT is 240ohm,so when ODT enable, DRAM Vref=0.56*VDDQ.

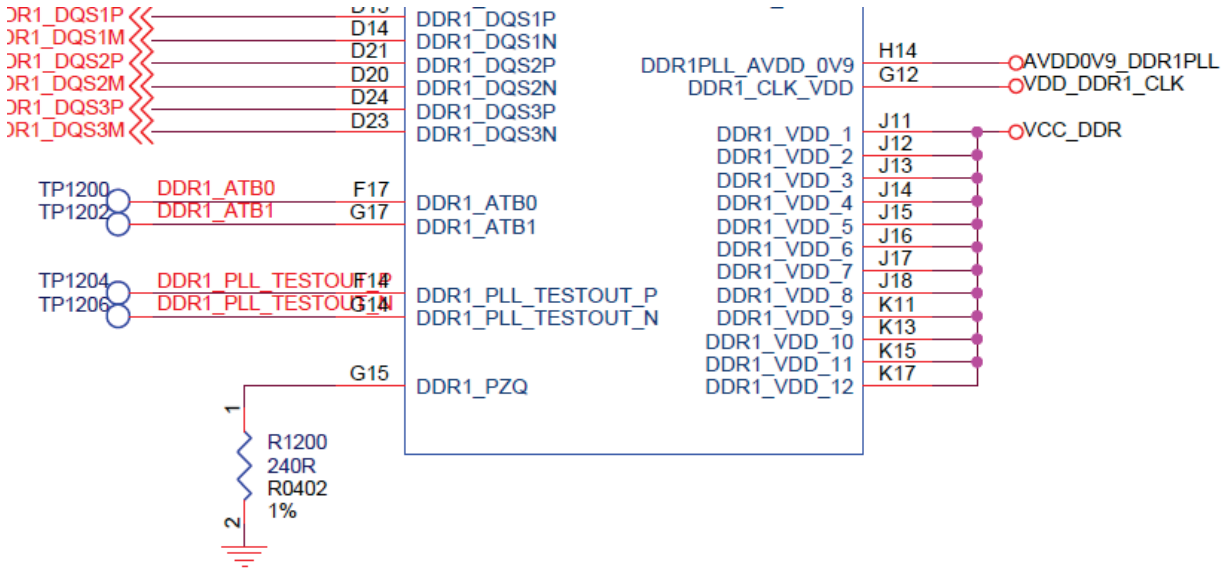


Figure 3-23 RK3399 DDR Controller Power Supply

RK3399 DDR controller's clock is generated by a separate PLL, it needs a separate power supply（DDR0PLL_AVDD_0V9, DDR1PLL_AVDD_0V9）. Each DDR PLL power pin needs a 100nF decoupling capacitor, and should be placed close to it.

DDR0_CLK_VDD and DDR1_CLK_VDD from VCC_DDR are power supply for RK3399 DDR CLKP/CLKN signals.It is recommended to use a series resistor to avoid the power noise from VCC_DDR power plane. Each power pin needs a 100nF decoupling capacitor, and should be placed close to it.

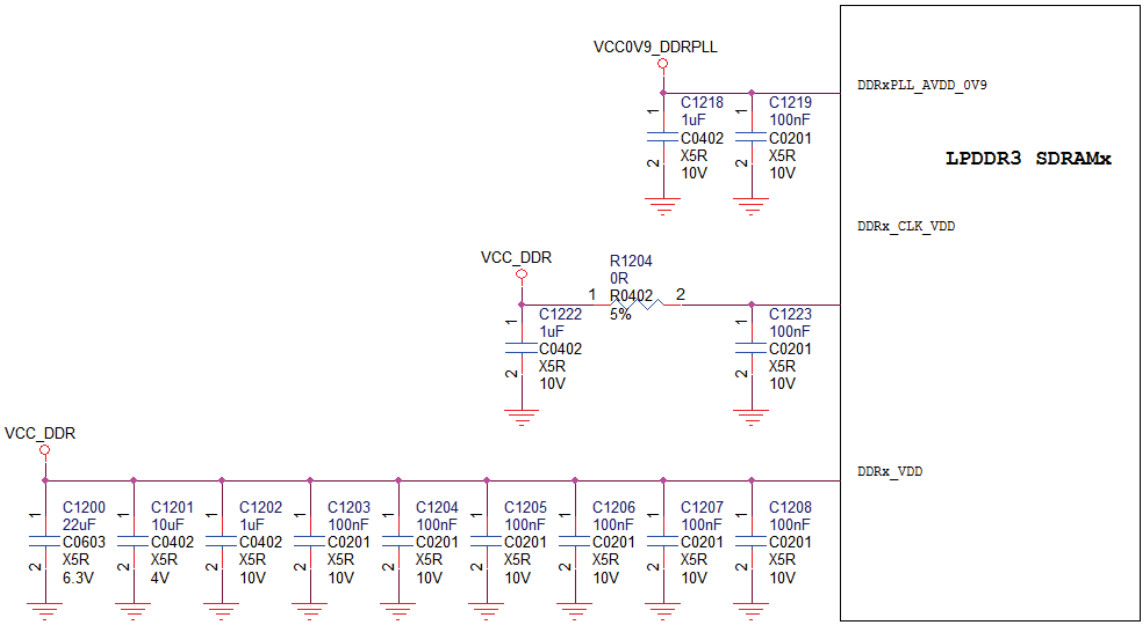


Figure 3-24 RK3399 DDR Controller Power Supply

The DRAM VREF_DQ and VREF_CA of DDR3 use a separate Vref reference circuit. The Vref_DQ can be power supplied by a 1K ohm resistors divider (1% accuracy), and for reduce power consumption Vref_CA usually be power supplied by a 10Kohm resistors divider (1% accuracy).Each power pin should be placed a 1nF decoupling capacitor.

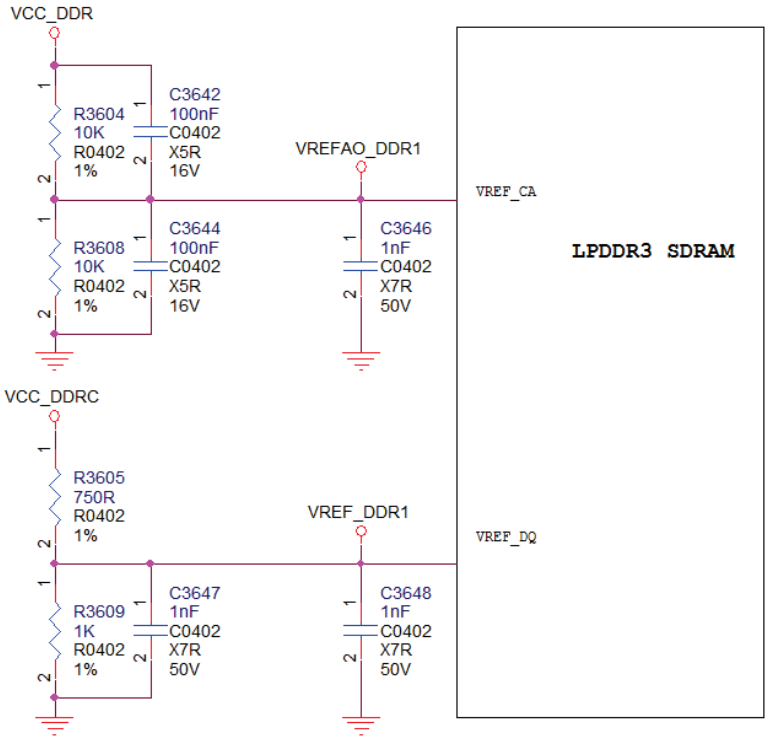


Figure 3-25 RK3399 LPDDR3 DRAM Vref Power Supply

- 3.2.2.7 GPIO Power Supply

Refer to Section 2.3.1 for GPIO power supply, it recommended to place a 100nF decoupling capacitor close to each power pin. For detailed design please refer to RK3399 reference design schematic.

3.2.3 RK808-D PMIC Introduction

- 3.2.3.1 RK808-D Block Diagram

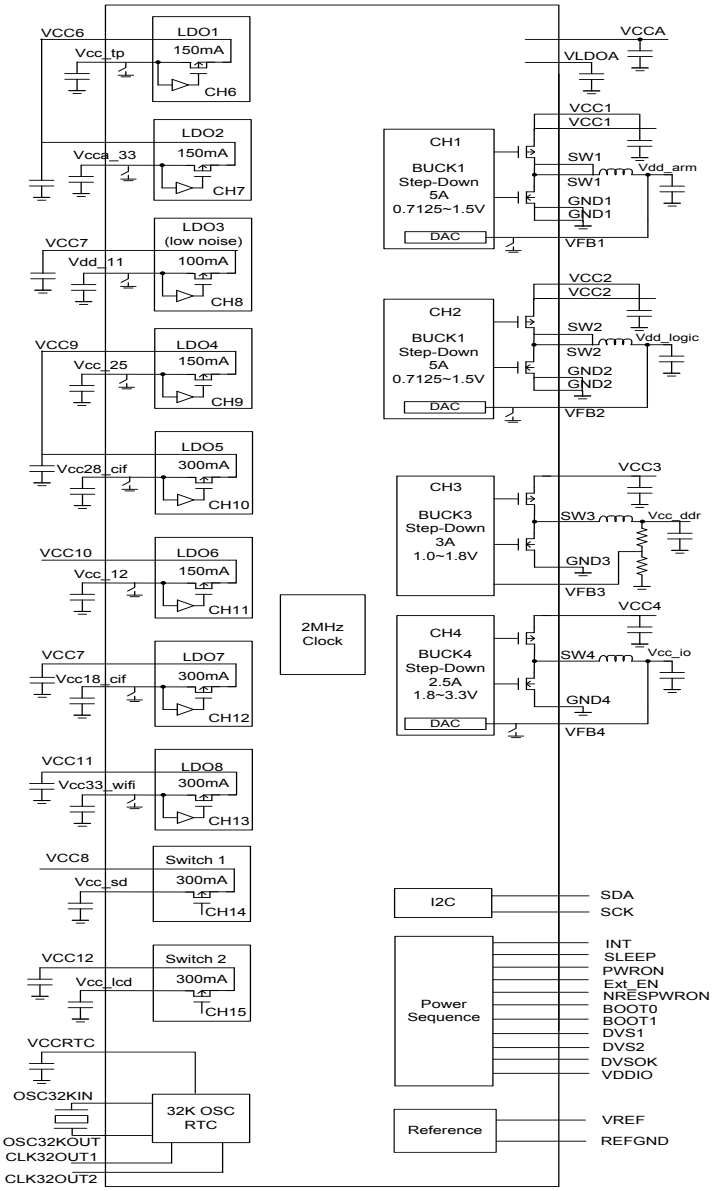


Figure 3-26 RK808-D Block Diagram

- 3.2.3.2 RK808-D Features

  - Input voltage:2.7V-5.5V
  - Instant 2MHz PWM architecture to achieve fast transient responses
  - Embedded RTC with two 32.768k clock output
  - Internal loop compensation and soft start function
  - I2C programmable output level and power-up sequence control
  - High conversion efficiency circuit architecture
  - Discharge function
  - Power supply capacity
    - Channel 1:Synchronous step-down DC-DC converter,5A max
    - Channel 2:Synchronous step-down DC-DC converter,5A max
    - Channel 3:Synchronous step-down DC-DC converter,3A max
    - Channel 4:Synchronous step-down DC-DC converter,2.5A max
    - Channel 6,7,9,11: Low dropout linear regulator,150mA max
    - Channel 8:Low noise,high power supply rejection ratio low dropout linear regulator,100mA max
    - Channel 10,12,13: Low dropout linear regulator,300mA max
    - Channel 14,15:Low resistance switch,0.2ohm(Vgs=3V)

- OTP and programmable power-up timing control
- Package：7mmx7mm QFN68

- 3.2.3.3 RK3399+RK808-D Power Tree

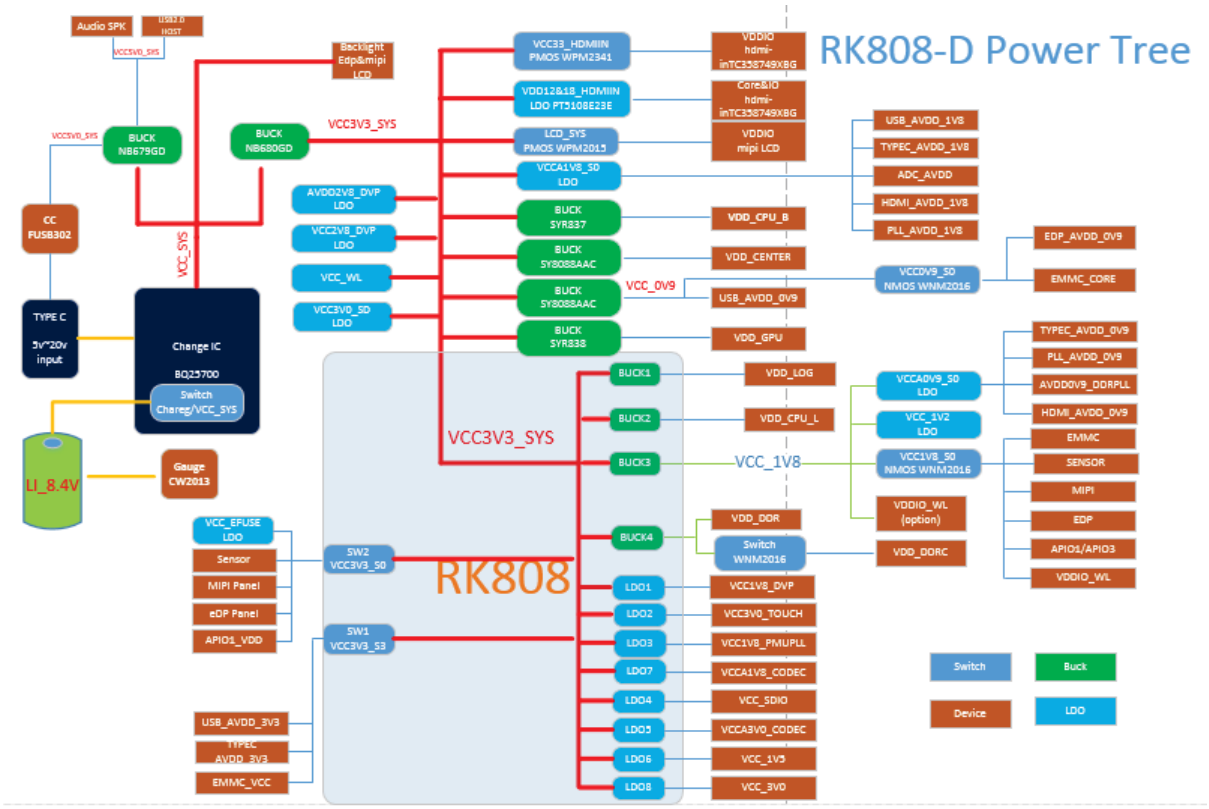


Figure 3-27 RK808-D Power Tree

- 3.2.3.4 RK808-D Application Block Diagram

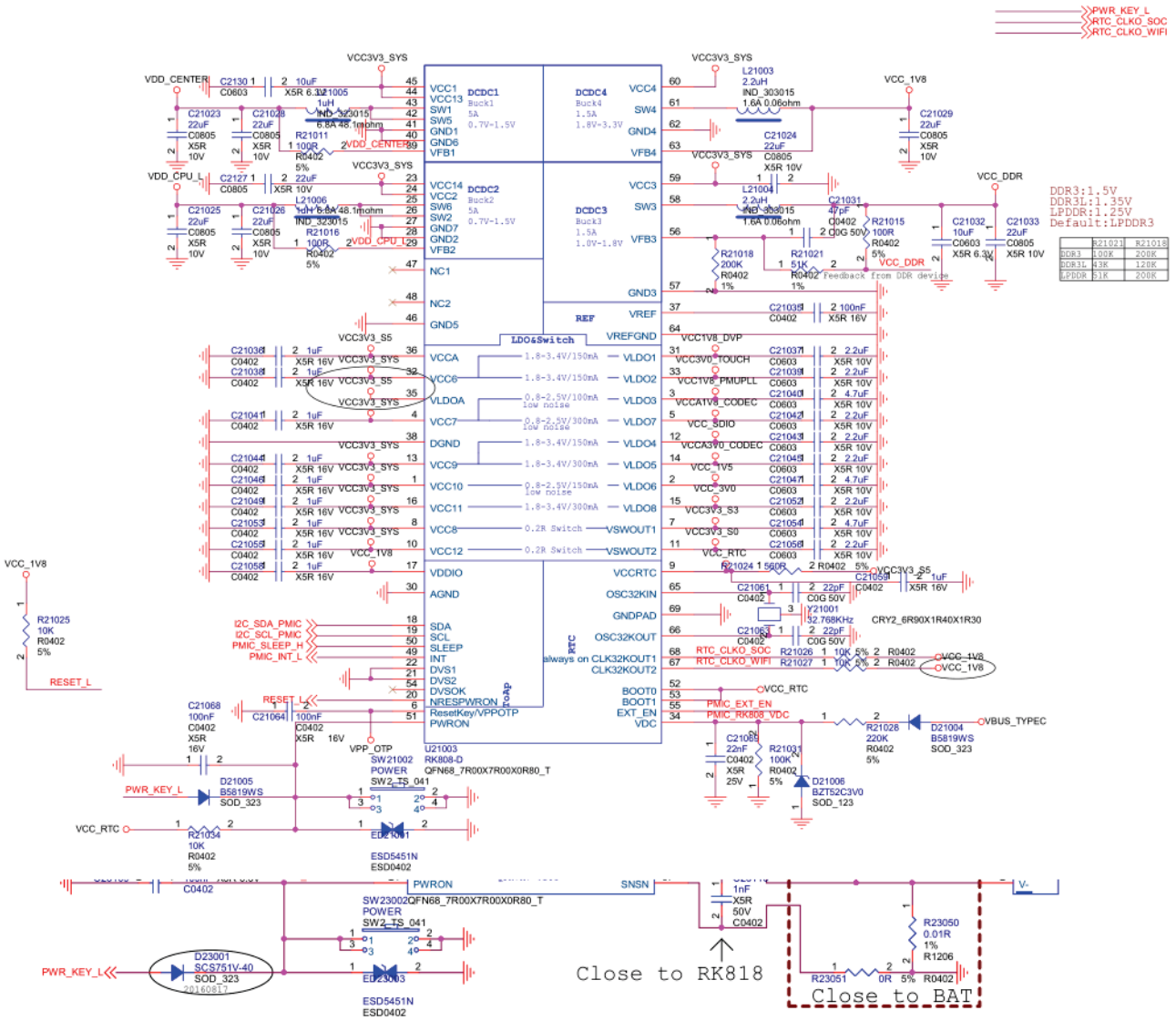


Figure 3-28 RK808-D Application Block Diagram

- 3.2.2.5 RK808-D Notes
  - The load capacitance of the crystal is 22pF, and the user can fine-tune the crystal according to the crystal specifactions.

Notes:

In order to reduce the power consumption PMIC RTC crystal oscillation driving is relatively weak, can not measured signal on the XOUT or XIN pin with a normal oscilloscope, or oscilloscope probe will cause OSC stop working, to measure this signal please measure CLK32KOUT output pin.

  - When VDC pin input voltage level is within 0.6V and 1.8V, and maintain more than 500mS .RK808-D is forced power-up, and could not power-off until the input voltage under 0.6V.
    - In the product need to be automatically boot when plug in the DC power supply. and the power-on/off is through the power switch or plug off the DC power to achieve, it can be consider the direct use of resistor divider,Shown as Figure 3-29.

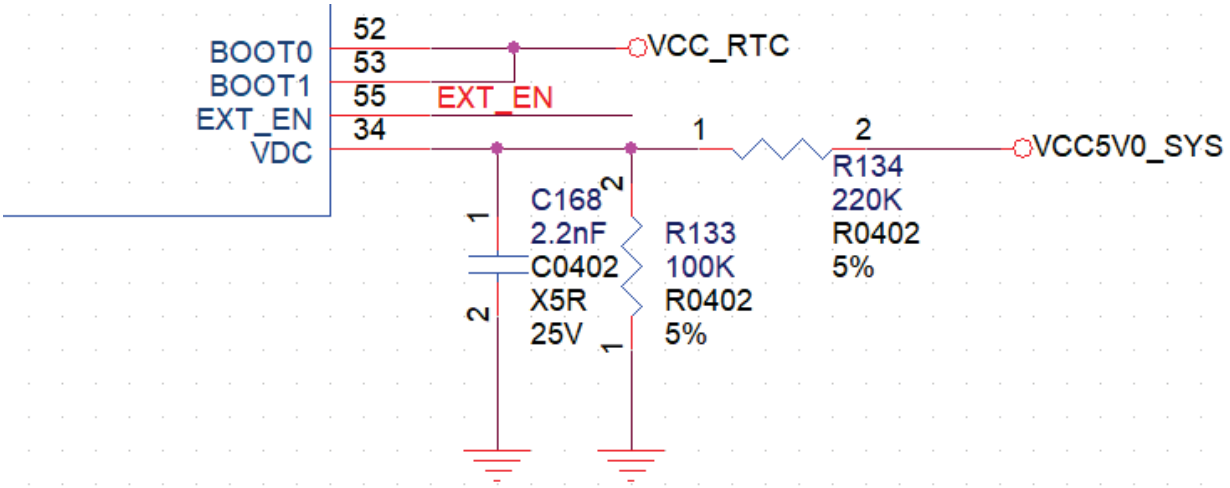


Figure 3-29 VDC Application Circuit 1

- In the productor need to be automatically boot and can be powered down use power-key. the level of VDS must to be pulled-up when PMIC boot, and should to be pulled-down after about 500ms . Shown as Figure 3-30.

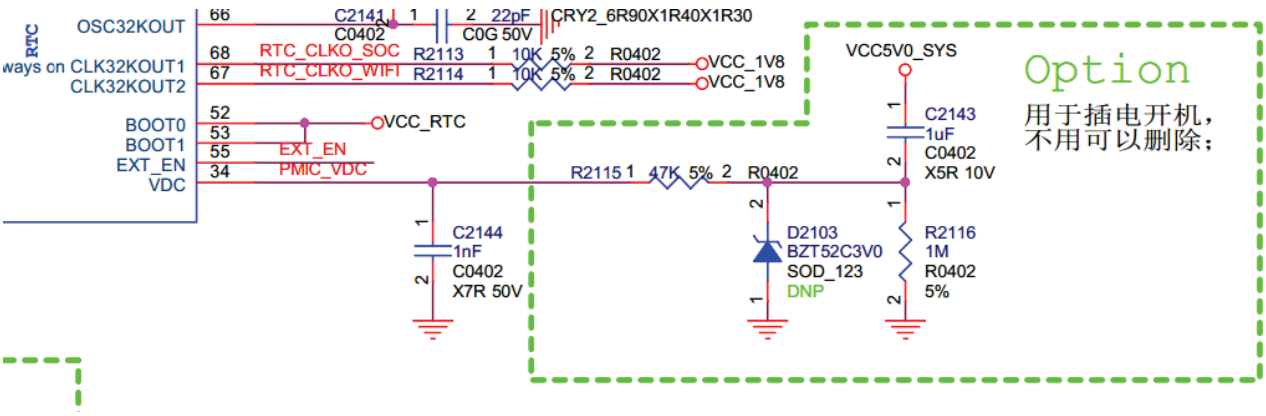


Figure 3-30 VDC Application circuit 2

- In the productor need to be power up/off use only power-key,the pin of VDC only need to be a capacitor to GND(VDC could not floating),shown as Figure 3-31.

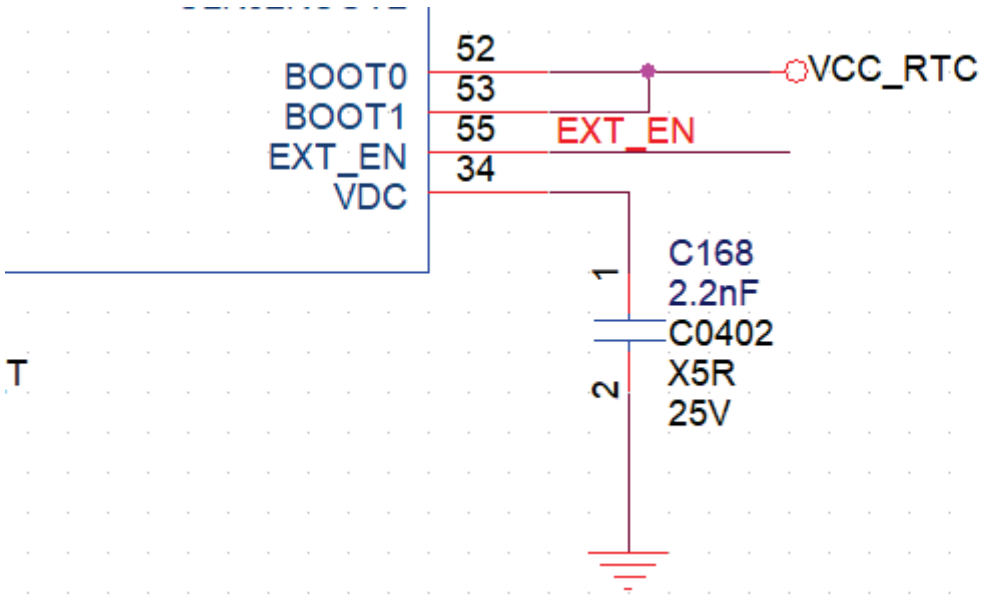


Figure 3-31 VDC Application circuit 3

- To ensure the power quality, BUCK1 and BUCK2 output filter capacitor value must be bigger

than 33uF, especially in the high current and high dynamic load case; it needs to increase the value of filter capacitor.

- RK808-D maximum input voltage is 5.5V, If the adapter directly supplies to the RK808-D, the input-end of RK808 must to be added a TVS (Recommended model: AZ5825-01F, the detail refer to section 3.2.4.5), to prevent the surge voltage over 5.5V or more. If RK808-D power supply from the BUCK, the voltage is more stable, no need TVS.
- If the ResetKey/VPPOTP pin is pulled high level during working (the voltage as the same as VCCRTC) and last 10ms, RK808-D will issue a shutdown signal, then automatically restart.
- When the PWRON pin is pulled up to VCCRTC by resistor for more than 500ms RK808-D will automatically power-up.If the PWRON pin is pulled down for more than 6 seconds, RK808-D will force shutdown (usually for the system crash forced shutdown and restart).During power-sleep and wake-up operation, the low level of the PWRON pin needs to be maintained above 30mS.
- RK808-D power-up process
  - VCC_RTC must been power supplied
  - RTC circuit working stably
  - VCCA voltage more than 3V
  - One of the following three cases is occurring: PWRON be pulled down and be maintained more than 500mS; VDC voltage level is within 0.6V and 1.8V and be maintained more than 500mS;RTC alarm is enabled and in timeout.
  - When RK808-D power-up, each power output interval is about 2ms, until all power are completed, it will release the reset, power-up process complete

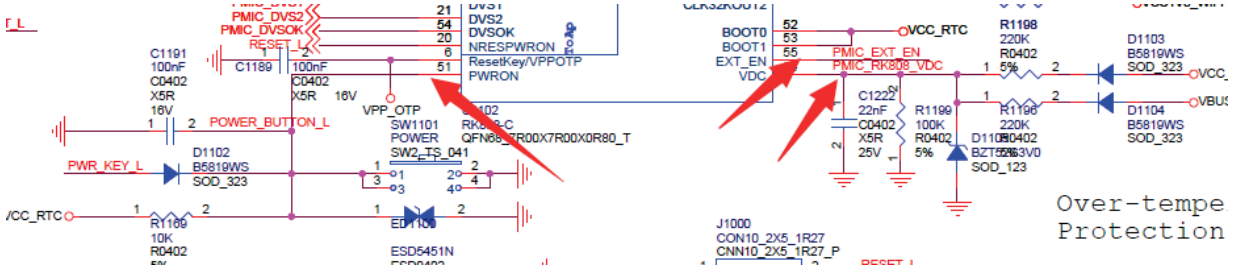


Figure 3-32 RK808-D Power-up Enable Pin

Notes:

RK808-D power-up timing is match with OT.You can select different power-up sequencing by setting BOOT0 and BOOT1.

- RK808-D power-down process
  - One of the following three cases is occurring: I2C write DEVICE_OFF=1 and VDC=0V, the PWRON be pulled down more than 6 s and VDC=0V, VCCA less than 3.0V.
  - During power-down, after one RTC clock cycle (about 30.5us) enable resets, and then after around 2ms all power output are shut down at the same time, power-down process complete.

- 3.2.3.6 RK808-D Design Description

RK808-D specific design instructions, please refer to the document "RK808 design guide Ver1.0" released by Rockchip.

3.2.4 RK818-3 PMIC Introduction

- 3.2.4.1 RK818-3 Block Diagram

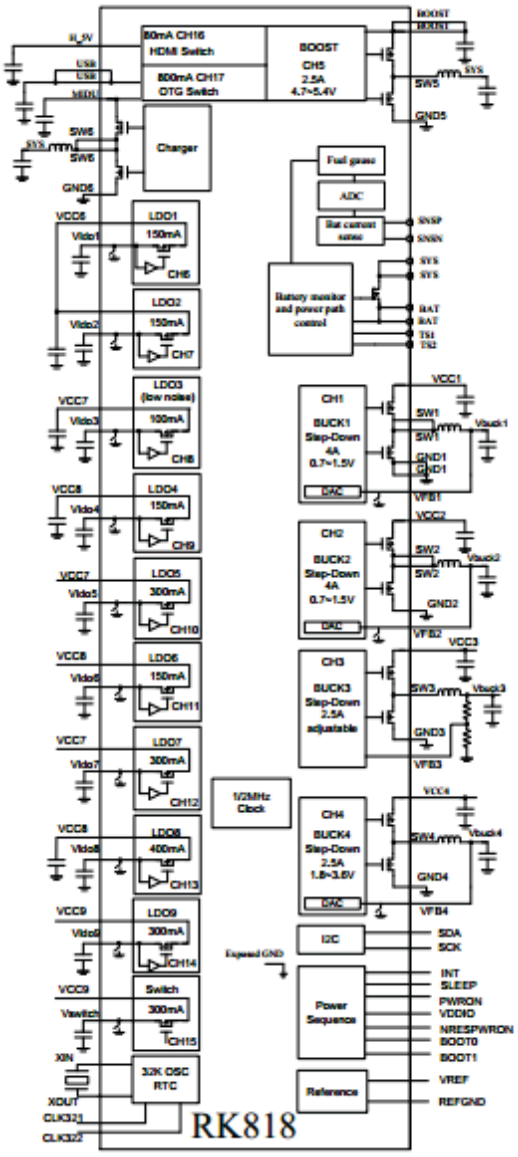


Figure 3-33 RK818-3 Block Diagram

- 3.2.4.2 RK818-3 Features

  - Input voltage:USB port is 3.8V-5.7V,BAT port 3.0V-4.35V
  - Maximum 3A charging current,with power switch
  - Maximum 5A automatic power path management
  - Embedded precision fuel gauge
  - Embedded RTC with two channels 32.768k clock output
  - Less than 40uA current in standby (at 32kHz clock frequency)
  - Switching frequency 2MHz step-down DC-DC converter
  - Switching frequency 1MHz step-up DC-DC converter
  - Current mode architecture with excellent transient response
  - Internal loop compensation and soft start function
  - I2C programmable output level and power-up sequence control
  - High conversion efficiency circuit architecture
  - Discharging function
  - Power supply capacity
    - Channel 1:Synchronous step-down DC-DC converter,4A max
    - Channel 2:Synchronous step-down DC-DC converter,4A max
    - Channel 3:Synchronous step-down DC-DC converter,2.5A max
    - Channel 4:Synchronous step-down DC-DC converter,2.5A max

- Channel 5:Synchronous step-up DC-DC converter,2.5A max
- Channel 6,7,9,11: Low dropout linear regulator,150mA max
- Channel 8:Low noise,high power supply rejection ratio low dropout linear regulator,°mA max
- Channel 10,12,14: Low dropout linear regulator,300mA max
- Channel 13: Low dropout linear regulator,400mA max
- Channel 15:Low resistance switch,0.15ohm(Vgs=3V)
- Channel 16:HDMI 5V power switch,80mA max
- Channel 16:USB OTG power switch,1000mA max

- OTP and programmable power-up timing control
- Package：7mmx7mm QFN68

- 3.2.4.3 RK3399+RK818-3 Power Tree

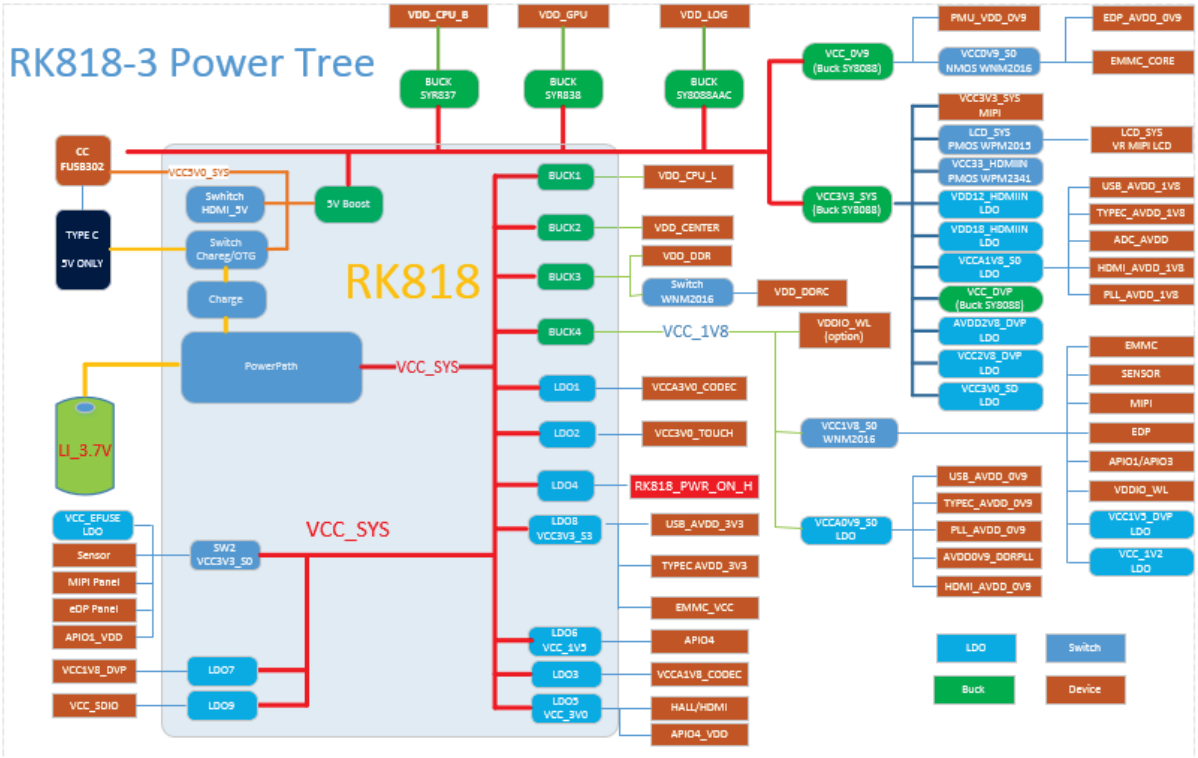


Figure 3-34 RK818-3 Block Diagram

- 3.2.4.4 RK818-3 Application Block Diagram

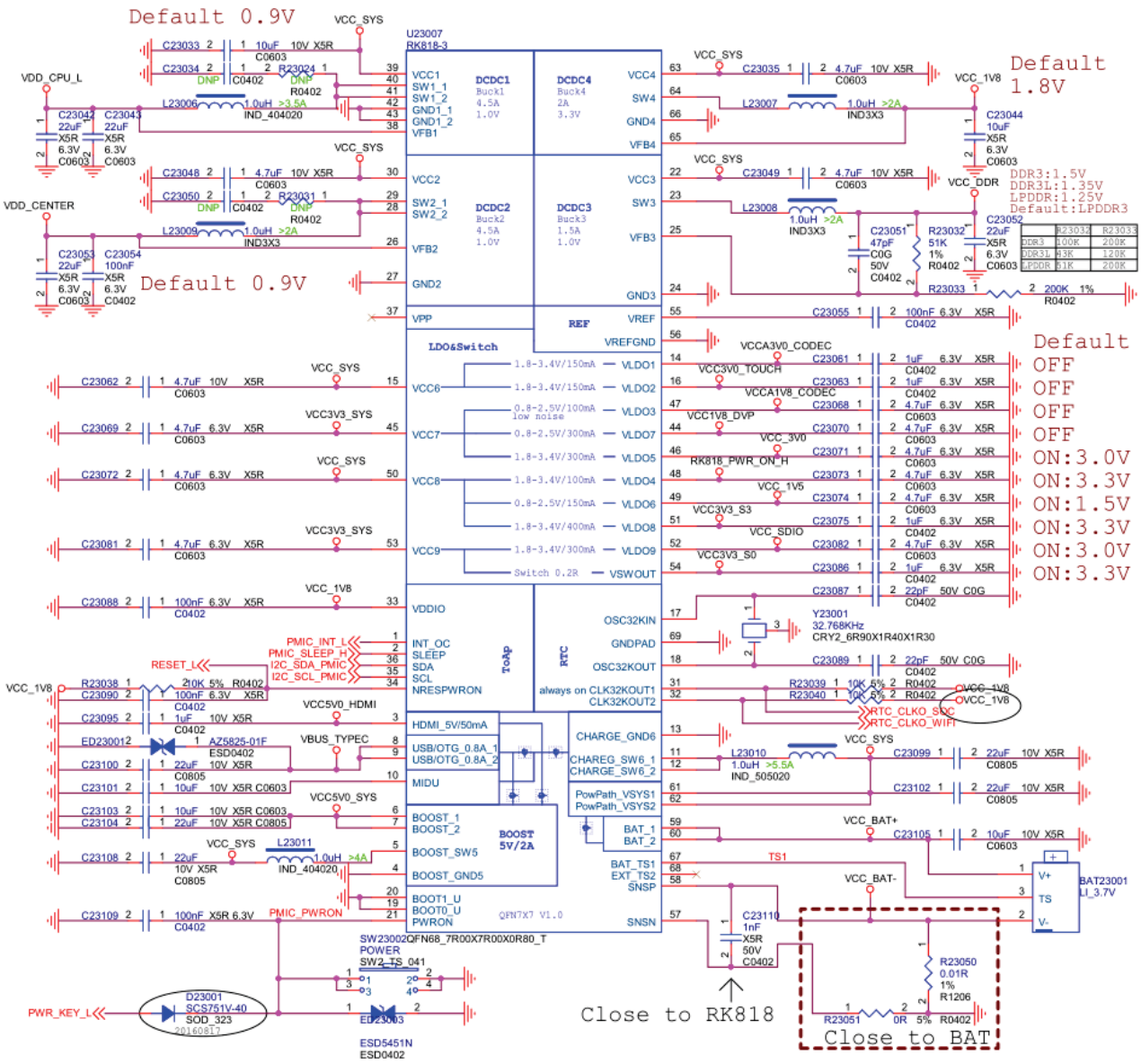


Figure 3-35 RK818-3 Application Block Diagram

- 3.2.4.5 RK818-3 Note
  - The loading capacitance of the crystal is 22pF, and the user can fine-tune the value according to the crystal specification.

Notes:

In order to reduce the power consumption, the PMIC RTC crystal oscillation driving is relatively weak, the signal of the XOUT or XIN pin could not be measured with a normal oscilloscope , or oscilloscope probe will cause OSC stop working, please measure the signal on the CLK32KOUT output pin.

  - To ensure the power quality, the BUCK1 and BUCK2 output filter capacitor value must be greater than 33uF, especially in the high current and high dynamic load case; it needs to increase the value of filter capacitor.
  - RK818-3 maximum input voltage is 5.7V, to prevent USB port voltage over 5.7V or more by the surge voltage, the pin 8 and pin 9 of RK818-3 need to add TVS, which is very important. It is recommended model: AZ5825-01F, which meet the ESD immunity requirements of IEC

61000-4-2, level 4 (±15Kv air, ±8kV contact discharge). The TVS application design shown as Figure 3-37; protected line is connected at pin 1, and the pin 2 is connected to a ground plane on the PCB.In order to minimize parasitic inductance in the traces, all path lengths connected to the pins of TVS should be kept as short as possible. The absolute maximum ratings parameter index of AZ8525-01F shown as Figure 3-38.If the TVS wanted be replaced with other models, it is must to meet the parameters requirements in the Figure 3-38.

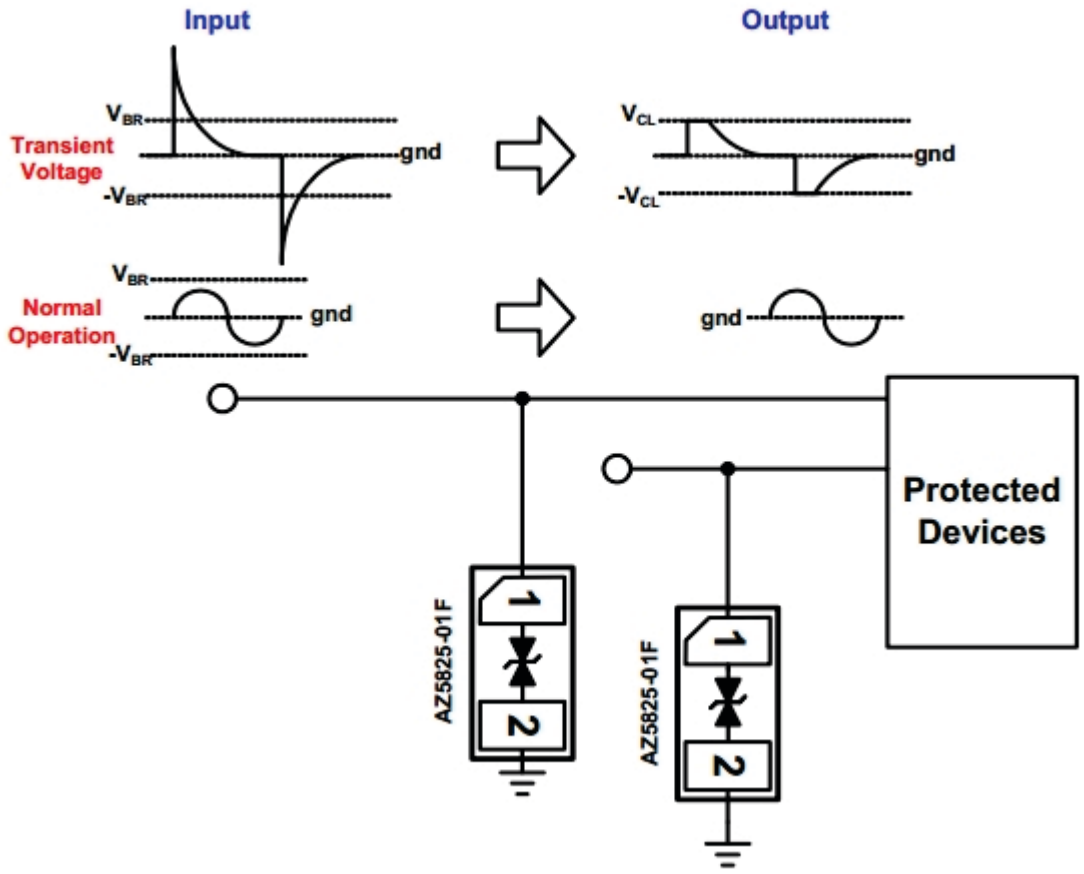


Figure 3-36 AZ5825-01F Application Design

PARAMETER	PARAMETER	RATING	UNITS
Peak Pulse Current (tp=8/20μs)	I_{PP}	18	A
Operating Supply Voltage (pin-1 to pin-2)	V_{DC}	5.5	V
ESD per IEC 61000-4-2 (Air)	V_{ESD}	±30	kV
ESD per IEC 61000-4-2 (Contact)		±30	
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	℃
Operating Temperature	T_{OP}	-55 to +85	℃
Storage Temperature	T_{STO}	-55 to +150	℃

Figure 3-37 AZ5825-01F Absolute Maximum Ratings

- RK818-3 has 5V BOOST with max 2A load capacity, but it has no short-protect function, so a current limit IC is needed if using the function. RK818-3 USB OTG power-switch (PIN8, PIN9 output) with a built-in 700-1000mA optional current limit.
- The RK818-3 PWRON pin is needed connect to RK3399 GPIO by an isolation diode, the pin internal pull-up resistor value is bigger, when the diode leakage is higher, which may make the voltage of PMIC-PWRON less than 2.0V, and will be mistaken as power key enabled and then RK818-3 could not work properly.So, you should use a diode with leakage less than 0.55V. SCS751V-40 is recommended,shown as Figure 3-39.

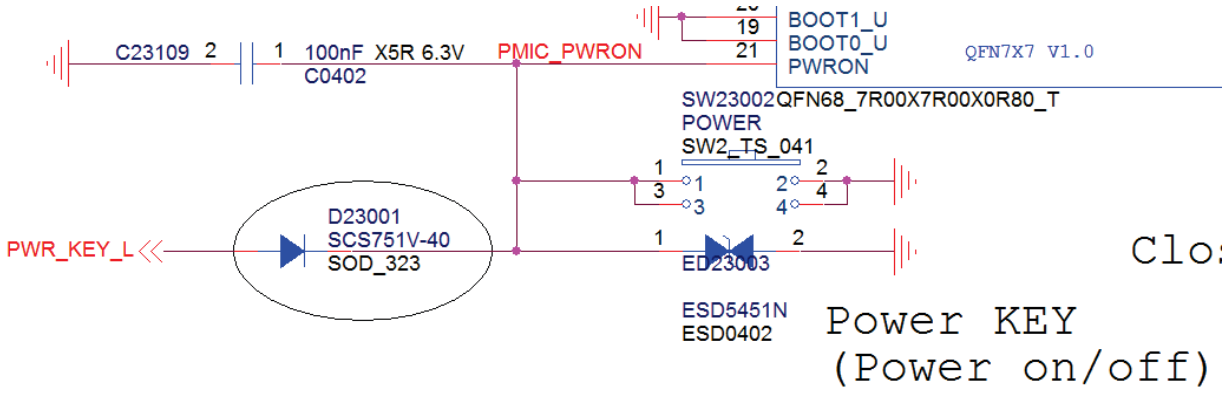


Figure 3-38 RK818-3 PWRON Isolation Diode

- In single-cell lithium battery design, the battery voltage will be easy to cause collapse due to excessive load, and the fuel gauge detect the battery voltage lower than the preset power-off voltage and then enter the power-off process, resulting in insufficient battery capacity.So it needs to widen the power trace width, increase vias or any favorable method to minimize the power circuit and the battery impedance. Power circuit impedance is shown as below red arrow.

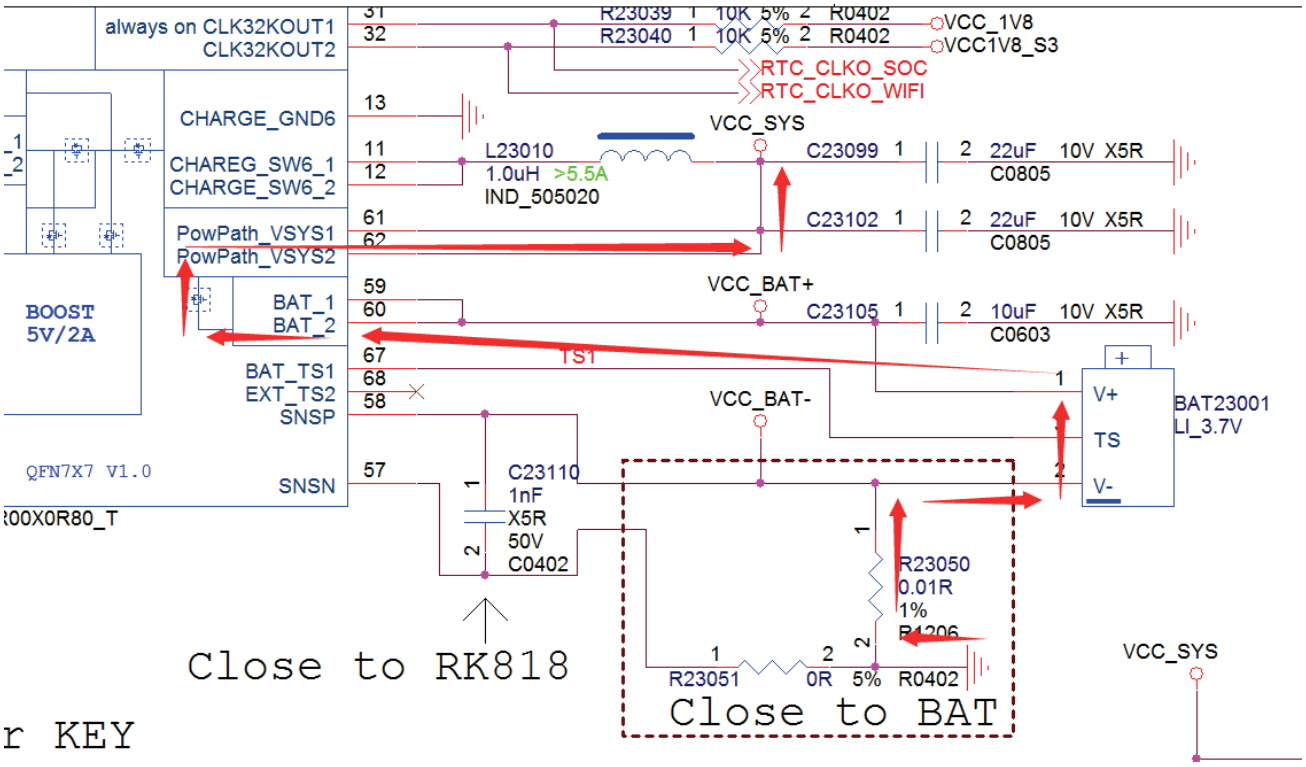


Figure 3-39 RK818-3 Battery Discharge Path

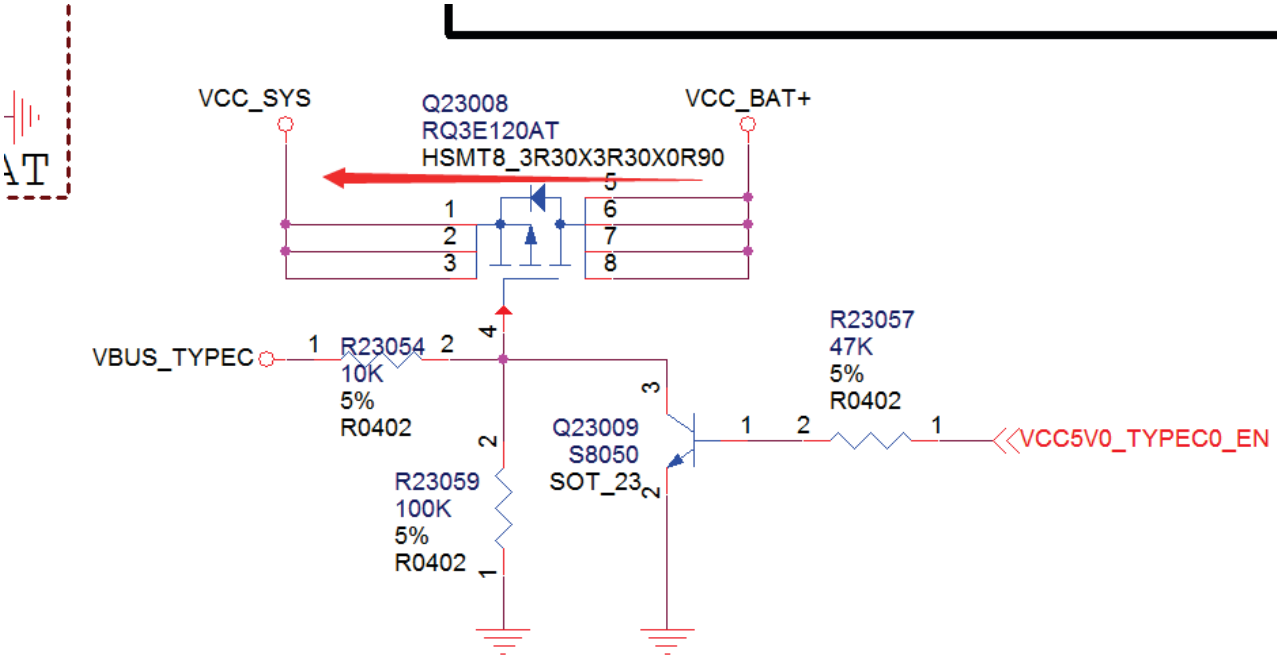


Figure 3-40 RK818-3 Power Manage Path

- 3.2.4.6 RK818-3 Design Description

  RK818-3 specific design instructions, please refer to the document "RK818 design guide" released by Rockchip.

3.2.5 Type-C Power Introduction

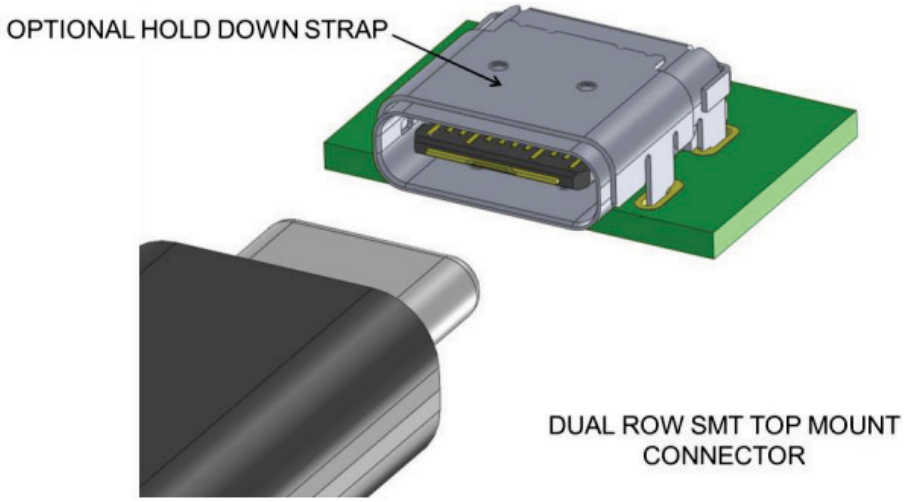


Figure 3-41 Type-C Port

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1−	VBUS	CC1	D+	D−	SBU1	VBUS	RX2−	RX2+	GND
GND	RX1+	RX1−	VBUS	SBU2	D−	D+	CC2	VBUS	TX2−	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Figure 3-42 Type-C Interface Signal（Front View）

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2−	VBUS	SBU1	D−	D+	CC	VBUS	TX1−	TX1+	GND
GND	TX2+	TX2−	VBUS	VCONN			SBU2	VBUS	RX1−	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

Figure 3-43 Type-C Interface Signal（Front View）

- 3.2.5.1 Type-C Port Features

Type-C Port Description

- VBUS:USB cable bus power
- GND:USB cable return current path
- TXn+/TXn-/RXn+/RXn-:USB3.0/3.1 USB3.0/3.1 SuperSpeed USB serial differential data pair
- D+/D-:USB2.0 HighSpeed differential data pair
- CC:Use for connection detect,interface configuration and Vconn
- VCONN:USB plug power
- SBU1/2:Sideband Use

- 3.2.5.2 Type-C CC Introduction

The CC channel is used for connection detect, interface configuration and Vconn.In DFP mode, VBUS has no voltage output, but it will inform the peripheral it's default power capacity by pull-up current.When a peripheral (UFP) inserted, CC line will be pulled-down by a 5.1K resistor, than VBUS will output 5V, DFP will adjust output voltage by consulting with UFP by CC lines (PD function).

- 3.2.5.3 RK808-D Type-C Circuit

RK808-D+BQ25700 can support type-c PD charging protocol cooperate with the CC IC.It is mainly used

in multi-cell lithium battery product solutions.The charge circuit is shown as Figure 3-45,RK808-D related circuit refer to the section 3.2.3.

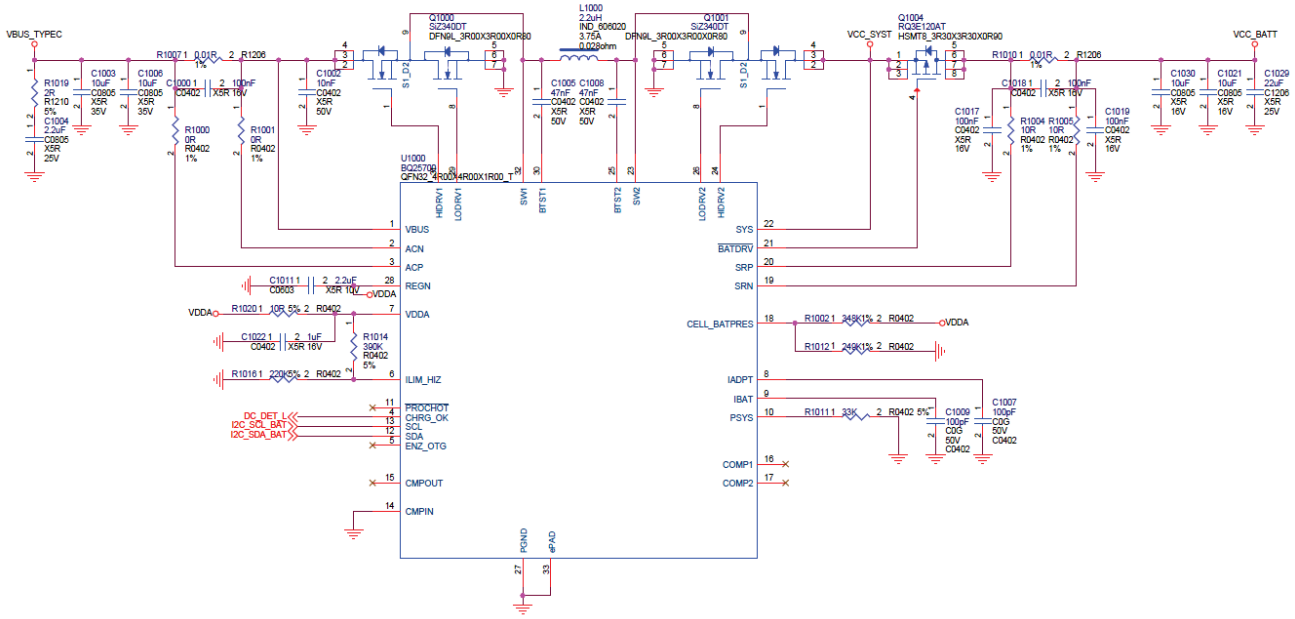


Figure 3-44 BQ25700 Type-C Charge Circuit

- 3.2.5.4 RK818-3 Type-C Circuit

RK818-3 can not support type-c PD charging protocol and high voltage input ,can only support 5V/900mA,5V/1.5A,5V/3A input.But the circuit is simpler with low cost comparing to RK808-D+BQ25700, which suitable for small size PCB products. The detail refers to the section 3.2.4.

3.2.6 Other Circuit

- 3.2.6.1 Over-temperature Protection Circuit

When RK3399 is over-temperature or crash, the OTP_OUT_H pin will output a high level signal to the VPP_OTP pin of RK808-D by level conversion circuit, or a low level signal to the reset pin of RK818-3 by level conversion circuit. RK808-D/RK818-3 will be forced power-down and restart.

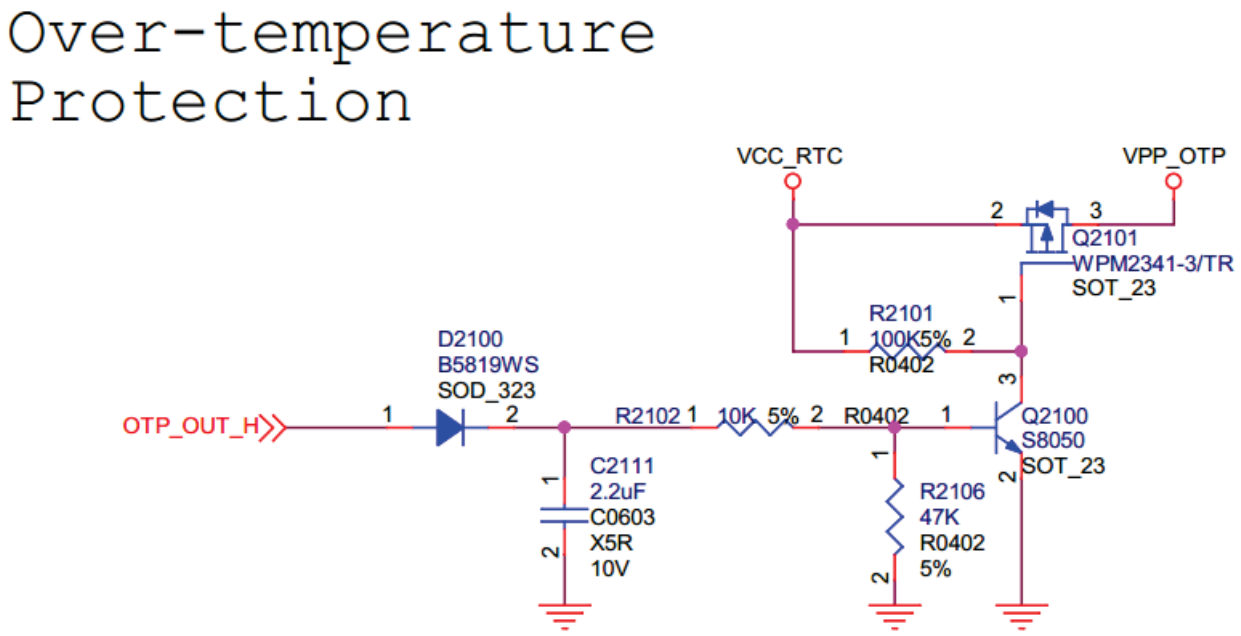


Figure 3-45 RK808-D Over-temperature Protection Circuit

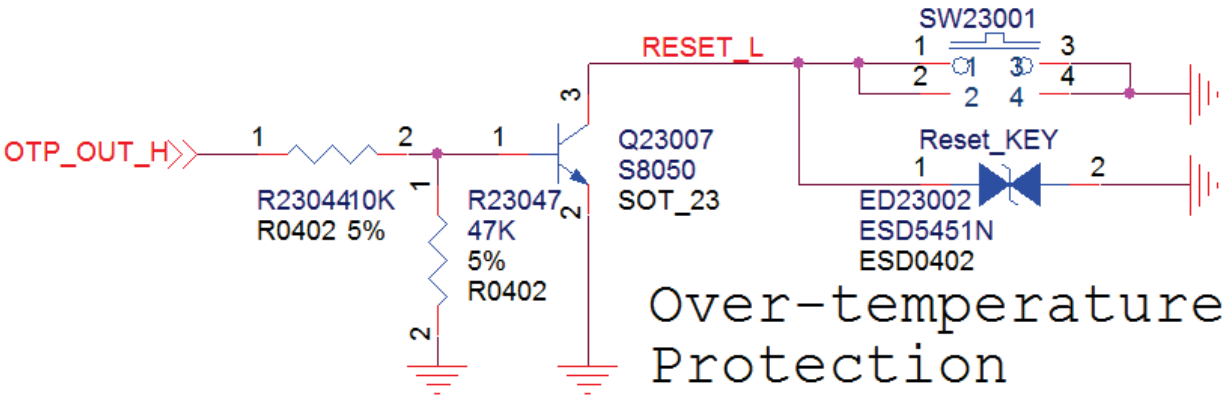


Figure 3-46 RK818-3 Over-temperature Protection Circuit

- 3.2.6.2 PMIC Power-sleep Circuit

When RK3399 enter standby mode, the PMIC_SLEEP pin will output a high level signal "PMIC_SLEEP_H", which will control PMIC into power-sleep mode according to the corresponding to software configuration, the power supply controlled by this signal is also powered off. When RK3399 is resumed from power-sleep, the PMIC_SLEEP pin will output a low level signal "PMIC_SLEEP_H" first timing, the PMIC and all the power supply will be back to normal work.

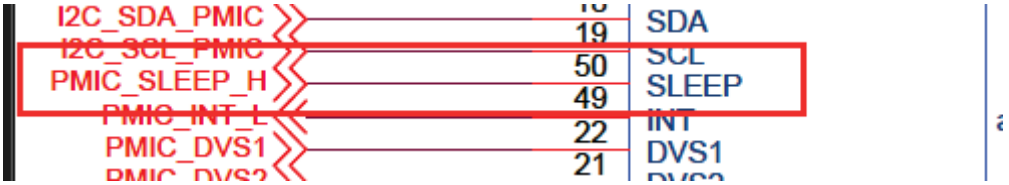


Figure 3-47 PMIC Power-sleep Input

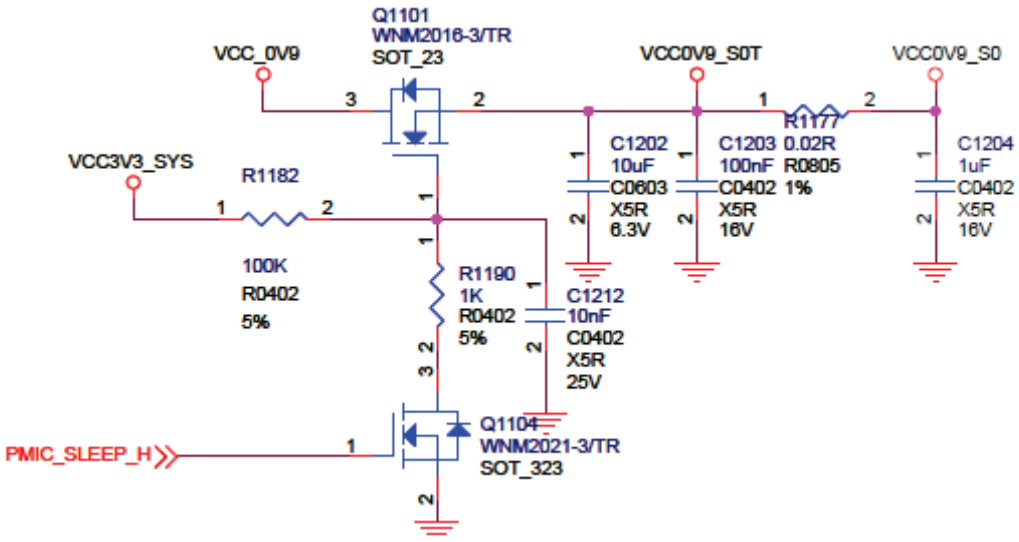


Figure 3-48 Power supply controlled by power-sleep signal

3.2.7 Power Supply Peak Current

The following table is the RK3399 BOX peak current test results, for reference only.The test conditions are shown as following:

- CPU_L maximum operating frequency:1.5GHz
- CPU_B maximum operating frequency: 1.8GHz
- GPU maximum operating frequency:800MHz
- DDR maximum operating frequency:800MHz,use 2x32bit LPDDR3(K4E6E304EB-EGCF)
- The oscilloscope turns on the 20MHz bandwidth limited

Table 3-8 RK3399 Peak Current

Power Supply	Voltage（V）	Peak Current(mA)
VCC5V0_SYS	5.00V	2493.0
VDD_GPU	0.97V	3880.0
VDD_CPUB	1.25V	4010.0
VDD_CPUL	1.08V	1480.0
VCC_DDR	1.26V	1440.0
VDD_LOG	0.90V	390.0
VDD_CENTER	0.91V	1050.0
VCC3V3_SYS	3.3V	760.0
VCC0V9_PMUPLL	0.9V	12.3
VCC0V9_USB	0.9V	20.6
VCC0V9_PCIE	0.9V	6.3
VCC0V9_PLL	0.9V	13.4
VCC0V9_EMMC	0.9V	3.4
EDP_AVDD_0V9	0.9V	1.0
HDMI_AVDD_0V9	0.9V	7.7
VCC_1V8	1.8V	260.0
VCC1V8_LCD(Mipi eDP)	1.8V	15.1
MIPI_TXO_AVDD_1V8	1.8V	8.8
EDP_AVDD_1V8	1.8V	1.9
HDMI_AVDD_1V8	1.8V	11.7
VCC1V8_EMMC	1.8V	234.3
VCC1V8_IO	1.8V	3.5
VCC1V8_ADC	1.8V	3.3
APIO5_VDDPST	1.8V	1.5
APIO5_VDD	1.8V	4.3
VCC_1V5	1.5V	17.4
VCC3V0_EMMC	3.0V	174.2
VCC3V0_IO(APIO4_VDD)	3.0V	13.5
VCC3V3_USB	3.3V	17.7
VCC3V3_PCIE	3.3V	170.6

3.3 Functional Interface Circuit Design Guide

3.3.1 Memory Card Circuit

RK3399 is embedded a SDMMC controller, compatible with SDMMC 3.0 protocol, shown as Figure 3-50.

- SDMMC controller has an independent power domain.
- SDMMC and UART2, AP JTAG, MCU JTAG function reuse, selected by SDMMC0_DET, please refer to section 3.1.4.
- Embedded a LDO and a power switch, SDMMC0_VDDPST only need to be connected a 100nF decoupling capacitor.
- SDMMC0_VDD is powered for SDIO, need to provide external 3.0V (SD 2.0) or 1.8V (SD 3.0) power.

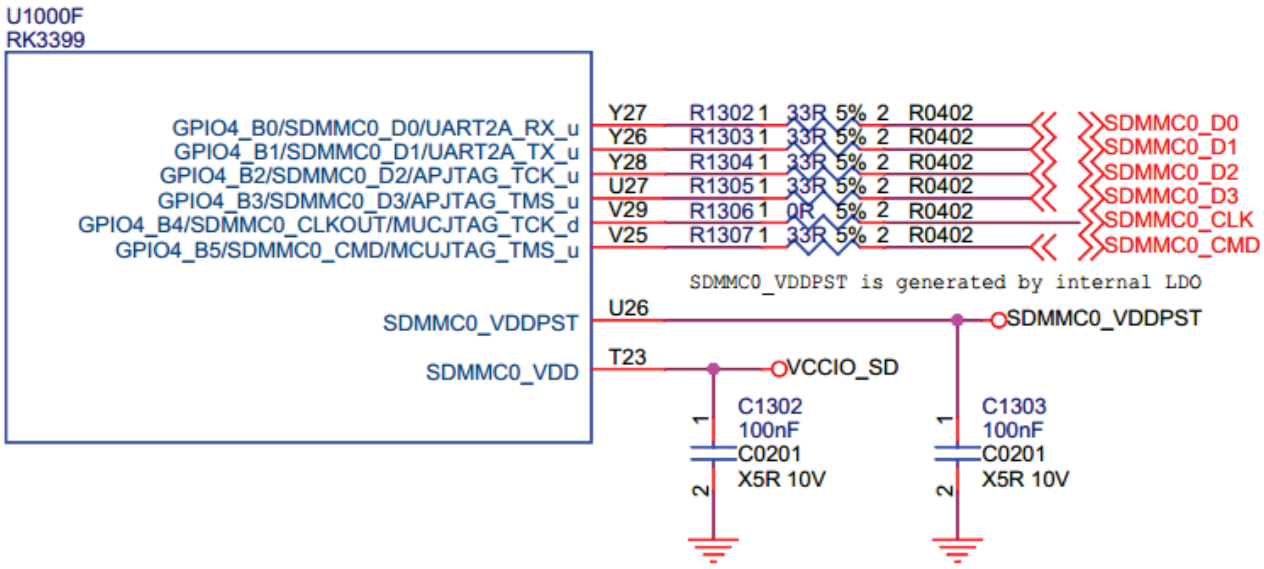


Figure 3-49 RK3399 SDMMC Interface

Table 3-9 shows the pull-up/pull-down and matching design of the SDMMC interface.

Table 3-9 RK3399 SDMMC Interface Design

Signals	Internal Pull-up/Pull-down	Series Resistance （SDR104 mode）	Description（SOC end）
SDMMC_DQ[3:0]	Pull-up	22ohm	SD data transmit / receive
SDMMC_CLK	Pull-down	NO	SD clock transmit
SDMMC_CMD	Pull-up	22ohm	SD command transmit / receive

In order to meet ESD requirements, the protective circuit is needed in SDMMC. In order to avoid the impact of protect parts on the SDMMC signal, and to achieve good protection, the PCB design should use the following principles:

- The protective part should be placed close to SDMMC port.
- The parasitic capacitance of protective part should less than 0.5pF.

3.3.2 Ethernet Port Circuit

RK3399 embedded a GMAC controller, support 10/100/1000M MAC PHY.The detail circuit please refer to the design documents released by MAC PHY vendors..

In 100M mode, the working clock used by phy can be provided by the MAC controller of rk3399, can omit one crystal at the phy side,shown as Figure3-50.

In gigab mode, the working clock used by phy needs to be supplied through an external crystal,shown as Figure 3-51.

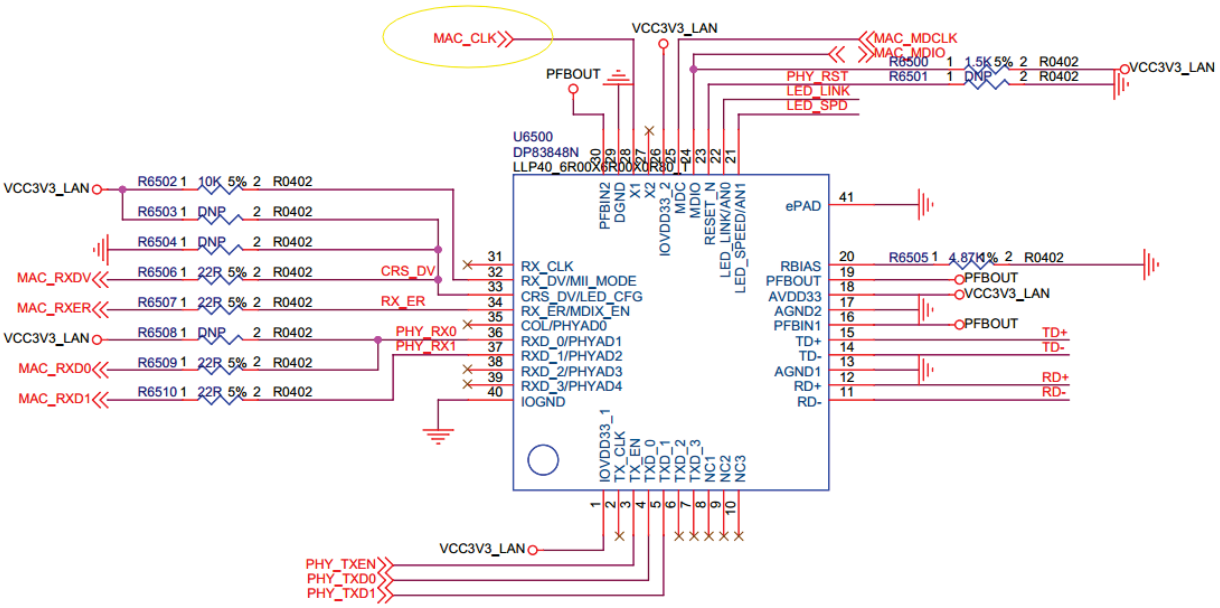


Figure 3-50 100M PHY Clock Source

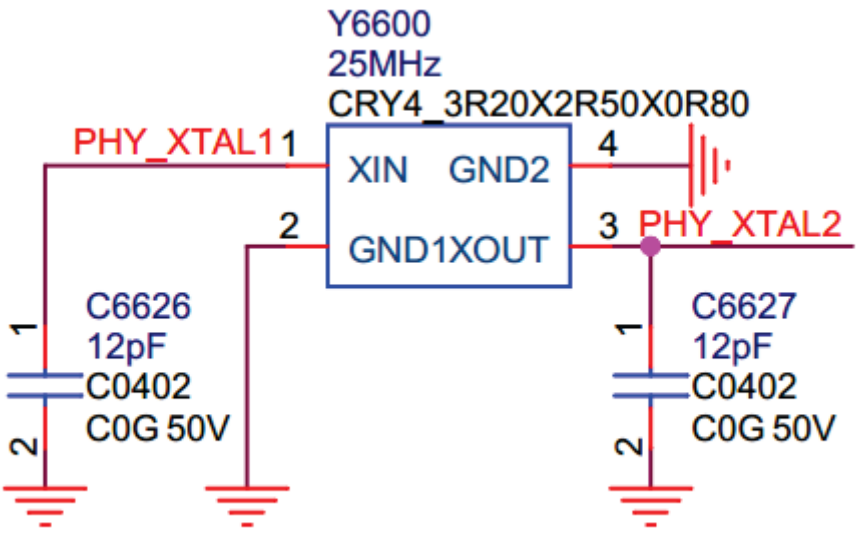


Figure 3-51 Gidab PHY Clock Source

RK3399 GMAC has two power supply,core power is 1.8V（Pin J22）,IO power is 3.3V（Pin J23）.The Ethernet PHY IO supply voltage needs to be consistent with the GMAC IO level.

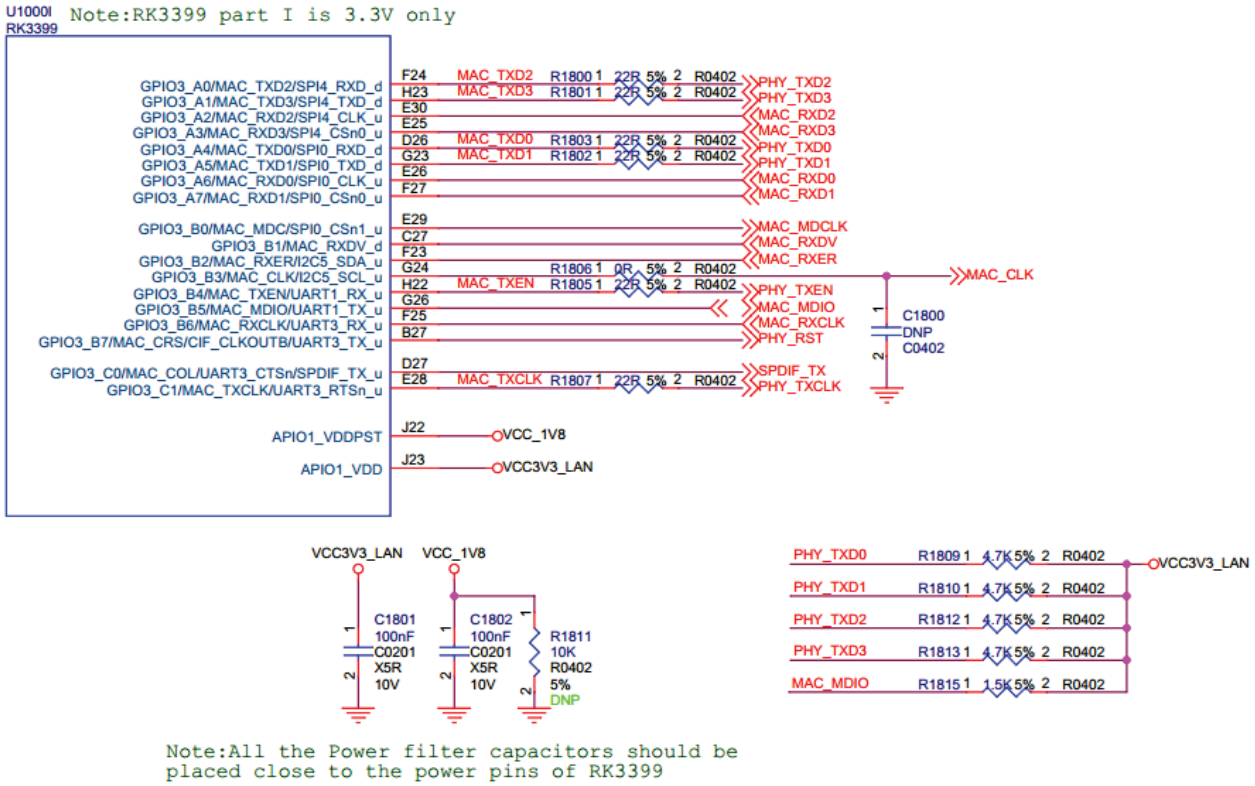


Figure 3-52 GMAC Power Supply

MAC can reset PHY via GPIO, and can also use the RC reset circuit to do it, it should be noted that the PHY power supply must be controllable.

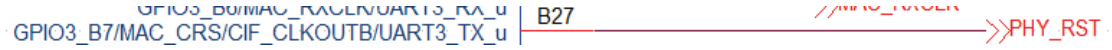


Figure 3-53 RK3399 RGMII Reset

The MDIO is the interface which transmits the control and status information between MAC and PHY, the MDC is clock signal and the MIDO is data signal, it should be noted that the MDIO signal needs to be pulled-up, shown as below.

Figure 3-54 RK3399 RGMII MDIO

- 3.3.2.1 1000M MAC

RK3399 RGMII interface design.

Table 3-10 RK3399 RGMII Interface Design

Signals	Internal Pull-up/Pull-down	Series Resistance	Description
MAC_TXCLK	Pull-up	22ohm	The reference clock for data transmit
MAC_RXCLK	Pull-up	NO	The reference clock for data receive
MAC_TXD[3:0]	Pull-up	22ohm	Data transmit
MAC_RXD[3:0]	Pull-up	NO	Data receive
MAC_TXEN	Pull-up	22ohm	Data transmit enable
MAC_RXDV	Pull-up	NO	Receive data valid indication
MAC_MDC	Pull-up	NO	Serial management interface clock
MAC_MDIO	Pull-up	NO	Serial Management Interface data input/output

MAC_CLK	Pull-up	22ohm	MAC main clock output

- The TX_CLK and RX_CLK frequency of RGMII is 125 MHz, in order to achieve the transmission rate of 1000 Mb, TXD and RXD are sampled in the bilateral edge of the clock. Data enable signal (MAC_TXEN, MAC_RXDV) must be valid before data is issued.

- 3.3.2.2 100M MAC

  RK3399 RMII interface design.

Table 3-11 RK3399 RMII Interface Design

Signals	Internal Pull-up/Pull-down	Series Resistance	Description
MAC_TXCLK	Pull-up	22ohm	The reference clock for data transmit
MAC_RXCLK	Pull-up	NO	The reference clock for data receive
MAC_TXD[1:0]	Pull-down	22ohm	Data transmit
MAC_RXD[1:0]	Pull-up	NO	Data receive
MAC_TXEN	Pull-up	22ohm	Data transmit enable
MAC_RXDV	Pull-down	NO	Receive data valid indication
MAC_MDC	Pull-up	NO	Serial management interface clock
MAC_MDIO	Pull-up	NO	Serial Management Interface data input/output
MAC_CLK	Pull-up	22ohm	MAC main clock output

- The MAC_CLK frequency is 50MHz; it is reference clock for RMII data transmission, samples the data once every clock cycle. Data enable signal (MAC_TXEN, MAC_RXDV) must be valid before data is issued.

- In RMII mode, it should be noted that the PHY_CRS_DV must be connected to MAC_RXDV, not MAC_CRS.

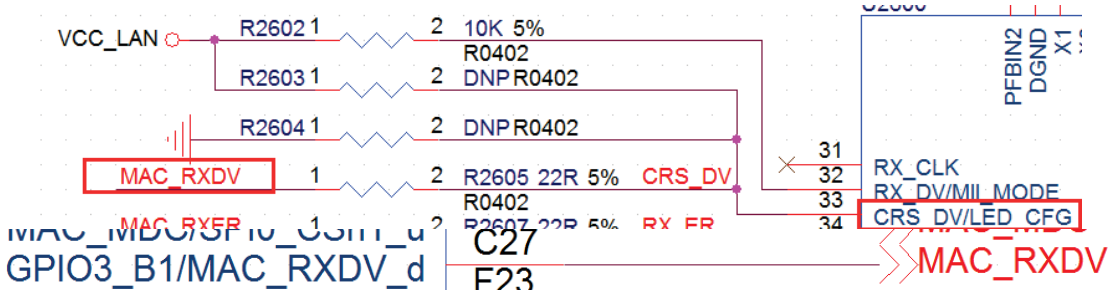


Figure 3-55 RK3399 RMII MAC_RXDV

- 3.3.2.3 ESD Protect

In order to meet the ESD, surge protection requirements, the protective circuit is needed, In order to avoid the impact of protective part on the MAC signal, and to achieve good protection, the PCB design should use the following principles.

- The protective part must be placed close to transformer.
- It is recommended to use TVS as protective part, breakdown voltage is 8KV, response time is less than 1ns.

3.3.3 USB Interface

RK3399 embedded two USB 2.0 controllers and two USB 3.0 controllers, USB 3.0 PHY 0 (or PHY 1) and USB 2.0 OTG 0 (or OTG 1) can compose a complete USB3.0 (or Type-C) interface.

Notes:

USB 2.0 controller and USB 3.0 controller used in conjunction need to follow the USB 2.0 PHY0 and USB 3.0 PHY0 to be matched, USB2.0 PHY1 and USB 3.0 PHY1 to be matched principle.

- 3.3.3.1 USB 2.0

USB2.0 PHY interface is shown as Figure 3-56.

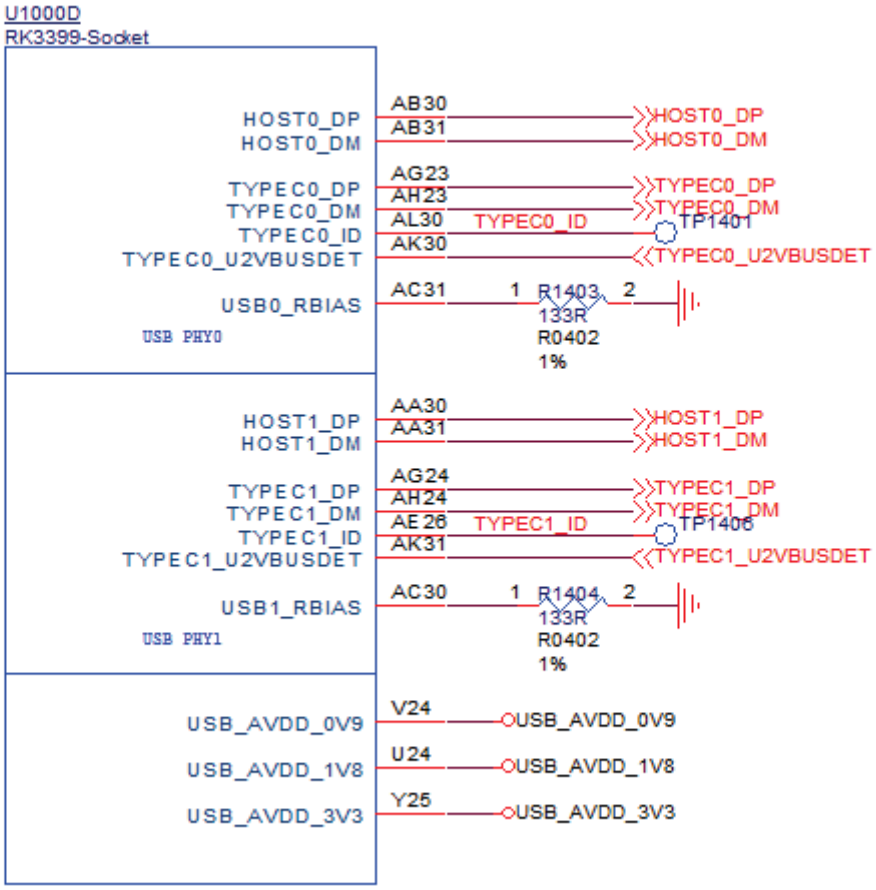


Figure 3-56 RK3399 USB 2.0 PHY

USB2.0 interface design is shown as Table 3-12.

Table 3-12 RK3399 USB2.0 Interface Design

Signals	Series Resistance	Description
HOST0_DP/DM	NO	USB2.0 HOST0 differential data lines
TYPEC0_DP/DM	NO	USB2.0 OTG0 differential data lines
TYPEC0_ID	NA	USB2.0 OTG0 ID detect，no use in Type-C
TYPEC0_U2VBUSDET	NA	USB2.0 OTG0 inserted detect
TYPEC0_RBIAS	NA	USB2.0 PHY0 reference resistor for HOST0 and OTG0, connect a 133R resistor to GND
HOST1_DP/DM	NO	USB2.0 HOST1 differential data lines
TYPEC1_DP/DM	NO	USB2.0 OTG1 differential data lines
TYPEC1_ID	NA	USB2.0 OTG1 ID detect，no use in Type-C

TYPEC1_U2VBUSDET	NA	USB2.0 OTG1 inserted detect
TYPEC1_RBIAS	NA	USB2.0 PHY1 reference resistor for HOST1 and OTG1, connect a 133R resistor to GND

Notes:

- OTG0 is fixed as firmware download interface,must be retained in design.
- USB2.0 OTG and USB2.0 HOST can be used at the same time.
- U2VBUSDET is used for USB inserted detect, high active.
- The reference resistor R1403 and R1404 must be within 1% accuracy, which is related to USB amplitude and eye diagram.
- In order to suppress the EMI, the common mode choke coil needs to be series connected in differential traces.

- 3.3.3.2 USB 3.0 Interface

  USB3.0 PHY interface

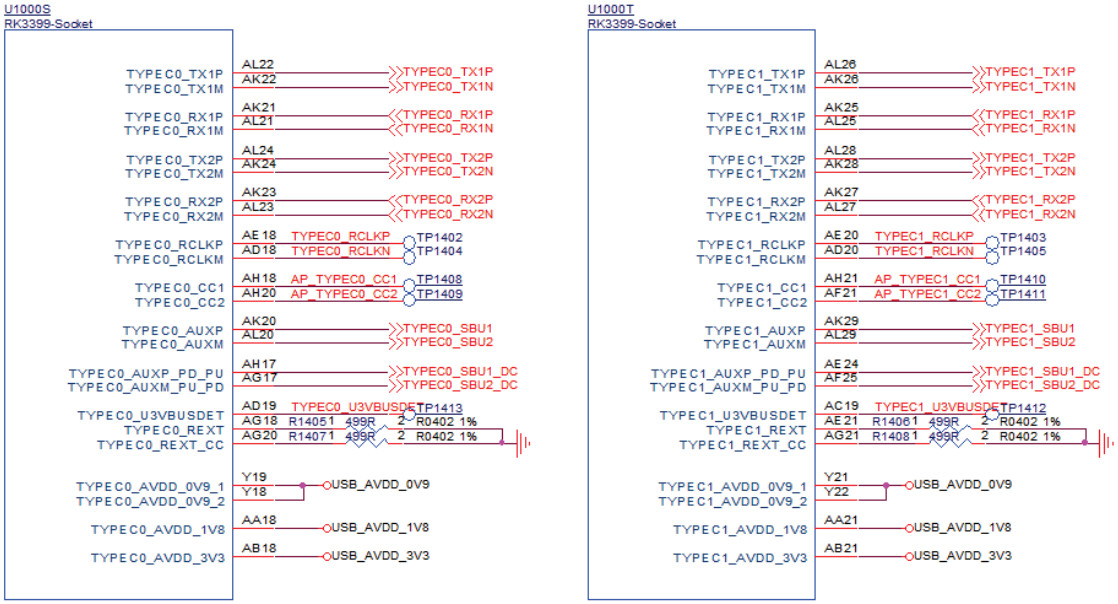


Figure 3-57 RK3399 USB 3.0 PHY

USB3.0 interface design is shown as Table 3-13, take PHY0 as an example.

Table 3-13 RK3399 USB3.0 Interface Design

Signals	Series Parts	Description
TYPEC0,1_TX1P/TX1M	100nF coulping capacitor	USB3.0 PHY SuperSpeed differential data transmit 1
TYPEC0,1_TX2P/TX2M	100nF coupling capacitor	USB3.0 PHY SuperSpeed differential data transmit 2
TYPEC0,1_RX1P/RX1M	NO	USB3.0 PHY SuperSpeed differential data receive 1
TYPEC0,1_RX2P/RX2M	NO	USB3.0 PHY SuperSpeed differential data receive 2
TYPEC0,1_RCLKP/RCLKM	NA	USB3.0 PHY external reference clock,no use
TYPEC0,1_CC1/CC2	NA	USB3.0 PHY CC internal signal ,no use
TYPEC0,1_AUXP/AUXM	100nF coupling capacitor	USB3.0 PHY auxiliary differential signal
TYPEC0,1_AUXP_PD_PU	NA	USB3.0 PHY auxiliary signal DC bias

TYPEC0,1_AUXM_PU_PD	NA	USB3.0 PHY auxiliary signal DC bias
TYPEC0,1_U3VBUSDET	NA	No use
TYPEC0,1_REXT	NA	USB3.0 PHY reference resistor, connect a 499R resistor to GND
TYPEC0,1_REXT_CC	NA	USB3.0 PHY internal CC reference resistor, connect a 499R resistor to GND,no use

Notes:

- Use external CC IC,do not use the embedded cc controller.
- USB 3.0 and USB 2.0 should to be collocation used, in order to achieve the USB protocol compatible.
- Use as USB 3.0 Type-A interface, fixed use TYPEC0_TX1P/TX1M and TYPEC0_RX1P/RX1M as SSTX and SSRX.
- The reference resistor R1405, R1406, R1407 and R1408 must be within 1% accuracy, which is related to USB amplitude and eye diagram.
- In order to suppress the EMI, the common mode choke coil needs to be series connected in differential traces.

- 3.3.3.3 USB Type-C

  USB Type-C interface reference design is shown as Figure 3-58.

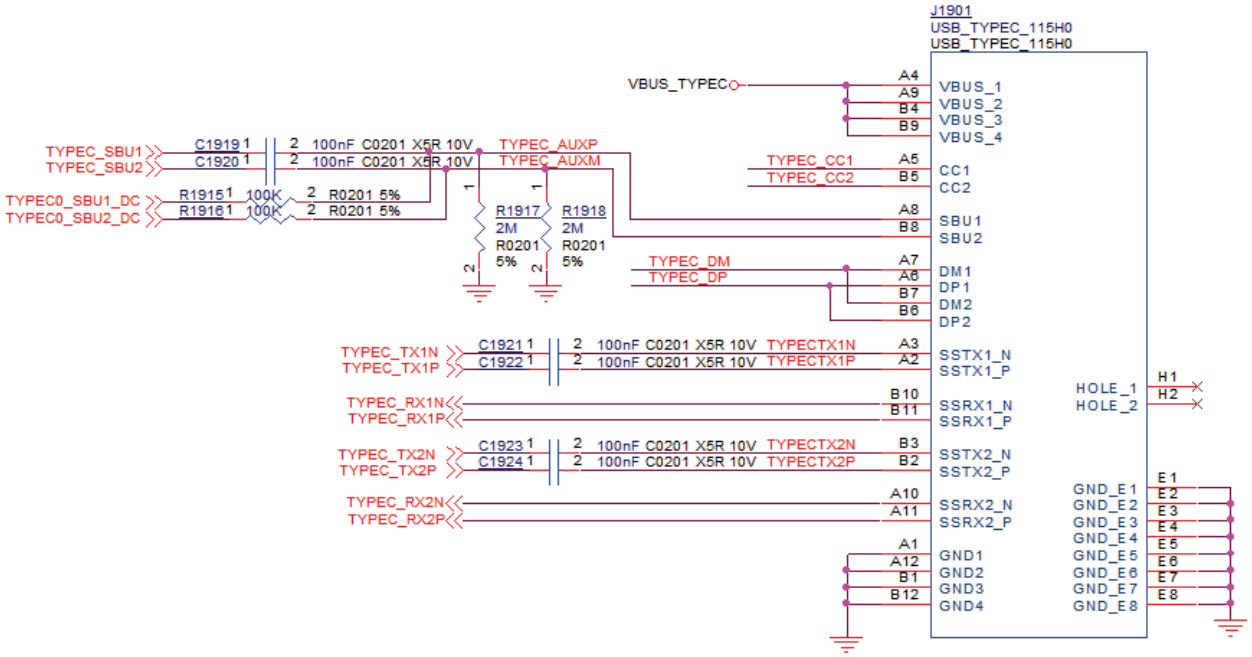


Figure 3-58 USB Type-C Interface

- The coupling capacitor of TX should be placed close to Type-C port, RX needs no coupling capacitor.
- If use PD function, it needs to add discharge circuit in power input port to prevent the device from damaged by over-voltage caused by replacing the device.shown as Figure 3-59.

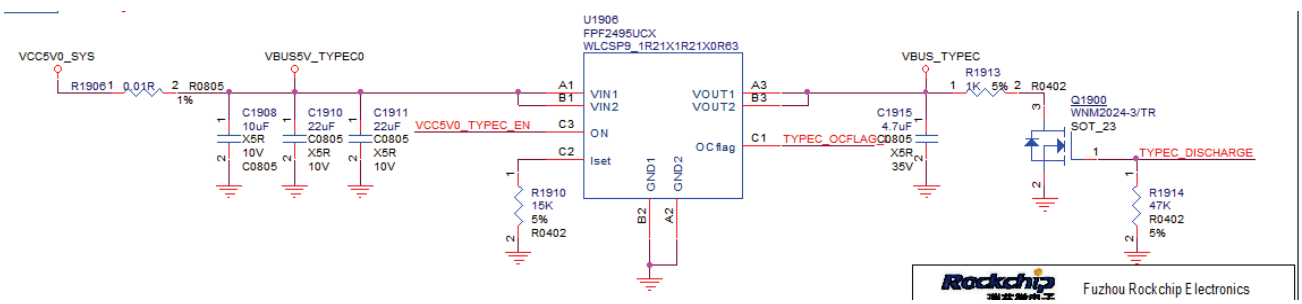


Figure 3-59 USB Type-C Interface Discharge Circuit

- 3.3.3.4 ESD Protect

In order to meet the ESD, the protective circuit must be needed, In order to avoid the impact of protective part on the USB signal, and to achieve good protection, the PCB design should use the following principles.

- The ESD part should be placed close to USB port.
- It is recommended to use TVS as protective part, air breakdown voltage is 15KV and contact breakdown voltage is 8KV, response time is less than 1ns.
- The protective part parasitic capacitance needs less than 1 pF in USB 2.0.
- The protective part parasitic capacitance needs less than 0.5 pF in USB 3.0.

3.3.4 DP Interface

RK3399 built-in DP（Display Port）controller(reused with USB3.0 interface)，it can be connected directly to the DP device,without the USB type-c protocol. The specific connection is divided into two cases: direct connect with DP device or DP conversion IC; or use USB Type-C cable connects.

In schematic design, make sure to follow the order in this section.

- 3.3.4.1 Device Direct Connect

In netbook product or industry application, it may be use DP port or DP conversion IC, in this case, only need to connect the Type-C interface to the DP port according to the order of the signal.

Table 3-14 RK3399 DP Interface Design

Signals	Series Parts	Description
TYPECn(n=0,1)_TX1P/TX1M	100Nf coulping capacitor	Correspond to DP_TX2P/TX2N
TYPECn(n=0,1)_TX2P/TX2M	100nF coulping capacitor	Correspond to DP_TX1P/TX1N
TYPECn(n=0,1)_RX1P/RX1M	100nF coulping capacitor	Correspond to DP_TX3P/TX3N
TYPECn(n=0,1)_RX2P/RX2M	100nF coulping capacitor	Correspond to DP_TX0P/TX0N
TYPECn(n=0,1)_AUXP/AUXM	100nF coulping capacitor,and provides DC bias	Correspond to DP_AUX

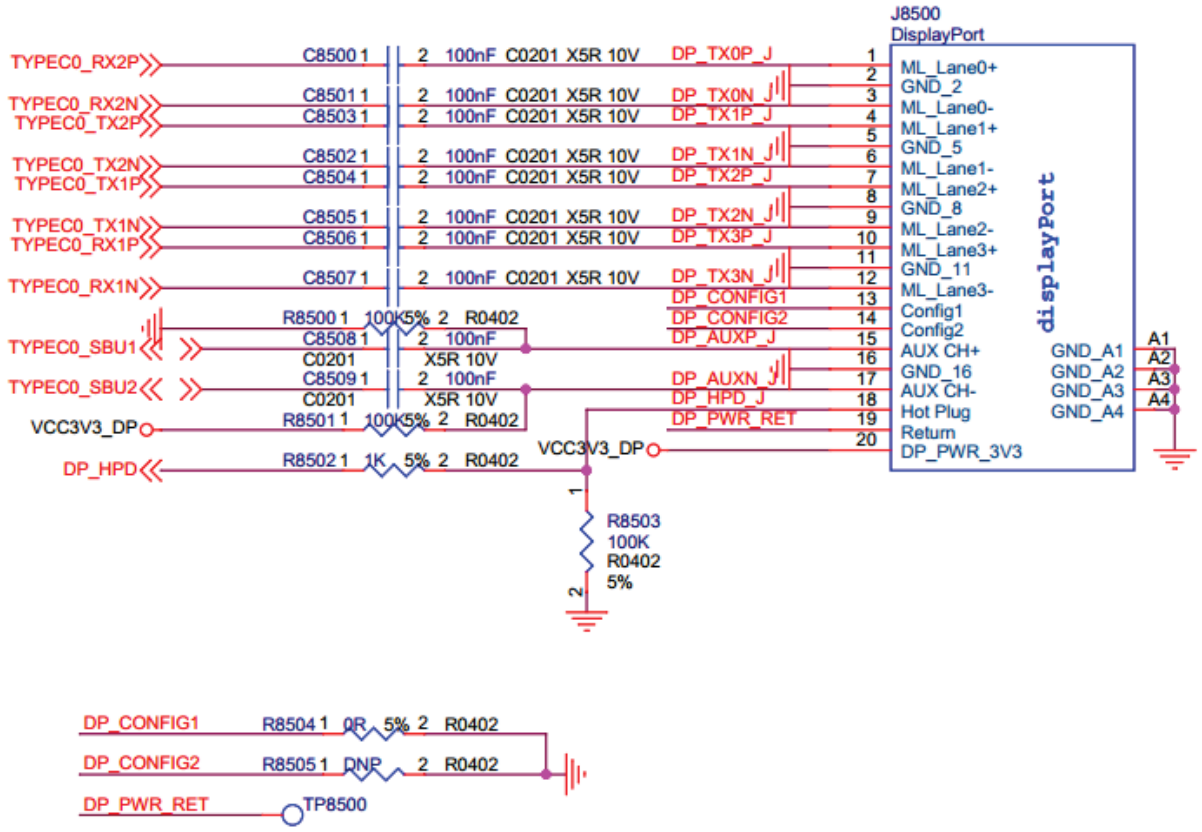


Figure 3-60 USB Type-C to DP Port circuit

- 3.3.4.2 Cable Connect

In the application of split VR, DP host will use Type-C cable to connect with the device. Since the TX and RX in the USB Type-C cable are cross-over, there is a need for cross-processing of the signals on the device.

Table 3-15 is the Type-C cable connection defined by the USB protocol.

Table 3-15 Full Function USB Type-C Cable

USB Type-C Plug #1		Wire		USB Type-C Plug #2	
Pin	Signal Name	Wire Number	Signal Name	Pin	Signal Name
A1,B1,A12,B12	GND	1[16]	GND_PWRrt1[GND_PWRrt2]	A1,B1,A12,B12	GND
A4,B4,A9,B9	Vbus	2[17]	PWR_Vbus1[PWR_Vbus2]	A4,B4,A9,B9	Vbus
A5	CC	3	CC	A5	CC
B5	Vconn	18	PWR_Vconn	B5	Vconn
A6	Dp1	4	UTP_Dp	A6	Dp1
A7	Dn1	5	UTP_Dn	A7	Dn1
A2	SSTXp1	6	SDPp1	B11	SSRXp1
A3	SSTXn1	7	SDPn1	B10	SSRXn1
B11	SSRXp1	8	SDPp2	A2	SSTXp1
B10	SSRXn1	9	SDPn2	A3	SSTXn1
B2	SSTXp2	10	SDPp3	A11	SSRXp2
B3	SSTXn2	11	SDPn3	A10	SSRXn2
A11	SSRXp2	12	SDPp4	B2	SSTXp2
A10	SSRXn2	13	SDPn4	B3	SSTXn2
A8	SBU1	14	SBU_A	B8	SBU2
B8	SBU2	15	SBU_B	A8	SBU1
Shell	Shield	Braid	Shield	Shell	Shield

In RK3399 SOC end connection is shown as Table 3-16.

Table 3-16 RK3399 DP Interface-SOC End

Signals	Series Parts	description
TYPECn(n=0,1)_TX1P/TX1M	100nFcoulping capacitor	Correspond to DP_TX2P/TX2M
TYPECn(n=0,1)_TX2P/TX2M	100nF coulping capacitor	Correspond to DP_TX1P/TX1M
TYPECn(n=0,1)_RX1P/RX1M	NO	Correspond to DP_TX3P/TX3M
TYPECn(n=0,1)_RX2P/RX2M	NO	Correspond to DP_TX0P/TX0M
TYPECn(n=0,1)_AUXP/AUXM	100nF coulping capacitor, and provides DC bias	Correspond to DP_AUX

In the VR end connection is shown as Table 3-17.

Table 3-17 RK3399 DP Interface-VR End

Signals	Series Parts	description
TYPEC_TX1P/TX1M	100nF coulping capacitor	Correspond to DP_TX3P/TX3M
TYPEC_TX2P/TX2M	100nF coulping capacitor	Correspond to DP_TX0P/TX0M
TYPEC_RX1P/RX1M	NO	Correspond to DP_TX2P/TX2M
TYPEC_RX2P/RX2M	NO	Correspond to DP_TX1P/TX1M
TYPEC_AUXP/AUXM	100nF coulping capacitor, and provides DC bias	Correspond to DP_AUX

For detail application, please refer to the document of “RK3399_VR&TABLET” and “RKNANOC_VR_REFBOARD_HDMI-DP_DUALMIP” released by Rockchip.

3.3.5 Audio Circuit

RK3399 embedded two groups of I2S controller, support master and slave. They all support the highest sampling rate up to 192 kHz, bit rate from 6 bits to 32 bits.

- 3.3.5.1 I2S0 Interface

Shown as Figure 3-54,I2S0 interface contains 1 SDI0,1 SDO0 and 3 SDIn/SDOn signals,it can be configured flexibly SDIn AND SDOn function,support up to 8 channels input / 2 channels output or 2 channels input / 8 channels output at the same time.Shown as Figure 3-61,Figure 3-62 and Figure 3-63.

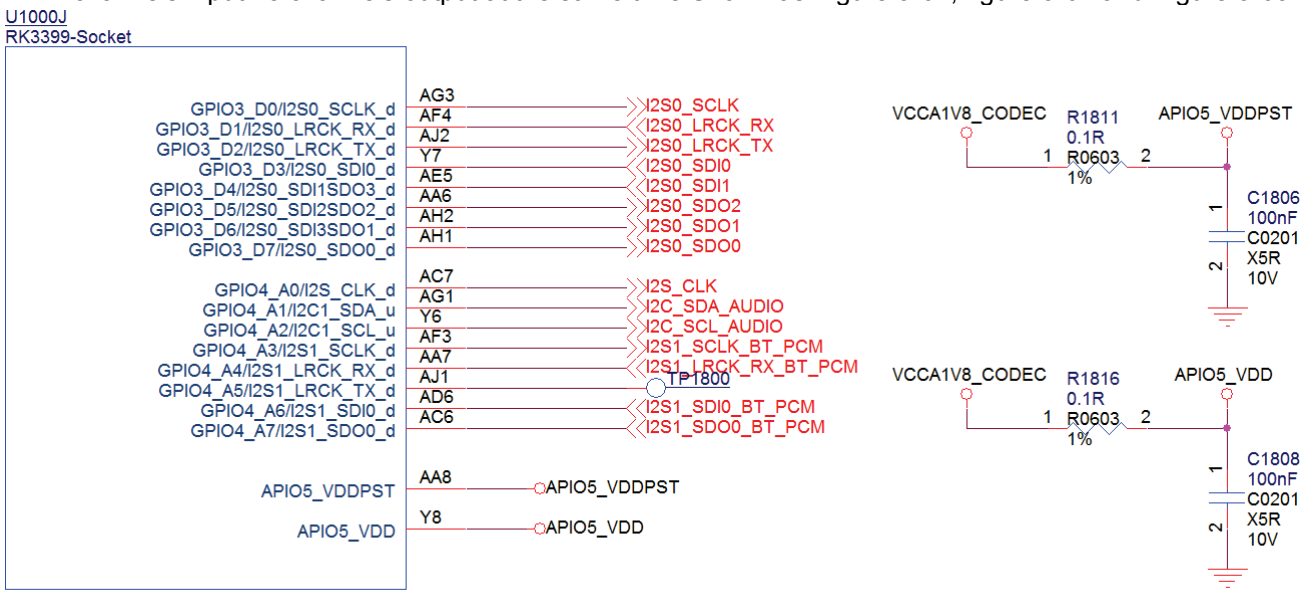


Figure 3-61 RK3399 I2S Interface

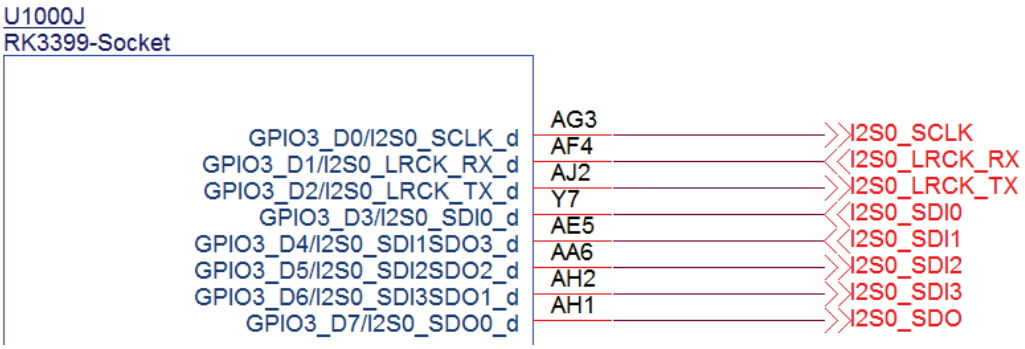


Figure 3-62 RK3399 I2S0 8 Channels input / 2 Channels Interface

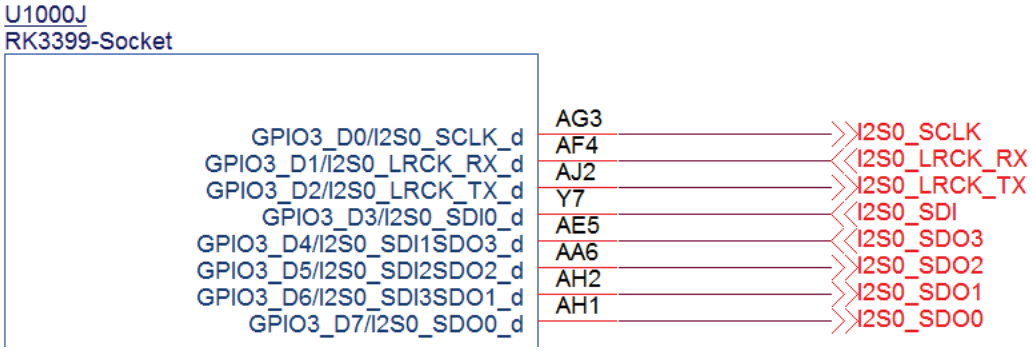


Figure 3-63 RK3399 I2S0 2 Channels input / 8 Channels Interface

I2S0 interface design is shown as Table 3-18

Table 3-18 RK3399 I2S0 Interface Design

Signals	Internal Pull-up/Pull-down	Series Parts	Description
I2S_CLK	Pull-down	22ohm	I2S main clock output
I2S0_SCLK	Pull-down	22ohm	I2S0 bit clock output
I2S0_LRCK_TX/RX	Pull-down	22ohm	I2S0 channel input/output select
I2S0_SDI0	Pull-down	22ohm	I2S0 data input 0
I2S0_SDI1SDO3	Pull-down	22ohm	I2S0 data input 1/output 3
I2S0_SDI2SDO2	Pull-down	22ohm	I2S0 data input 2/output 2
I2S0_SDI3SDO1	Pull-down	22ohm	I2S0 data input 3/output 1
I2S0_SDO0	Pull-down	22ohm	I2S0 data output 0

- 3.3.5.2 I2S1

  I2S1 support 2 channels input and 2 channels output, could be used as PCM.
  I2S1 interface design is shown as Table 3-19.

Table 3-19 RK3399 I2S1 Interface Design

Signals	Internal Pull-up/Pull-down	Series Parts	Description
I2S1_SCLK	Pull-down	22ohm	I2S1 bit clock output

PCM_CLK			Pcm CLK
I2S1_LRCK_TX/RX PCM_SYNC	Pull-down	22ohm	I2S1 channel input/output select PCM data frame synchronization
I2S1_SDI0 PCM_IN	Pull-down	22ohm	I2S1 data input 0 PCM data input
I2S1_SDO0 PCM_OUT	Pull-down	22ohm	I2S1 data output 0 PCM data output

- 3.3.5.3 Audio Codec

APIO5 is audio codec I2S interface power domain; it can support 1.8V and 3.0V, which is selected in the application according to the actual needs. Be noted that I2C signal level must meet with I2S interface level, otherwise, the audio codec would not work normally.

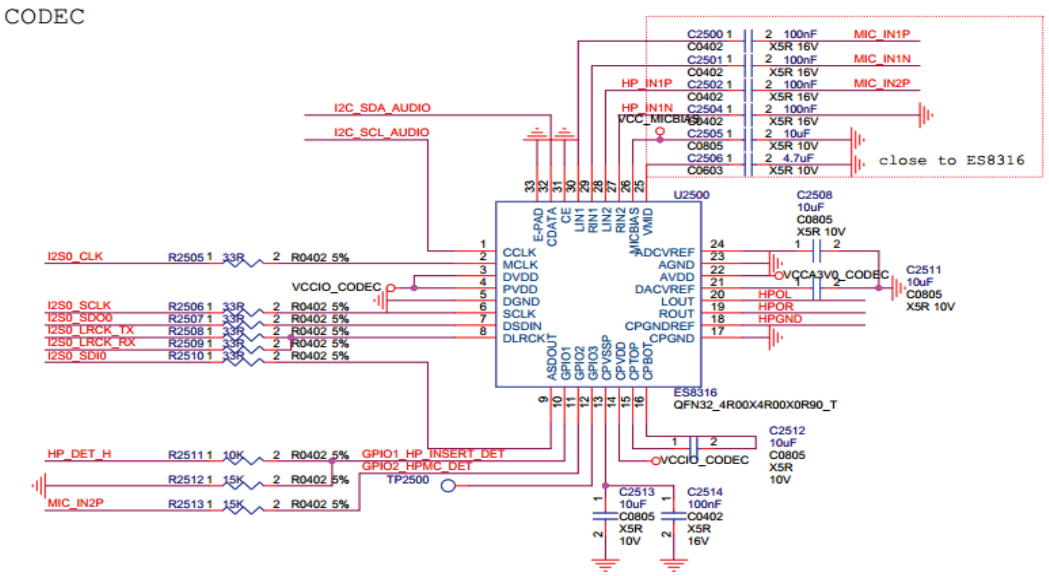


Figure 3-64 RK3399 Audio Codec

The HPGND output from the codec is used as an internal Offset reference and needs to be connected to GND, which is connected with GND at the headset to reduce the level difference with the headphone GND. If the Codec's GND is on the same complete GND plane as the headset GND, and the parts layout is close near, it can be connected directly to the GND plane.

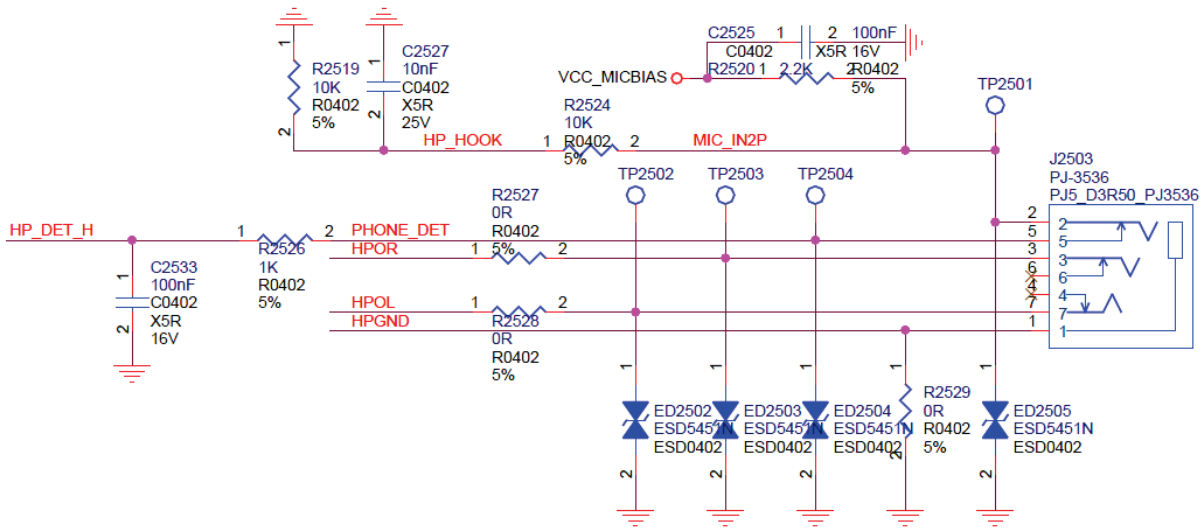


Figure 3-65 RK3399 Headset Circuit

- 3.3.5.4 MIC Input Circuit

MIC input circuit is shown as Figure 3-64.The value of R2500 and R2504 is selected according to the electret microphone specifications.

If use analog interface MEMS MIC, please refer to the recommended design.

If use digital interface MEMS MIC, it is connected directly to IS20 interface.Shown as Figure 3-65.

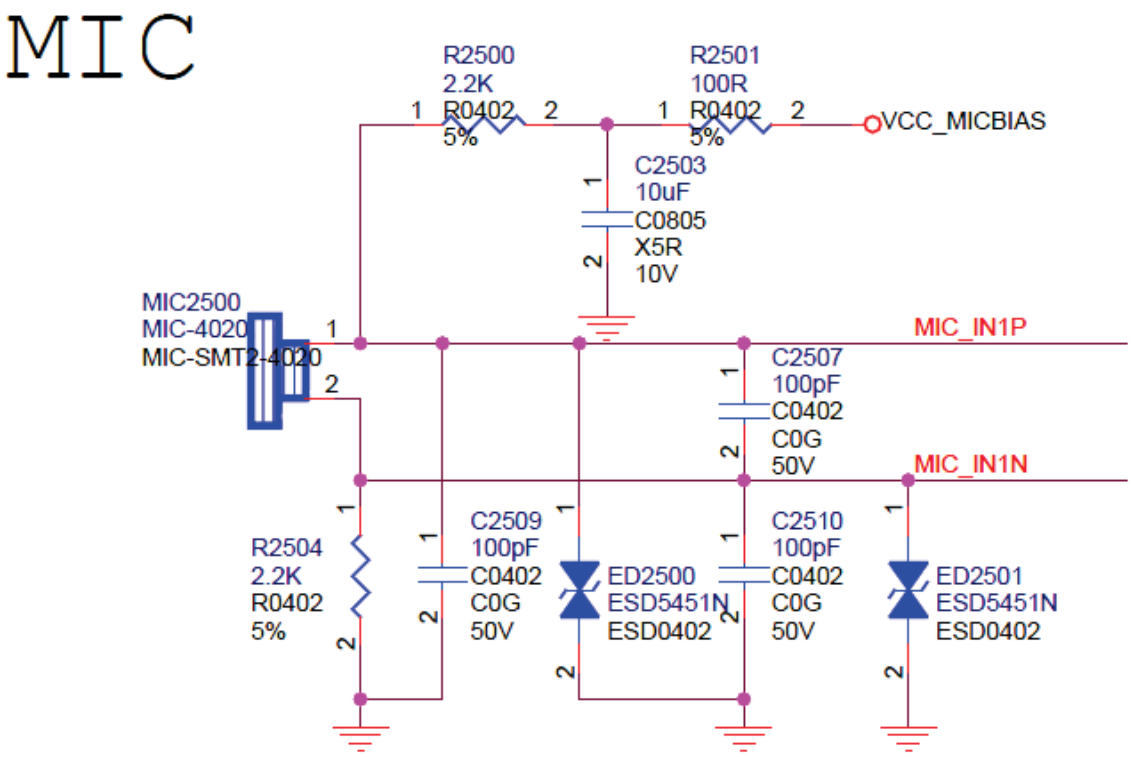


Figure 3-66 RK3399 MIC Input Circuit

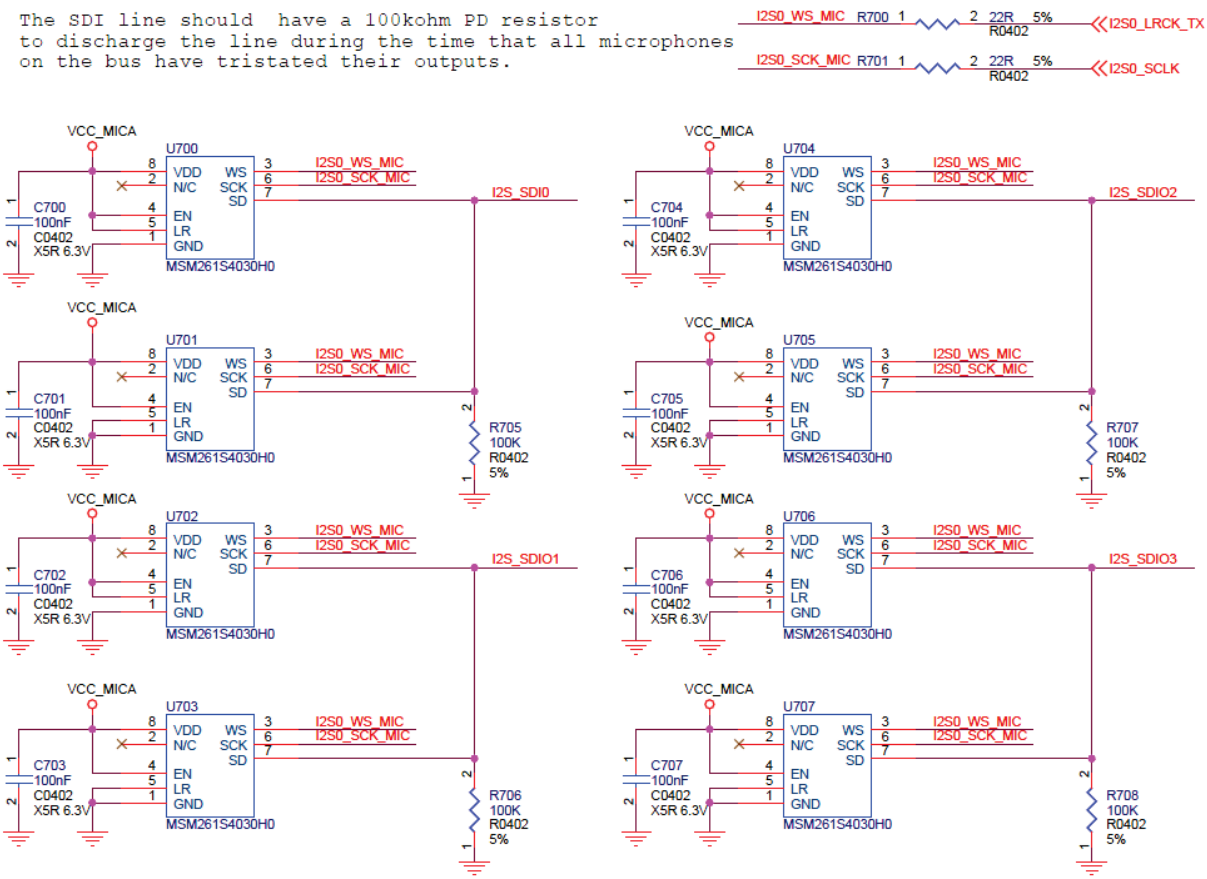


Figure 3-67 RK3399 Digital MIC Array Circuit

3.3.6 Video Interface

3.3.6.1 eDP

- The reference resistor of eDP controller must be within 1% accuracy, it is related to signal amplitude and eye diagram.
- The coupling capacitor of EDP_TXn should be placed close to SOC.

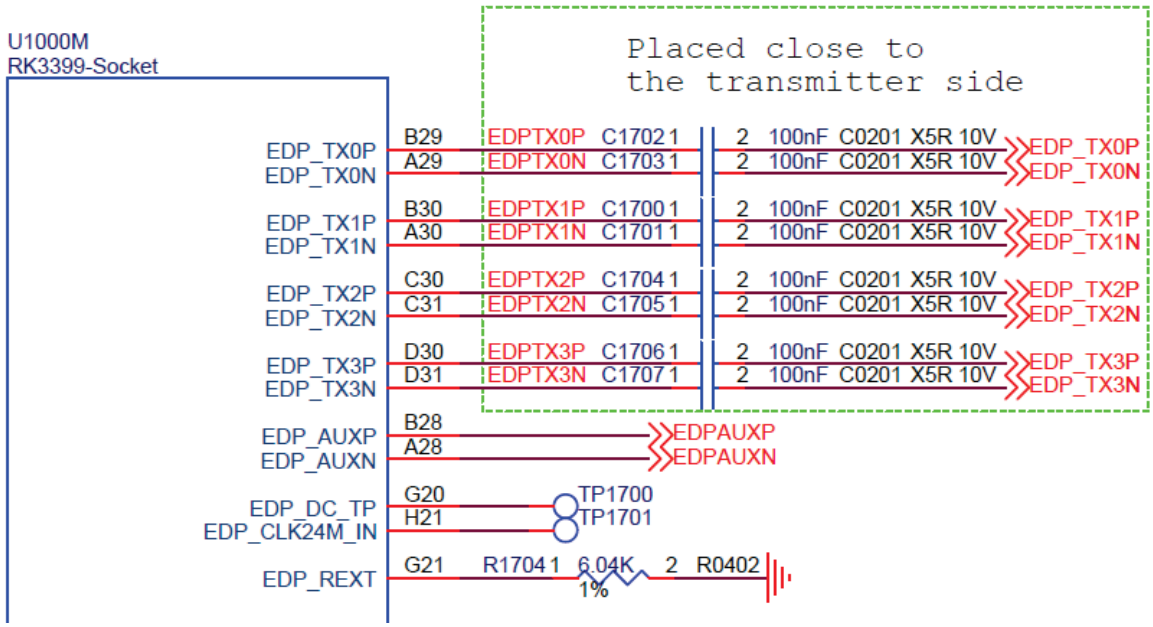


Figure 3-68 RK3399 eDP Interface

3.3.6.2 MIPI DSI

- The reference resistor of MIPI-DSI controller must be within 1% accuracy, it is related to signal amplitude and eye diagram.
- MIPI_TX_AVDD_1V8 and MIPI_TX/RX_AVDD_1V8 must use the same power supply.
- In single MIPI-DSI,it must be used MIPI-DSI0(MIPI_TX0).
- In dual MIPI-DSI, MIPI TX0 channel and MIPI TX1/RX1 channel exchanged can be according to layout.

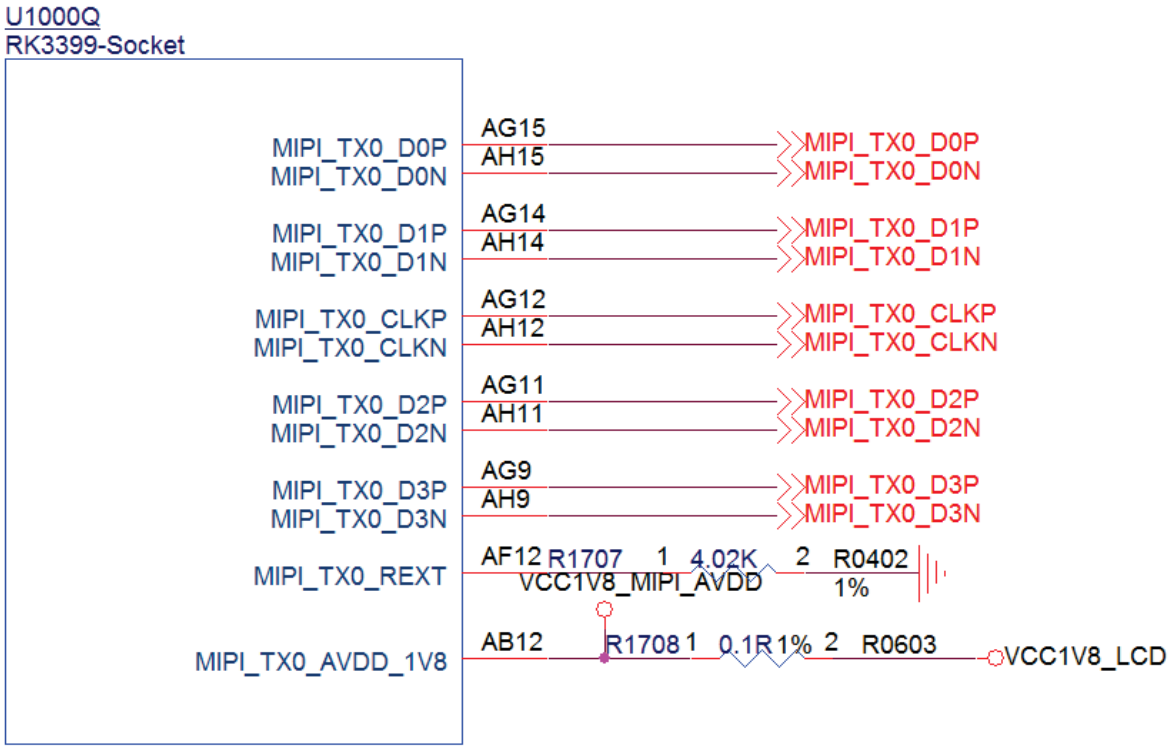


Figure 3-69 RK3399 MIPI DSI0 Interface

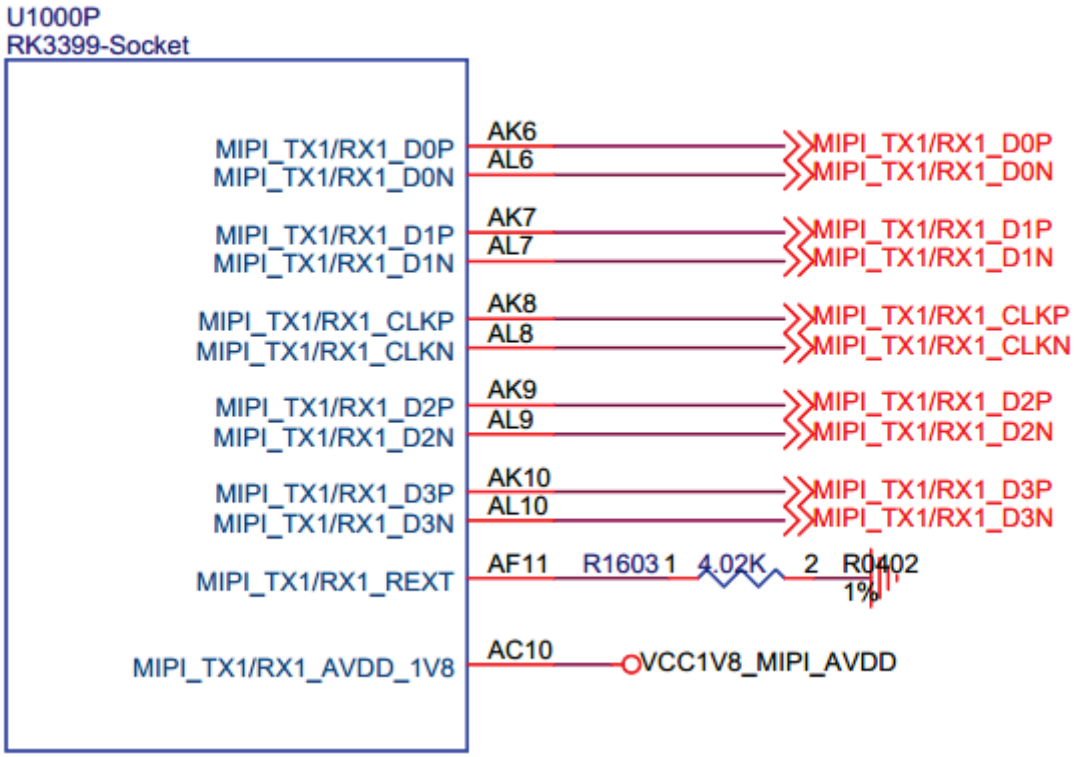


Figure 3-70 RK3399 MIPI DSI1 Interface

3.3.5.3 HDMI OUT

RK3399 built-in a HDMI controller, support HDMI 2.0.

- The reference resistor of HDMI controller must be within 1% accuracy, it is related to signal amplitude and eye diagram.

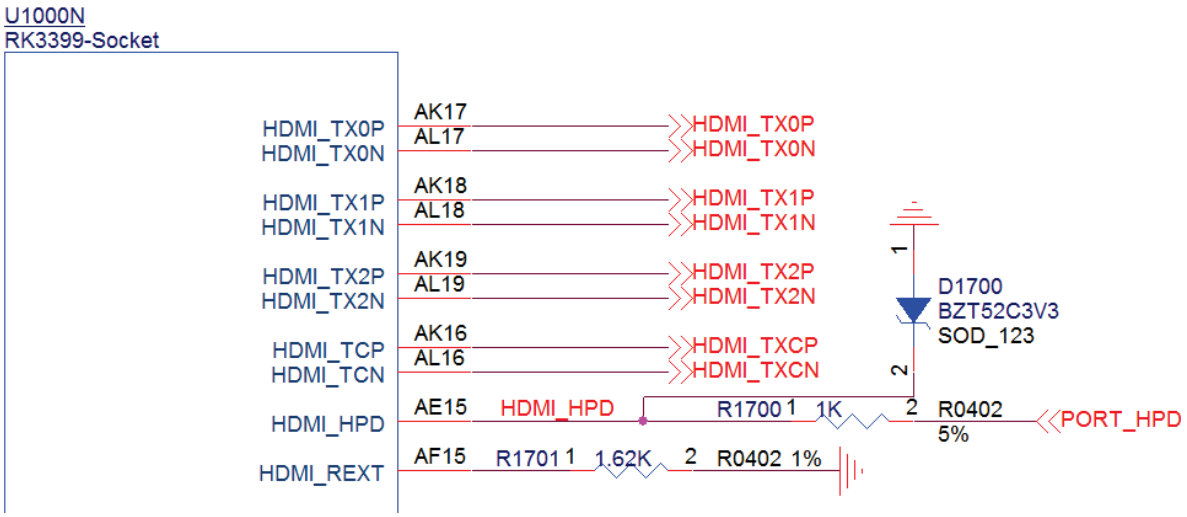


Figure 3-71 RK3399 HDMI Interface

- The HDMI CEC circuit should to prevent anti-irrigation design, the detail refer to RK3399 reference design.

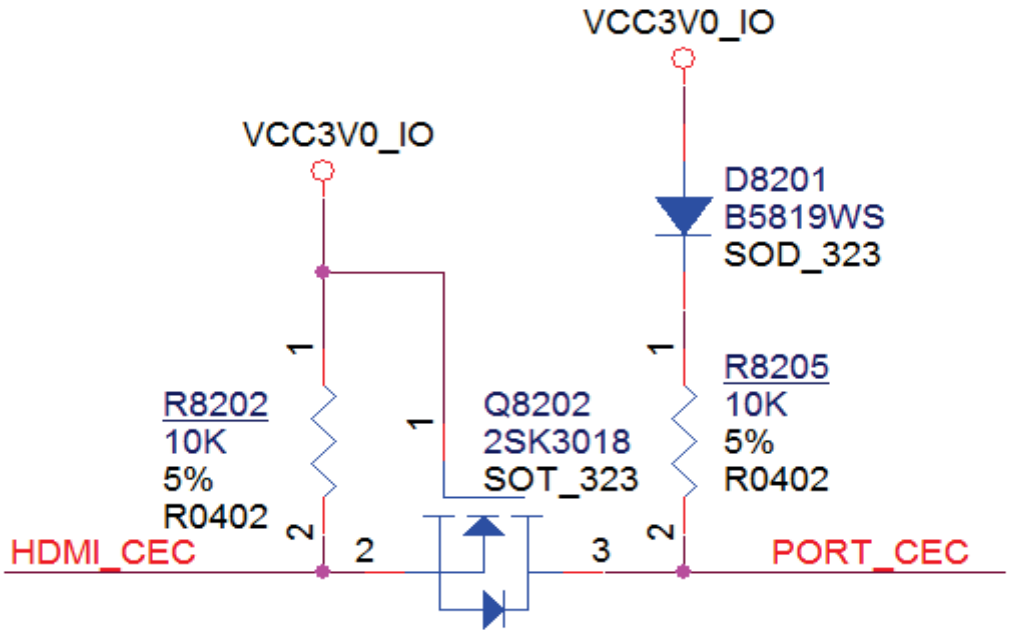


Figure 3-72 HDMI CEC Prevent Anti-irrigation Circuit

- HDMI DDC of RK3399 needs to add the level conversion circuit, because it could not support 5V level.

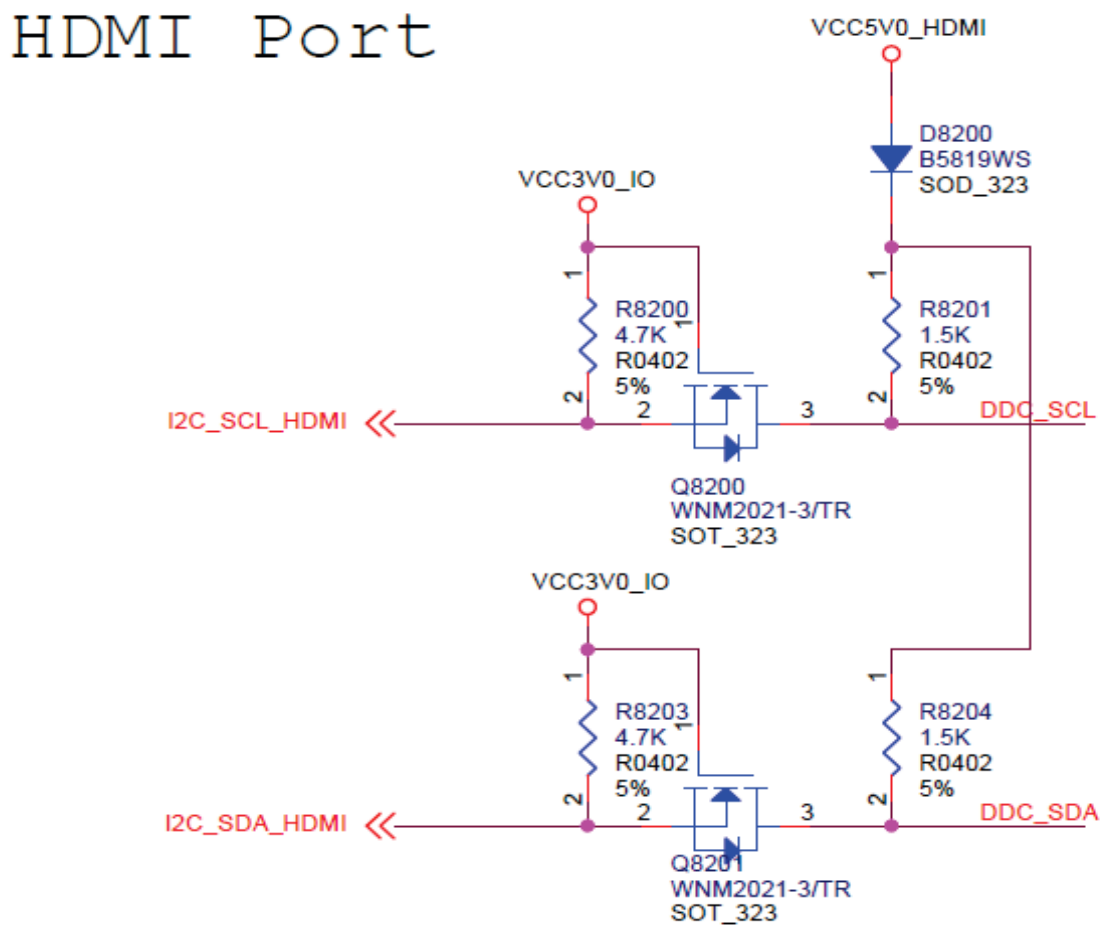


Figure 3-73 HDMI DDC Level Conversion Circuit

- The differential signals need to have ESD protection. The ESD parts should be placed close to HDMI port. The parasitic capacitance should be less than 0.5pF.

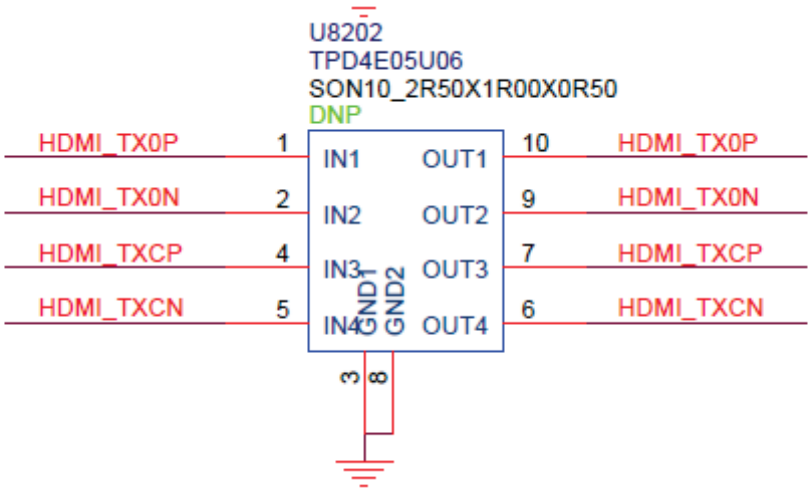


Figure 3-74 HDMI ESD Parts

3.3.7 Camera interface

- 3.3.7.1 USB Camera

  USB Camera please refers to Section 3.3.2.

- 3.3.7.2 MIPI CSI
- RK3399 built-in 2 channels MIPI-CSI with ISP processor, they can be use at the same time. The

reference resistor of MIPI-CSI controller must be within 1% accuracy, it is related to signal amplitude and eye diagram.

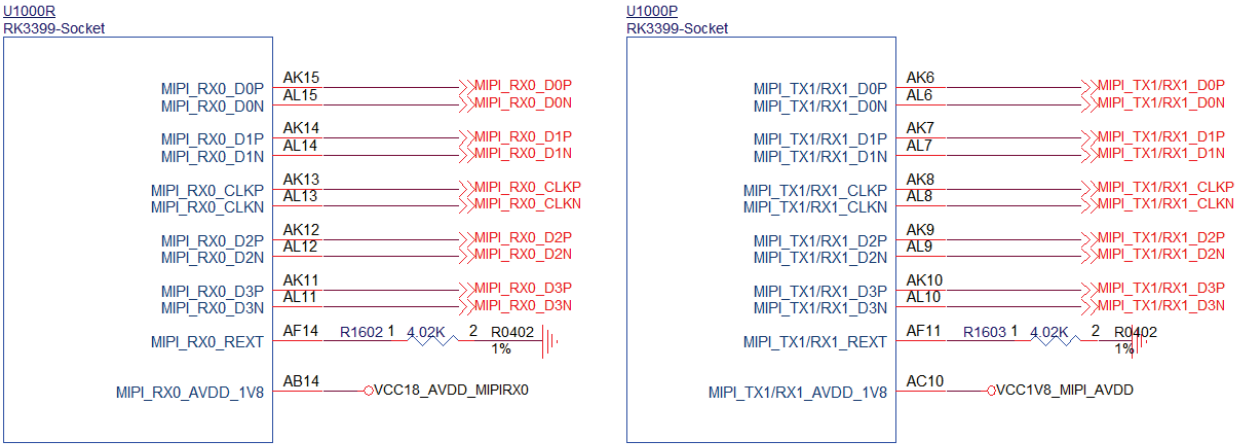


Figure 3-75 MIPI-CSI Interface

- 3.3.7.3 CIF CAMERA

APIO2_VDD is CIF interface power domain, it can support 1.8V and 2.8V, please select in the application according to the actual needs. Be noted that I2C signal level must meet with CIF interface level, otherwise, the camera would not work normally.

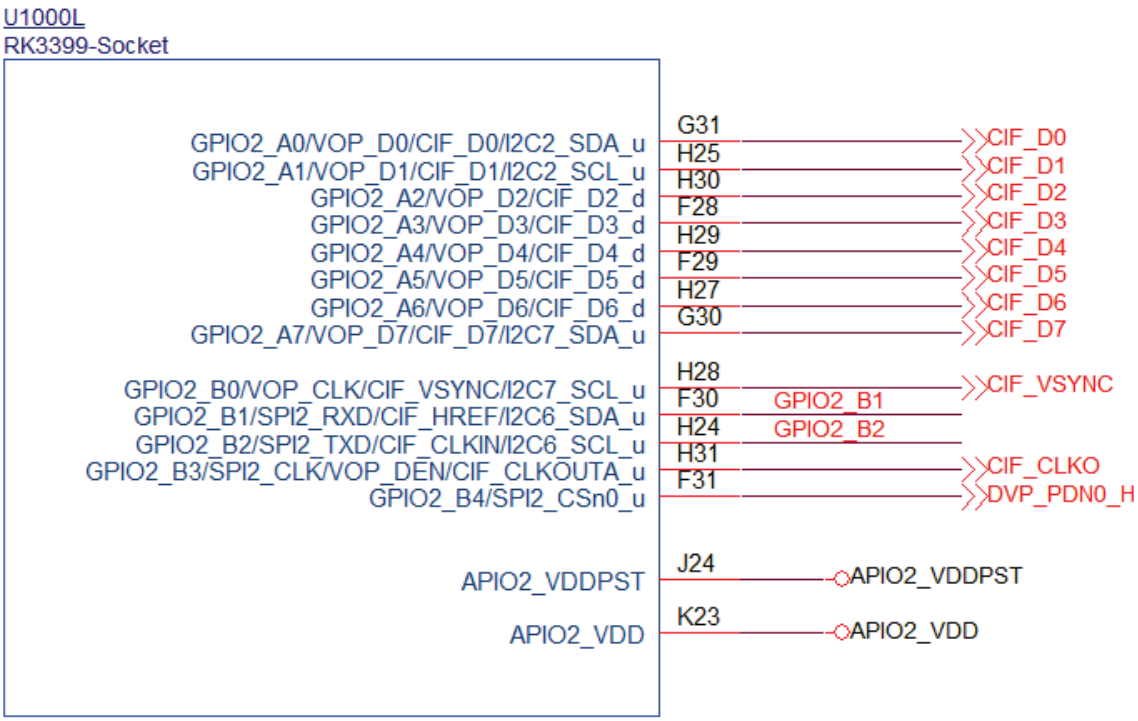


Figure 3-76 RK3399 CIF Interface

3.3.8 SARADC Interface

RK3399 embedded 5 channels SARADC input, Channel 1 is used for Keyboard detection, and reused as RECOVER function. Shown as Figure 3-69.When the key is pressed and the level of ADKEY_IN is lower than 100mV at system power-up, RK3399 will be enter firmware download mode.When PC recognizes the USB device, the key is released, then the firmware can be downloaded to SOC.

The SARADC is 10 bits accuracy and power supply is 1.8V.In keyboard design, to avoid power fluctuations

or disturbed to ensure accuracy, use the AD value as keys detection, rather than the voltage value, and the values between any two keys must be greater than 35 (AD sampling value) .The key values can be adjusted by divider resistor.

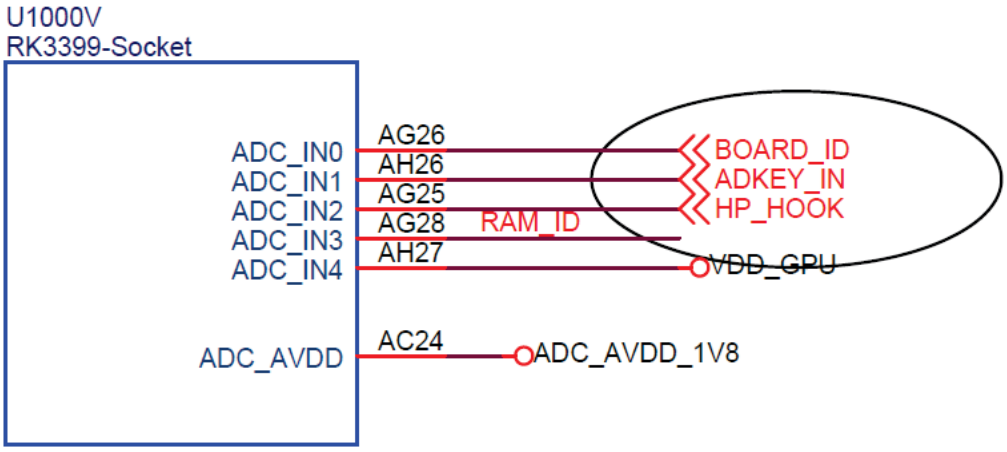


Figure 3-77 RK3399 SAR-ADC Interface

3.3.9 SDIO/UART Interface

RK3399 supports SDIO 3.0 interface WIFI module.It should be noted that the SDIO interface power domain is fixed 1.8V, so WIFI module IO power supply must be 1.8V.Shown as Figure 3-78.

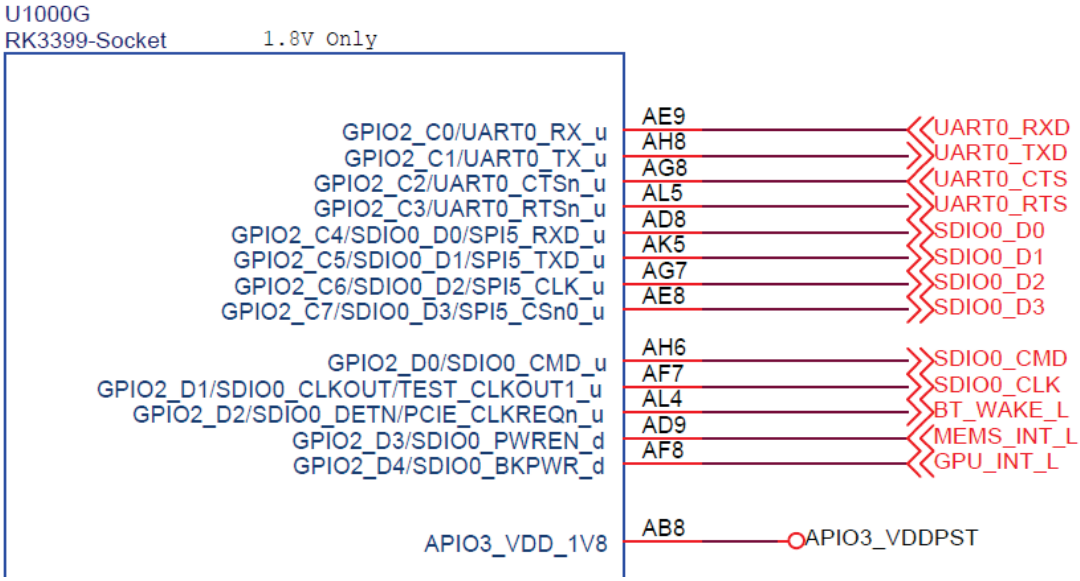


Figure 3-78 RK3399 SDIO/UART Interface

3.3.9.1 SDIO Interface Design

SDIO interface design is shown as Table 3-20.

Table 3-20 RK3399 SDIO Interface Design

Signals	Internal Pull-up/Pull-down	Series Parts	Description
SDIO_DQn[0:3]	Pull-up	22ohm	SDIO data transmit/receive
SDIO_CLKOUT	Pull-down	22ohm	SDIO clock output
SDIO_CMD	Pull-down	22ohm	SDIO command transmit/receive

3.3.9.2 UART

UART interface design is shown as Table 3-21.

Table 3-21 RK3399 UART Interface Design

Signals	Internal Pull-up/Pull-down	Series Parts	Description
UART0_RX	Pull-up	NO	UART0 data input
UART0_TX	Pull-up	NO	UART0 data output
UART0_CTSn	Pull-up	NO	UART0 allow to send
UART0_RTSn	Pull-up	NO	UART0 request to send

3.3.10 SPDIF Interface

SPDIF is an abbreviation for Sony/Philips Digital Interface Format, which is referred to SONY and PHILIPS digital audio interface. The SPDIF is divided into two kinds of coaxial and optical fiber, in fact, the transmitted signal is the same, but the carrier is different, the interface and connector appearance is also different. But the optical signal transmission does not consider the interface level and impedance problems, flexible interface and anti-interference ability.

RK3399 has a SPDIF output interface, support maximum 24bits interpretation. The maximum transmission rate of SPDIF connector limits the highest sampling rate of SPDIF. If the maximum transmission rate of SPDIF connector is 16Mbps, the sampling rate can only reach 96 KHz; if the sampling rate would need support 192 KHz, the fiber SPDIF connector would need to support 25Mbps.

The optical fiber SPDIF output circuit is shown as Figure 3-79, the signal traces need to be accompanied by ground traces.

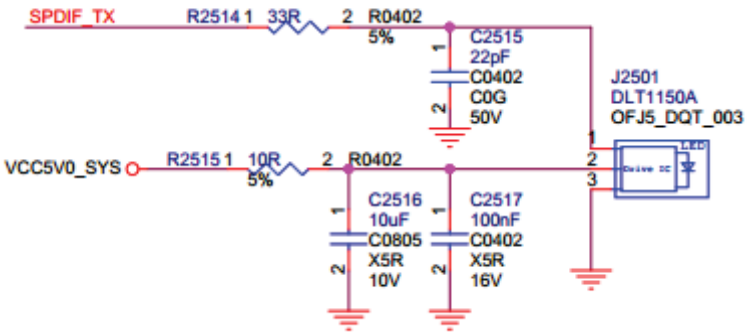


Figure 3-79 Optical Fiber SPDIF Interface

The coaxial SPDIF output circuit is shown as Figure 3-80.A coupling capacitor need to be series in signal traces, otherwise the CPU would be damaged when the level between devices do not match each other.

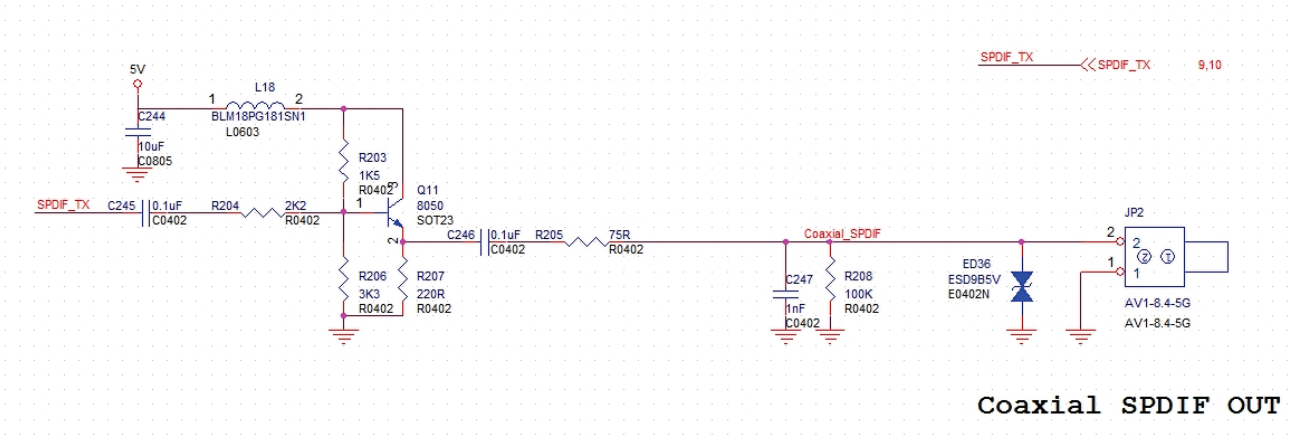


Figure 3-80 Coaxial SPDIF Interface

3.3.11 PCIe Interface

PCIe is an abbreviation for PCI-Express, It is the latest bus and interface standard.RK3399 support PCIe 2.1 protocol.It has following features:

- Support Root Complex（RC）and End Point（EP）
- Support 4x/2x/1x mode, respectively have 4 pairs of TX and RX differential lines
- Signal data channel data rate maximum up to 2.5GTb/s, with 8b/10b form, the maximum data rate up to 250MB/s
- Work in full-duplex mode, maximum data rate up to 10GTb/s, which is 1GB /s
- Support spread Spectrum Clock, SSC

The PCIE_AVDD_0V9 and the PCIE_AVDD_1V8 are RK3399 PCIe controller's power supply, PCIE_AVDD_0V9 should be powered on earlier than PCIE_AVDD_1V8

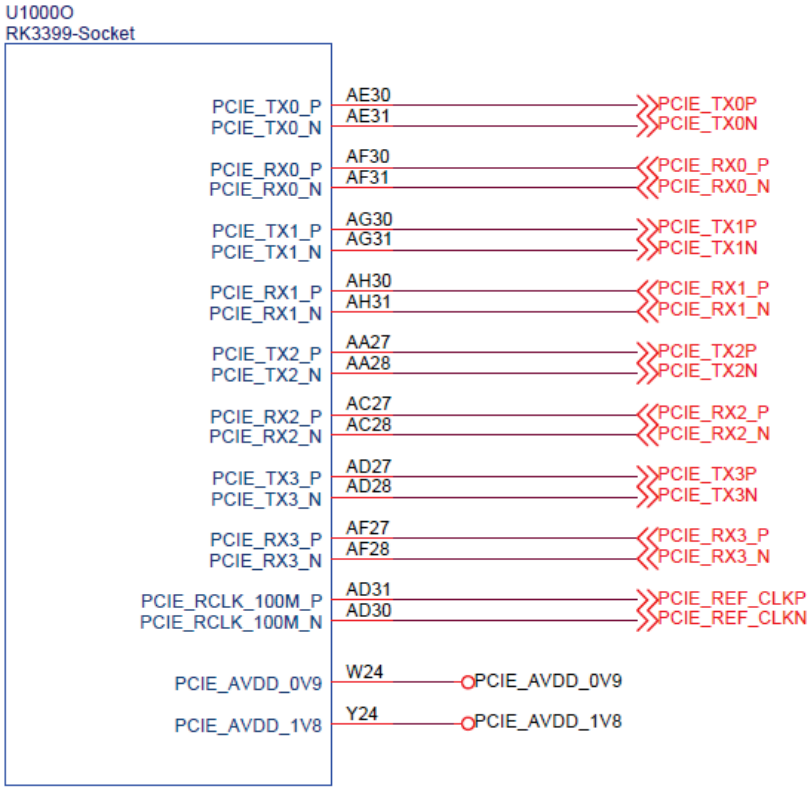


Figure 3-81 RK3399 PCIe Interface

- The coupling capacitor of TX signal should be placed close to PCIe connector.
- In the application, must pay attention to the PCIe device power consumption.If it is SSD storage, the power consumption are relatively high; and the power consumption of network card devices is

relatively low.

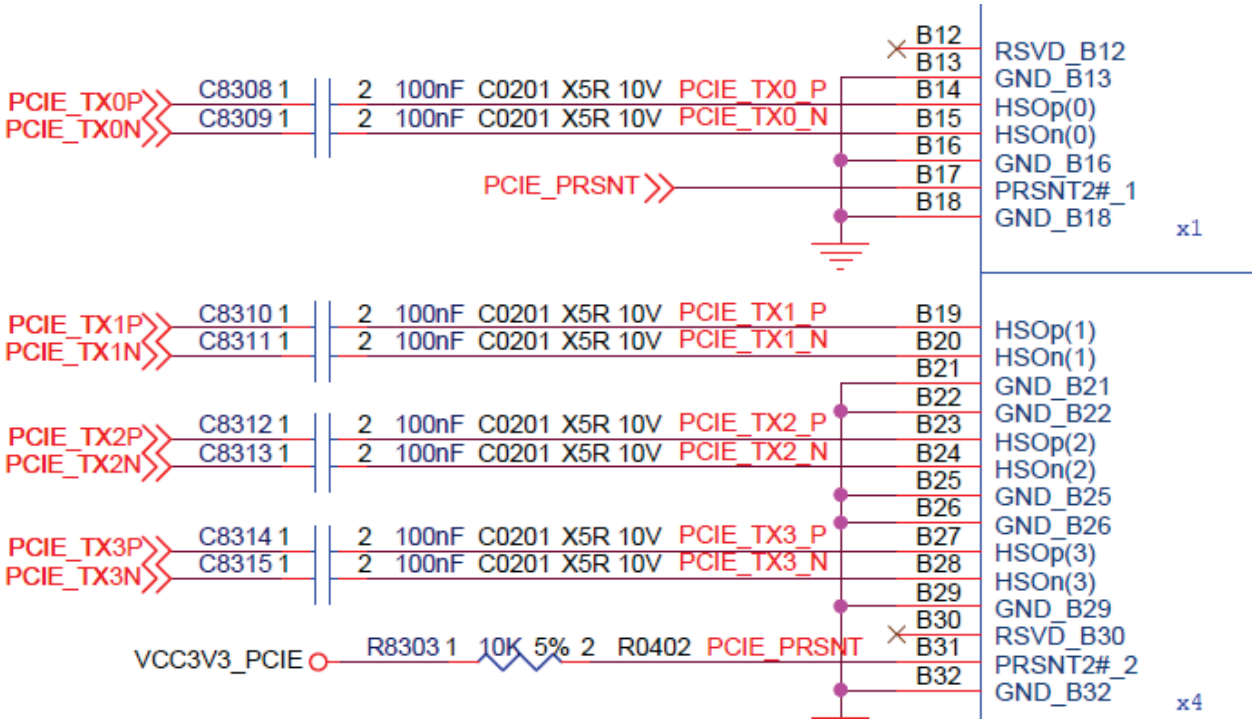


Figure 3-82 PCIe TX Coupling Capacitor

Chapter4 PCB Design

4.1 PCB Stack

In order to reduce the reflection in the high-speed signal transmission process, the signal source, the receiver and the transmission traces impedance must be matching. The specific impedance of a single-ended signal trace depends on its width and the relative position to the reference plane. The trace width and spacing between the differential pairs required for particular impedance depends on the selected PCB stack. Since the minimum width and minimum spacing are dependent on the PCB type and the cost requirements, the selected PCB stack must be able to achieve all the impedance requirements on the PCB, including the inner and surface layers, single-ended and differential traces and so on.

It is recommended to use more than 6 layers PCB in RK3399 design.The following PCB stack as an example, can give customers a help in the choice of PCB stack and assessment.If you choose other types of PCB stack, and recalculate the impedance according to the specifications provided by the PCB vendor.

4.1.1 8-Layer PCB Stack

In 8- layer PCB stack design, L2 is L1 reference plane, L7 is L8 reference plane.L5 and L7 are L6 reference plane, depending on the stack.

Layer No.	sig/pln	Copper thk. before process (oz)	Construction	Finished thikness (um)	Finished thikness (mil)	Tolerance	Dk (1GHz)
S/M				20	0.79	+/-10	3
1	TOP	1		30	1.18	+/-10	
			PP 1080X1(RC68%)	75	2.95	+/-10	3.8
2	GND	H		17	0.67	+/-10	
			Core	365	14.37	+/-10	4.2
3	POWER1	H		17	0.67	+/-10	
			PP 2116X1(RC68%)	115	4.53	+/-10	3.8
4	POWER2	H		17	0.67	+/-10	
			Core	265	10.43	+/-10	4.2
5	GND	H		17	0.67	+/-10	
			PP 2116X1(RC68%)	115	4.53	+/-10	3.8
6	SIGNAL	H		17	0.67	+/-10	
			Core	365	14.37	+/-10	4.2
7	GND	H		17	0.67	+/-10	
			PP 1080X1(RC68%)	75	2.95	+/-10	3.8
8	BOTTOM	1		30	1.18	+/-10	
S/M				20	0.79	+/-10	3

Figure 4-1 RK3399 8-Layer PCB Stack

4.1.2 6-Layer PCB Stack

In 6-layer PCB stack design, L2 is L1 reference plane, L5 is L6 reference plane.L3 and L5 are L4 reference plane, depending on the stack.

Customer Name:				Total Thickness:	1.0+/-0.10mm		
Customer P/N:				Measure from	SM~SM		
Layer No.	sig/pln	Copper thk. before process (oz)	Construction	Finished thikness (um)	Finished thikness (mil)	Tolerance	Dk (1GHz)
S/M				20	0.79	+/-10	3
1	TOP	1		30	1.18	+/-10	
			PP 1080X1(RC68%)	75	2.95	+/-10	3.8
2	GND	H		17	0.67	+/-10	
			PP 2116	115	4.53	+/-10	3.8
3	POWER	H		17	0.67	+/-10	
			Core	1065	41.93	+/-10	4.2
4	SIGNAL	H		17	0.67	+/-10	
			PP 2116	115	4.53	+/-10	3.8
5	GND	H		17	0.67	+/-10	
			PP 1080X1(RC68%)	75	2.95	+/-10	3.8
6	BOTTOM	1		30	1.18	+/-10	
S/M				20	0.79	+/-10	3

Figure 4-2 RK3399 6-Layer PCB Stack

4.2 High-speed signal PCB Design

4.2.1 Crystal Design

For the crystal circuit PCB design, please note:

- The crystal circuit layout should be placed as close as possible to the RK3399 clock pins
- Use 4 mils traces and are as short as possible to reduce load capacitance of traces and prevent unwanted noise
- Not any signal could be placed under the crystal circuit to avoid noise coupling into the crystal circuit
- On the same layer as crystal, should place the ground ring around it.The ground ring is connected to the adjacent ground layer by the via to isolate the noise
- The adjacent layer below the crystal circuit needs a complete ground reference plane, avoid being divided by any other signal traces, helping to isolate the noise and ensure crystal working stably

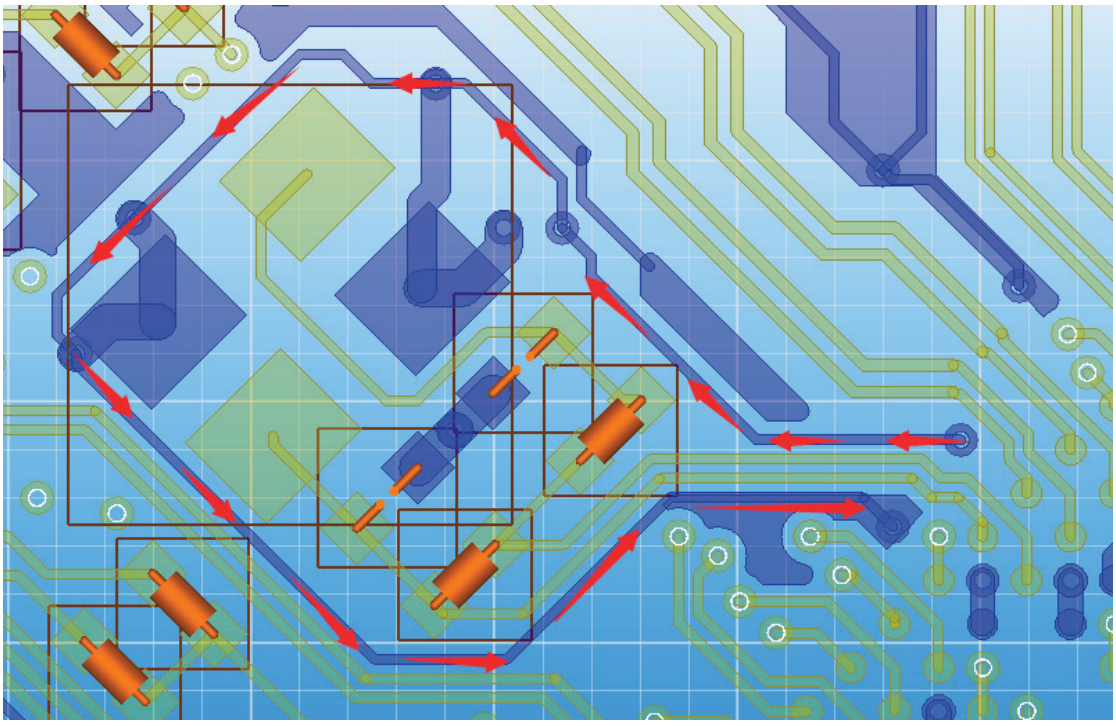


Figure 4-3 RK3399 Crystal Circuit Ground Ring

- Pin Y29 is analog ground of crystal oscillator, it should be isolated with other digital signal, and separately connected to the adjacent ground reference plane by the via.

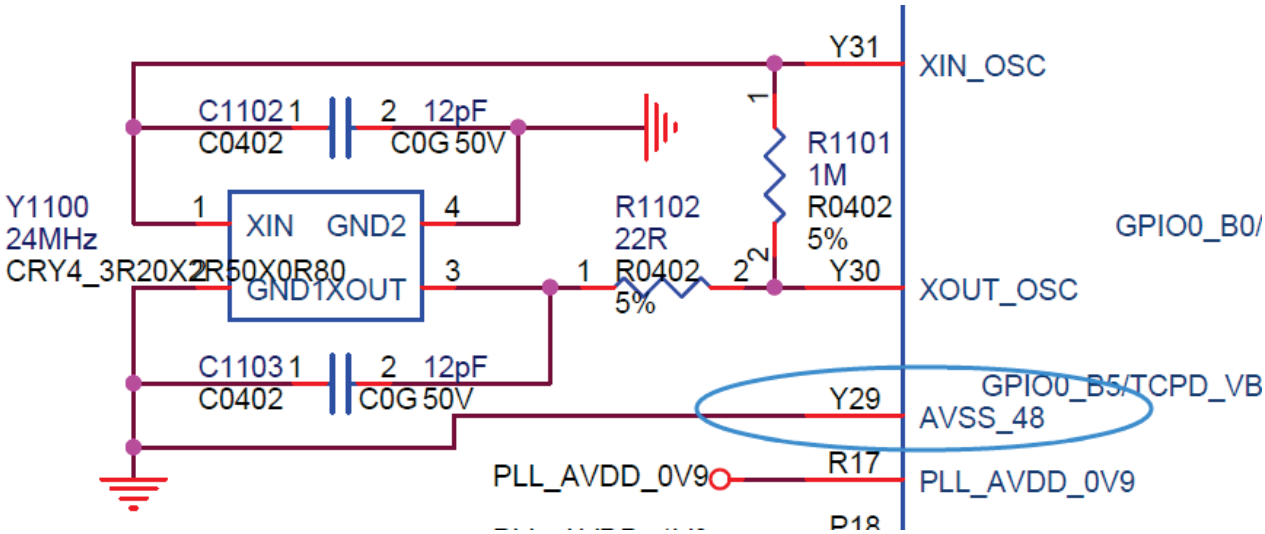


Figure 4-4 RK3399 Crystal Oscillator Analog Ground Pin

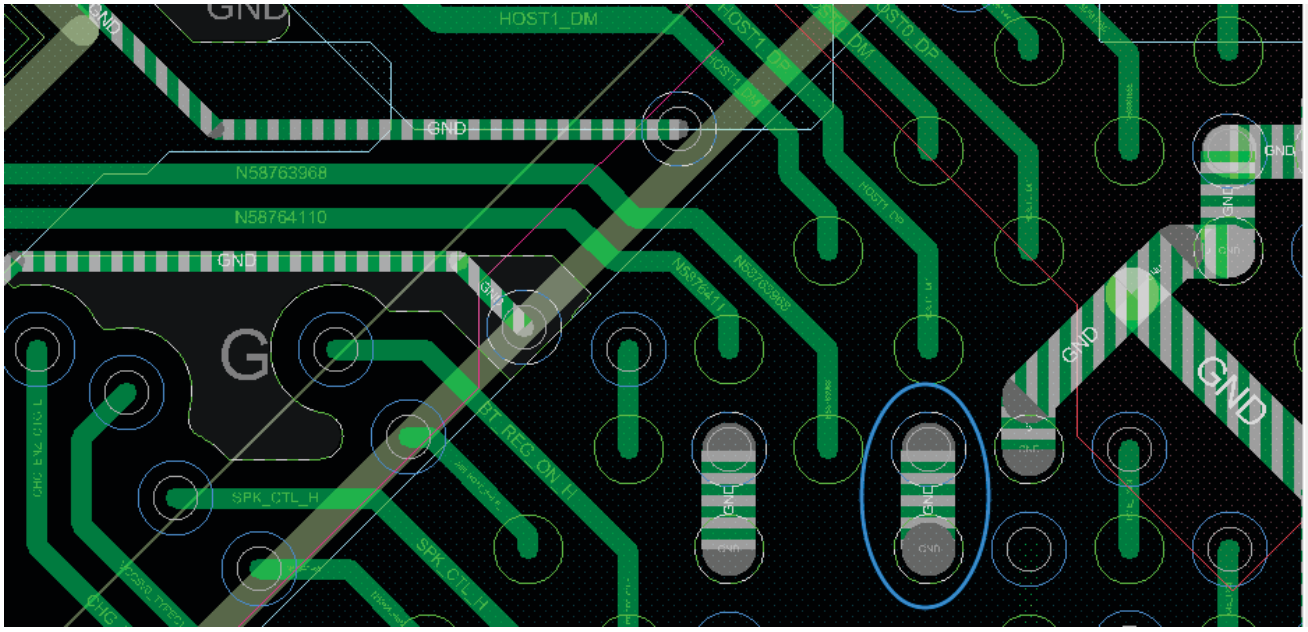


Figure 4-5 RK3399 Crystal Oscillator Analog Ground Layout

4.2.2 SDRAM Design

- The SDRAM with different column of 2 cs is not supported, neither is SDRAM with different column and the bank of 2cs.
- The 6Gb and 12Gb capacity SDRAM is special, it currently only support the same capacity on 2 CS of one channel, and the 8Gb, 4Gb, 2Gb capacity SDRAM do not have this limitation.
- If only use one channel of DDR, it can only use DDR0 channel.
- DDR_CLK trace could not be shorter than any DQ / DM / DQS traces of the same channel.
- CS2 is the copy signal of CS0, CS3 is the copy signal of CS1, and the behavior is exactly the same as the copied signal. So for DDR3, LPDDR3, in fact can only use 2 CS. And CS2, CS3 is only used for LPDDR4, because a channel of LPDDR4 devices is 16bit, when it needs the OSC up to 32bit, 2CS, it needs to use 4 CS signals.

- 4.2.2.1 LPDDR3

In LPDDR3 design, the D0-D16, D24 signals of DDR interface should be completely pin-to-pin connected to DRAM devices, otherwise the CA training and DQ calibration function would be not available.

All signals of LPDDR3, equivalent circuit is shown as Figure 4-6.

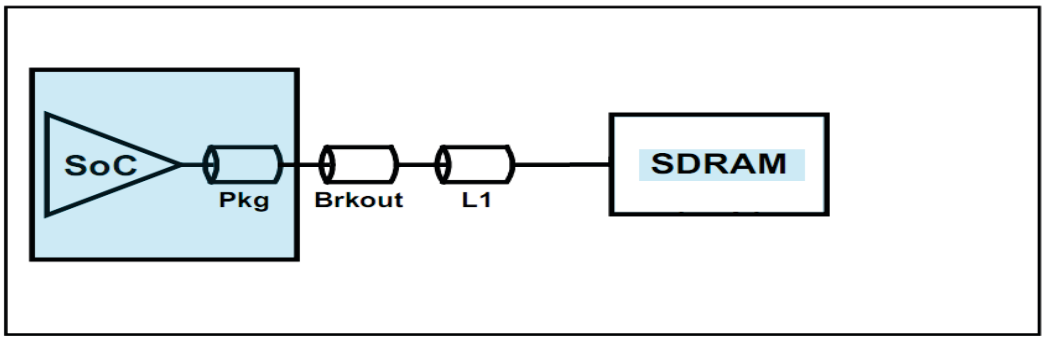


Figure 4-6 LPDDR3 Signals Equivalent Circuit

LPDDR3 data signals layout requirements are shown as Table-4-1.

Table 4-1 RK3399 LPDDR3 Data（DQ/DM/DQS）Layout Requirements

Items	Layout Requirements
Signal Group	DQ，DM，DQS
Target Impedance (Z0:DQ; Zdiff: DQS)	DQ: 50 Ohm ± 10%, DQS: 100 Ohm ± 10% , DM: 50 Ohm ± 10%
DQS Routing Trace Width and Spacing within pair	PCB stack-up dependent
DQ Routing Trace Width and Spacing within same Byte Group	Width : PCB stack-up dependent Spacing : ≥2 times the width of the trace
DQS to DQ Spacing within same Byte Group	≥2 times the width of the trace
Byte Group to Byte Group Spacing, Data to Other Signals Spacing	≥2 times the width of the trace
Max intra-pair skew of DQS	1ps
Max skew between DQ and DQS	5ps
Brkout	<100mil
Pkg+Brkout+L1	<1500mil
Pkg	Refer to package report
Maximum allowed via	2
Notes: DQ group A include：（DATA0—DATA7，DQM0，DQS0P/ DQS0M） DQ group B include：（DATA8—DATA15，DQM1，DQS1P/ DQS1M） DQ group C include：（DATA16—DATA23，DQM2，DQS2P/ DQS2M） DQ group D include：（DATA24—DATA31，DQM3，DQS3P/ DQS3M） The 5ps is the max skew inside DQ groups.It is not the requirement between DQ groups. Because max skew between CLK and DQS is 150ps, the max skew between DQ groups is 150ps too.	

LPDDR3 CLK signals layout requirements are shown as Table 4-2.

Table 4-2 RK3399 LPDDR3 CLK Layout Requirements

Items	Layout Requirements
Signal Group	CLK
Target Impedance (Diff Z0)	100 Ohm ± 10%
CLK Routing Trace Width and Spacing within pair	PCB stack-up dependent
CLK Routing Spacing to other Signals	≥3 times the width of the trace
Max intra-pair skew of CLK	1ps
Max skew between CLK and DQS	150ps
Brkout	<100mil
Pkg+Brkout+L1	<1700mil
Pkg	Refer to package report
Maximum allowed via	2

LPDDR3 control signals layout requirements are shown as Table 4-3.

Table 4-3 RK3399 LPDDR3 Control（CTL）Layout Requirements

Items	Layout Requirements
Signal Group	CSn，CKE
Target Impedance (Z0)	50 Ohm ± 10%
CTL Routing Trace Width and Spacing within same Byte Group	Width : PCB stack-up dependent Spacing : ≥3 times the width of the trace
Max skew between CTL and CLK	5ps
Brkout	<100mil
Pkg+Brkout+L1	<1700mil
Pkg	Refer to package report
Maximum allowed via	2

LPDDR3 command signals layout requirements are shown as Table 4-4.

Table 4-4 RK3399 LPDDR3 Command（CMD）Layout Requirements

Items	Layout Requirements
Signal Group	LPDDR3_A[0:9]
Target Impedance (Z0)	50 Ohm ± 10%
CA Routing Trace Width and Spacing	Width : PCB stack-up dependent Spacing : ≥3 times the width of the trace
Max skew between CMD and CLK	5ps
Brkout	<100mil
Pkg+Brkout+L1	<1700mil
Pkg	Refer to package report
Maximum allowed via	2

- 4.2.2.2 DDR3

In DDR3 design,the DQ lines in the same Group A or B or C or D(see Table 4-5) can be swapped. Also the group line can be swapped according to real need.

The data signal of DDR3 equivalent circuit is shown as Figure 4-7.

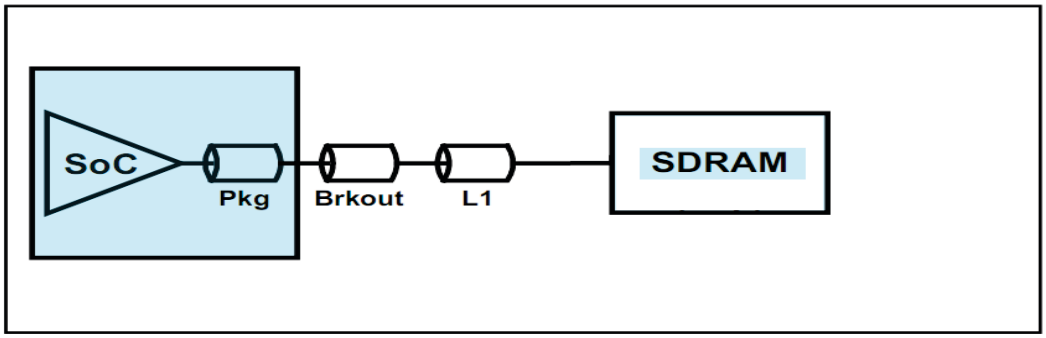


Figure 4-7 DDR3 DATA Equivalent Circuit

DDR3 Data signals layout requirements are shown as Table 4-5.

Table 4-5 RK3399 DDR3 Data（DQ/DM/DQS）Layout Requirements

Items	Layout Requirements
Signal Group	DQ，DM，DQS
Target Impedance (Z0:DQ; Zdiff: DQS)	DQ: 50 Ohm ± 10%, DQS: 100 Ohm ± 10% , DM: 50 Ohm ± 10%
DQS Routing Trace Width and Spacing within pair	PCB stack-up dependent
DQ Routing Trace Width and Spacing within same Byte Group	Width : PCB stack-up dependent Spacing : ≥2 times the width of the trace
DQS to DQ Spacing within same Byte Group	≥2 times the width of the trace
Byte Group to Byte Group Spacing, Data to Other Signals Spacing	≥2 times the width of the trace
Max intra-pair skew of DQS	1ps
Max skew between DQ and DQS	5ps
Brkout	<100mil
L1	<1500mil
L2a,L2b	<700mil,lenth match L2a and L2b within 1 ps
Pkg+Brkout+L1+L2	<2100mil, including package length
Pkg	Refer to package report
Maximum allowed via	4
Notes: DQ group A include：（DATA0—DATA7，DQM0，DQS0P/ DQS0M） DQ group B include：（DATA8—DATA15，DQM1，DQS1P/ DQS1M） DQ group C include：（DATA16—DATA23，DQM2，DQS2P/ DQS2M） DQ group D include：（DATA24—DATA31，DQM3，DQS3P/ DQS3M） The 5ps is the max skew inside DQ groups.It is not the requirement between DQ groups.Because max skew	

between CLK and DQS is 150ps, so the max skew between DQ groups is 150ps too.

DDR3 CLK equivalent circuit is shown as Figure 4-8.

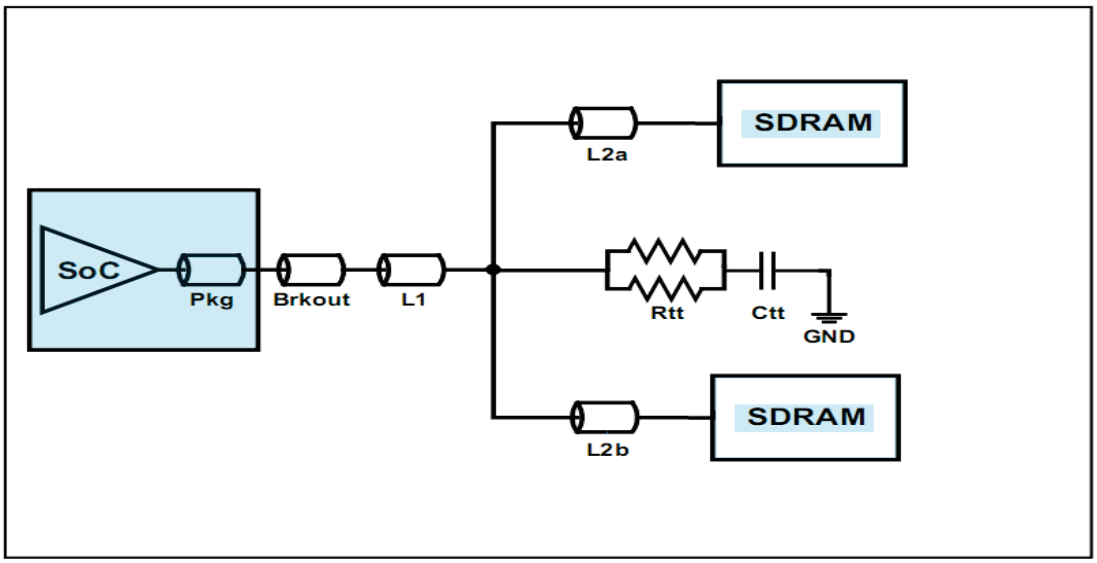


Figure 4-8 DDR3 CLK Equivalent Circuit

DDR3 CLK signals layout requirements are shown as Table 4-6.

Table 4-6 RK3399 DDR3 CLK Layout Requirements

Items	Layout Requirements
Signal Group	CLK
Target Impedance (Diff Z0)	100 Ohm ± 10%
CLK Routing Trace Width and Spacing within pair	PCB stack-up dependent
CLK Routing Spacing to other Signals	≥2 times the width of the trace
Max intra-pair skew of CLK	1ps
Max skew between CLK and DQS	150ps
Brkout	<100mil
L1	<1500mil
L2a, L2b	<700mil .length match L2a and L2b within 1 ps
Pkg+Brkout+L1+L2	<2100mil,including package length
Pkg	Refer to package report
Maximum allowed via	4

DDR3 Control signals equivalent circuit is shown as Figure 4-9.

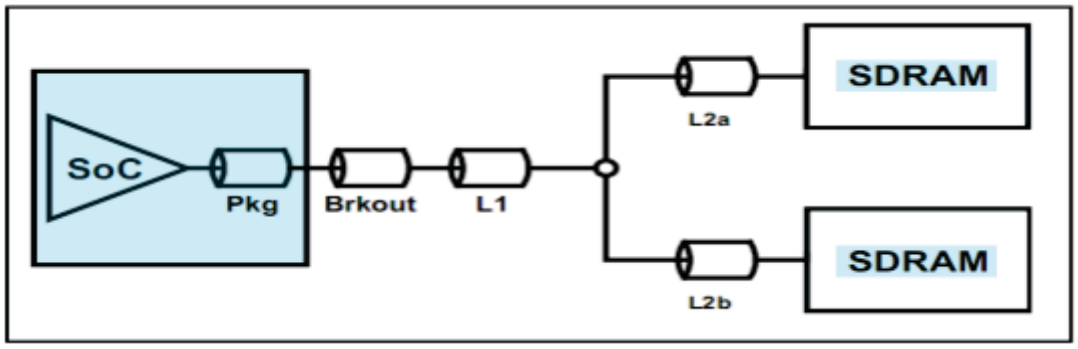


Figure 4-9 DDR3 Control（CTL）Signal Equivalent Circuit

DDR3 Control signals layout requirements are shown as Table 4-7

Table 4-7 RK3399 DDR3 Control（CTL）Layout Requirements

Items	Layout Requirements
Signal Group	CSn，CKE，ODT
Target Impedance (Z0)	50 Ohm ± 10%
CTL Routing Trace Width and Spacing within same Byte Group	Width : PCB stack-up dependent Spacing : ≥2 times the width of the trace
Max skew between CTL and CLK	10ps
Brkout	<100mil
L1	<1500mil
L2a, L2b	<700mil .length match L2a and L2b within 1 ps
Pkg+Brkout+L1+L2	<2100mil,including package length
Pkg	Refer to package report
Maximum allowed via	4

DDR3 Command signals equivalent circuit is shown as Figure 4-10.

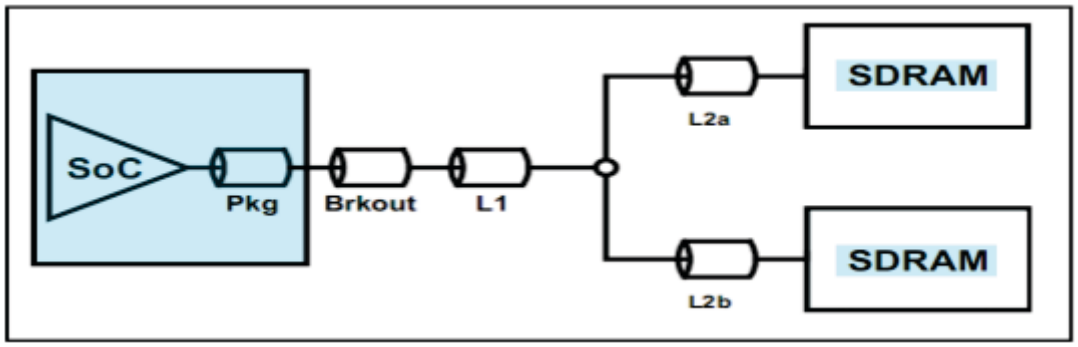


Figure 4-10 DDR3 Command（CMD）Signal Equivalent Circuit

DDR3 Command signals layout requirements are shown as Table 4-8

Table 4-8 RK3399 DDR3 Command（CMD）Layout Requirements

Items	Layout Requirements
Signal Group	DDR3_A[0:15], DDR3_CASn, DDR3_RASn, DDR3_WEn
Target Impedance (Z0)	50 Ohm ± 10%
CA Routing Trace Width and Spacing	Width : PCB stack-up dependent Spacing : ≥2 times the width of the trace
Max skew between CMD and CLK	10ps
Brkout	<100mil
L1	<1500mil
L2a, L2b	<700mil .length match L2a and L2b within 1 ps
Pkg+Brkout+L1+L2	<2100mil,including package length
Pkg	Refer to package report
Maximum allowed via	4

- 4.2.2.3 LPDDR4
  - One LPDDR4 SDRAM has four 16 bits channels, two channels share a ZQ pin, shown as Figure 4-11. In the design, only the A and B channel or C and D channel can be respectively combined as a 32bits channel, and connected respectively to the RK3399 two 32bits DDR controller.

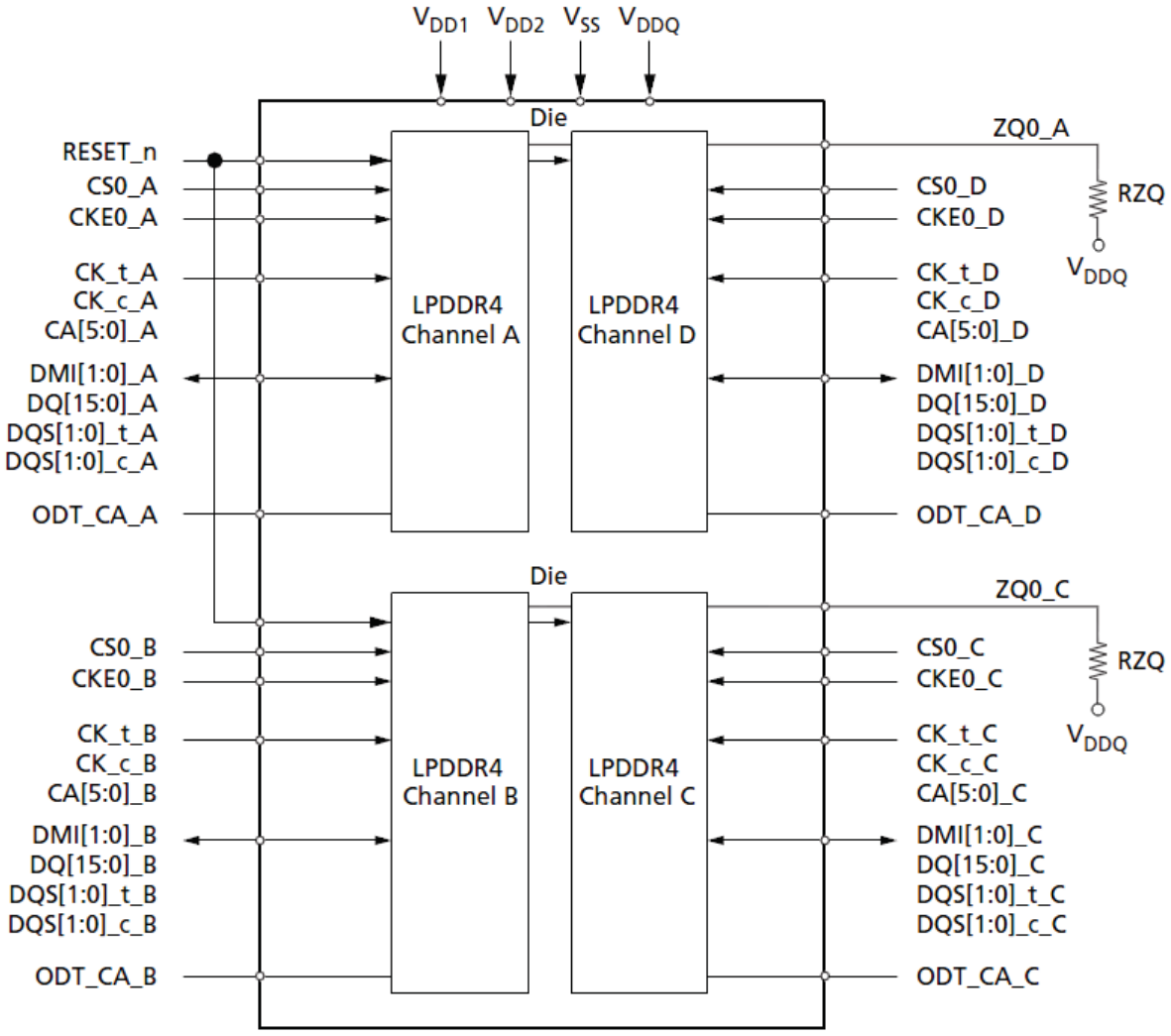


Figure 4-11 LPDDR4 SDRAM Block Diagram

- The RAQ of LPDDR4 SDRAM needs to be pulled-up to VDDQ by a 240 ohm resistor. The RZQ of RK3399 needs to be pulled-down to GND by a 240 ohm resistor.
- RK3399 can only support 2 rank of SDRAM.
- In LPDDR4 design, all data signals (DQ) of RK3399 must be connected to LPDDR4 pin-to-pin. That is, DDRn_D0-D15 must be connected to one channel D0-D15 of LPDDR4 pin-to-pin,and DDRn_D16-D31 must be connected to another channel D0-D15 of LPDDR4 pin-to-pin.The reason is that for one channel(16bits) LPDDR4,the MRR function needs to use DQ[0:7],the CA training function needs to use DQS0,DQ[0:6],DQ[8:13],and the RD DQ calibration function needs to use DQ[0:15] and DMI[1:0].
- The ODT of RK3399 DDR controller must be floating, and the ODT_CA of LPDDR4 must pulled-up to VDDQ.shown as Figure 4-12 and Figure 4-13.

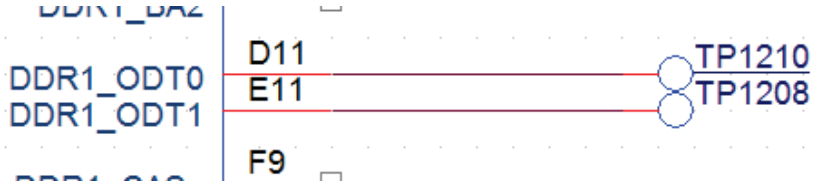


Figure 4-12 DDR Controller ODT

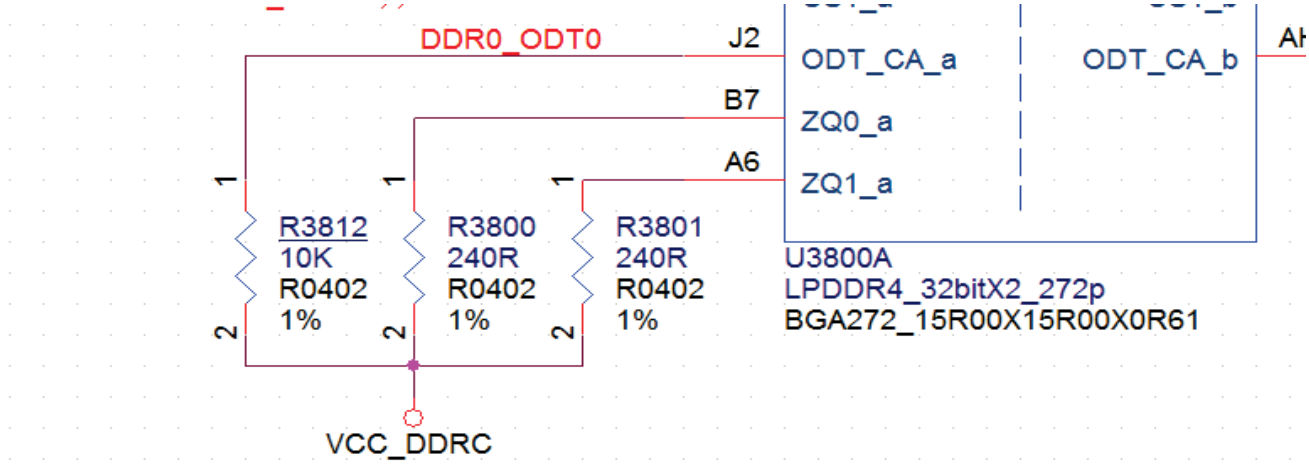


Figure 4-13 LPDDR4 ODT_CA

LPDDR4 Data signals equivalent circuit is shown as Figure 4-14

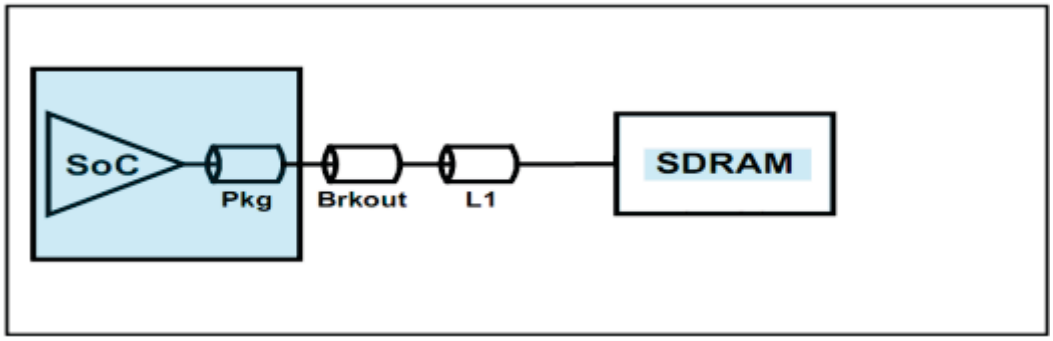


Figure 4-14 LPDDR4 DATA Equivalent Circuit

LPDDR4 data signals layout requirements are shown as Table 4-9:

Table 4-9 RK3399 DDR3 data Layout Requirements

Items	Layout Requirements
Signal Group	DQ，DM，DQS
Target Impedance (Z0:DQ; Zdiff: DQS)	DQ: 50 Ohm ± 10%, DQS: 100 Ohm ± 10% , DM: 50 Ohm ± 10%
DQS Routing Trace Width and Spacing within pair	PCB stack-up dependent
DQ Routing Trace Width and Spacing within same Byte Group	Width : PCB stack-up dependent Spacing : ≥2 times the width of the trace
DQS to DQ Spacing within same Byte Group	≥2 times the width of the trace
Byte Group to Byte Group Spacing, Data to Other Signals Spacing	≥2 times the width of the trace
Max intra-pair skew of DQS	1ps
Max skew between DQ and DQS	5ps
Note: DQ group A include：（DATA0oup A ， DQM0，DQS0P/ DQS0M） DQ group B include：（DATA8oup B i，DQM1，DQS1P/ DQS1M） DQ group C include：（DATA16up C in，DQM2，DQS2P/ DQS2M） DQ group D include：（DATA24up D in，DQM3，DQS3P/ DQS3M） The 5ps is the max skew inside DQ groups.It is no the requirement between DQ groups. Because max skew between CLK and DQS is 150ps,so the max skew between DQ groups is 150ps too.	

LPDDR4 CLK signals equivalent circuit is shown as Figure 4-15

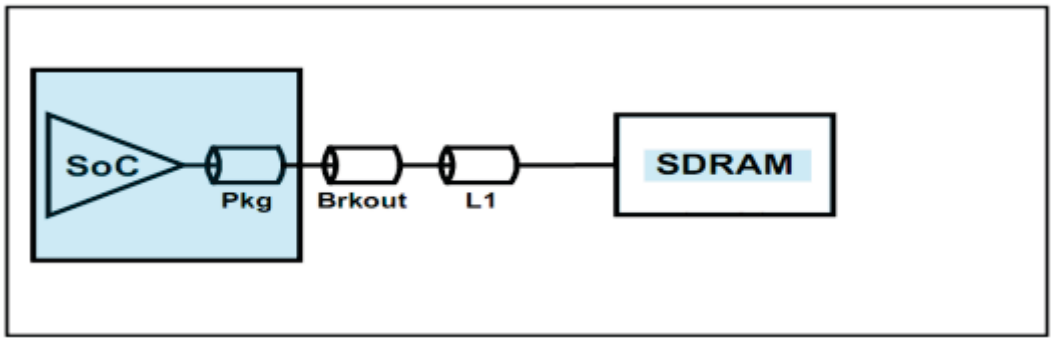


Figure 4-15 LPDDR4 CLK signals equivalent circuit

LPDDR4 CLK signals layout requirements are shown as Table 4-10:

Table 4-10 LPDDR4 CLK signals layout requirements

Items	Layout Requirements
Signal Group	CLK
Target Impedance (Diff Z0)	100 Ohm ± 10%
CLK Routing Trace Width and Spacing within pair	PCB stack-up dependent
CLK Routing Spacing to other Signals	≥2 times the width of the trace
Max intra-pair skew of CLK	1ps
Max skew between CLK and DQS	150ps

LPDDR4 Chip Select (CSn) signals equivalent circuit is shown as Figure 4-16

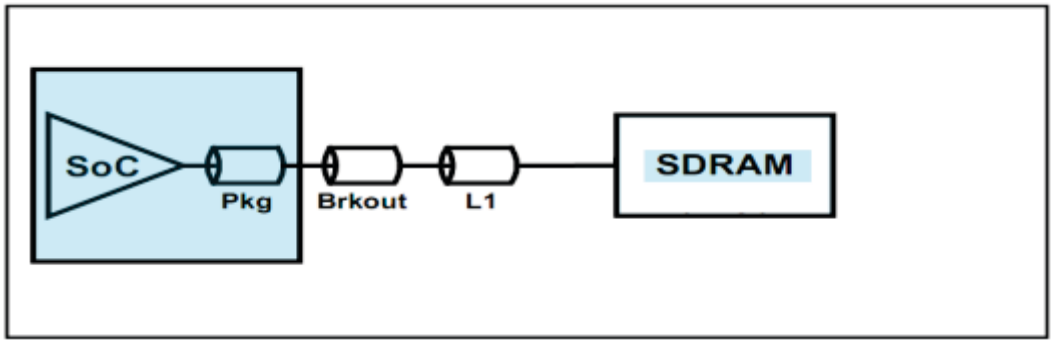


Figure 4-16 LPDDR4 CSn signals equivalent circuit

LPDDR4 Chip Select (CSn) signals layout requirements are shown as Table 4-11:

Table 4-11 LPDDR4 CSn signals layout requirements

Items	Layout Requirements
Signal Group	CS0n，CS1n，CS2n，CS3n
Target Impedance (Z0)	50 Ohm ± 10%
CSn Routing Trace Width and Spacing within same Byte Group	Width : PCB stack-up dependent Spacing : ≥2 times the width of the trace
Max skew between CSn and CLK	5ps

LPDDR4 Chip CKE signals equivalent circuit is shown as Figure 4-17

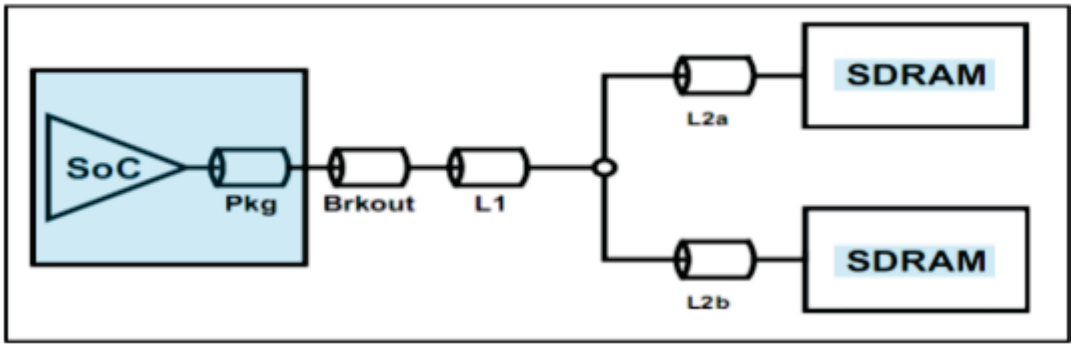


Figure 4-17 LPDDR4 Chip CKE signals equivalent circuit

LPDDR4 Chip CKE signals layout requirements are shown as Table 4-12:

Table 4-12 LPDDR4 Chip CKE signals layout requirements

Item	Layout Requirements
Signal Group	CKE0，CKE1
Target Impedance (Z0)	50 Ohm ± 10%
CKE Routing Trace Width and Spacing within same Byte Group	Width : PCB stack-up dependent Spacing : ≥2 times the width of the trace
Max skew between CKE and CLK	5ps
L2a，L2b	Length match L2a and L2b within 1 ps

LPDDR4 Chip Command(CMD) signals equivalent circuit is shown as Figure 4-18

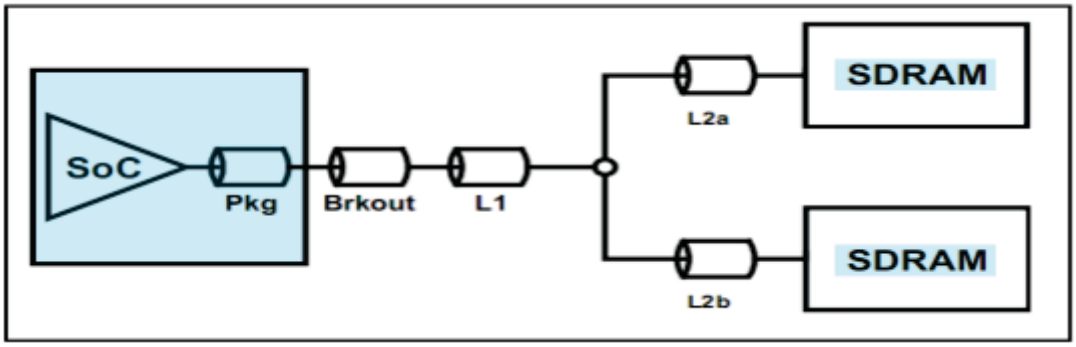


Figure 4-18 LPDDR4 Chip Command(CMD) signals equivalent circuit

LPDDR4 Chip CKE signals layout requirements are shown as Table 4-13:

Table 4-13 LPDDR4 Chip CKE signals layout requirements

Items	Layout Requirements
Signal Group	LPDDR4_A[0:5]
Target Impedance (Z0)	50 Ohm ± 10%
CA Routing Trace Width and Spacing	Width : PCB stack-up dependent Spacing : ≥2 times the width of the trace
Max skew between CMD and CLK	5ps
L2a, L2b	length match L2a and L2b within 1 ps

4.2.3 EMMC Design

EMMC V5.1 is increased Emmc_strobe signal compared with EMMC V4.5.

When RK3399 writes data down to eMMC, the reference clock is emmc_clk; the clock traces do not need to be equal to the data traces, since the controller has Timing Tunning function.

When RK3399 read data from eMMC, the reference clock is emmc_strobe; the clock traces must be equal to data traces, since eMMC could not support timing tunning.

eMMC layout requirements shown as Figure 4-19 and Figure 4-20.

- Data[0:7]、cmd、strobe traces as a group,parallel layout and the group traces should be shielded by GND traces,the requirement of equal length is ±100mil.

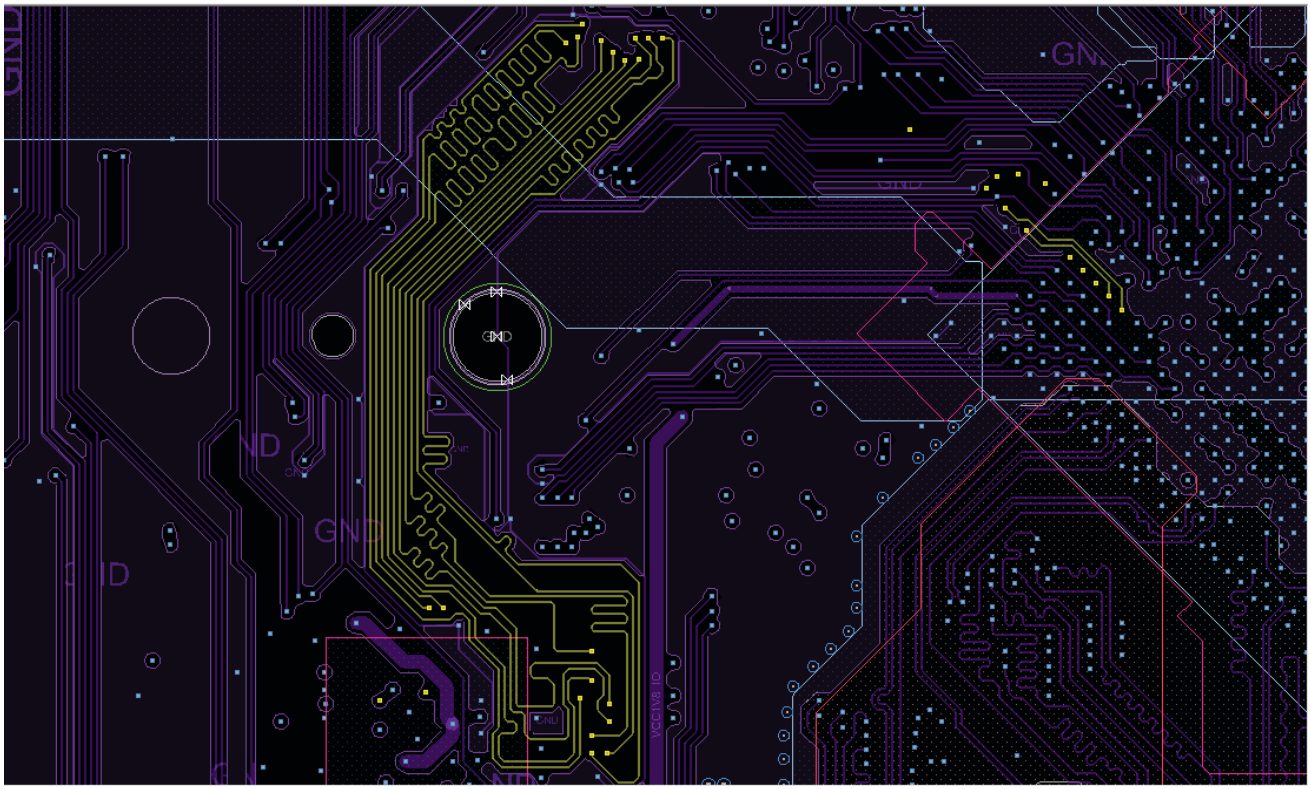


Figure 4-19 eMMC Traces（L4 view）

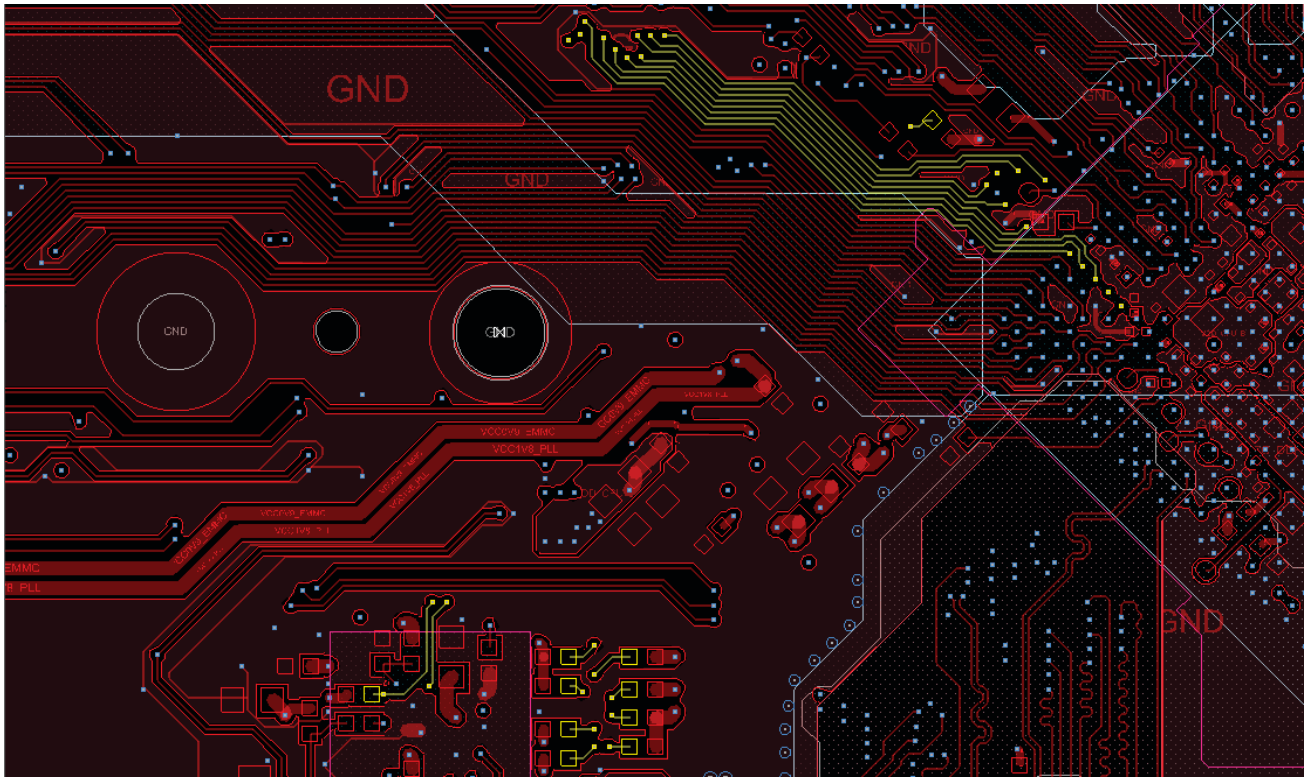


Figure 4-20 eMMC Traces（Bottom view）

- The CLK traces need to be shielded alone by GND traces.Shown as Figure 4-16 and Figure 4-17.

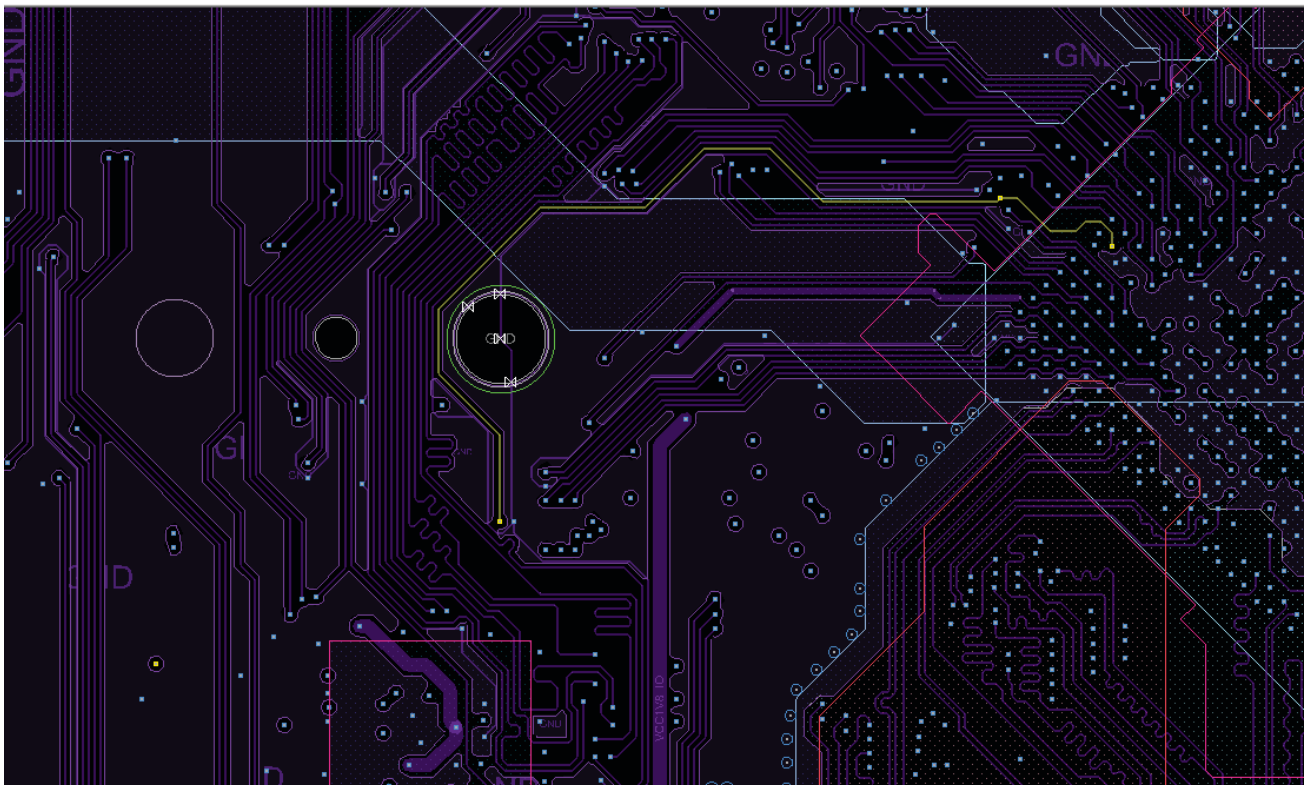


Figure 4-21 eMMC CLK Traces（L4 view）

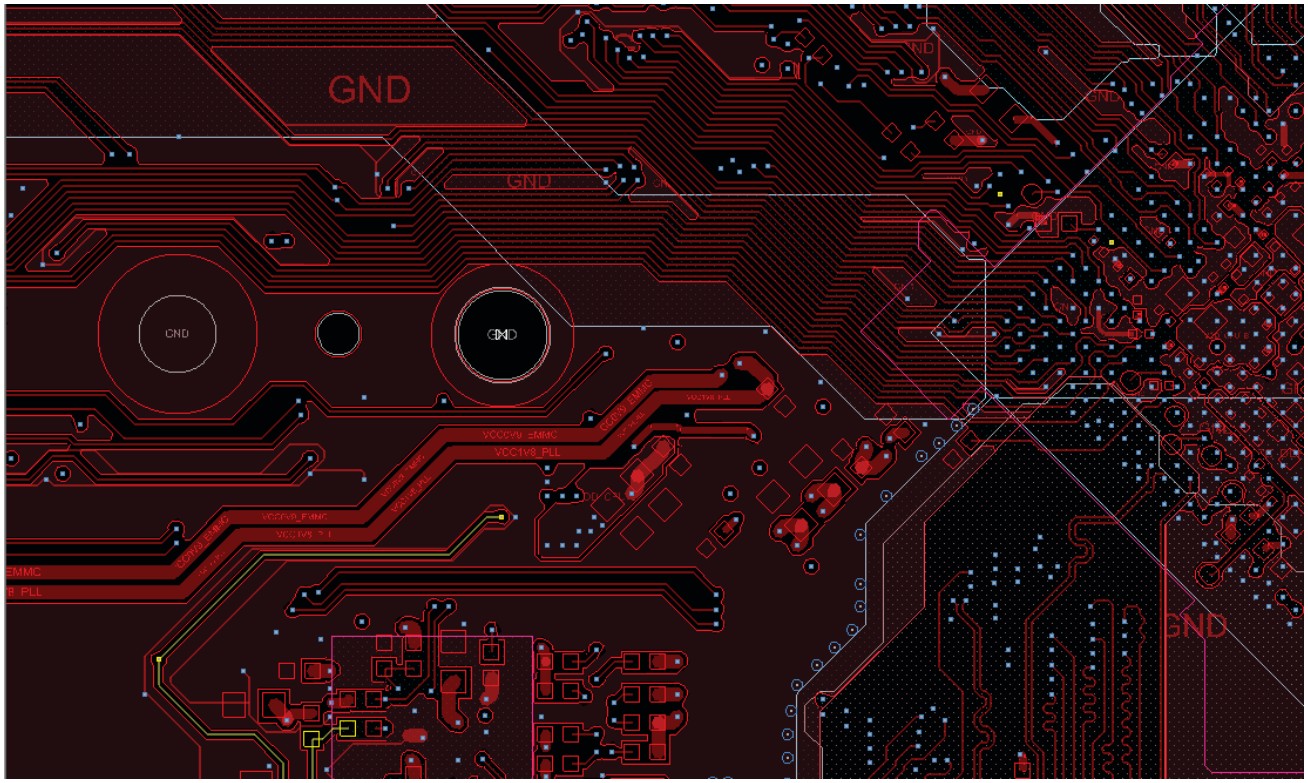


Figure 4-22 eMMC CLK Traces（Bottom view）

- The reserved pull-down resistor connected with Emmc_strobe should be placed close to the pin.

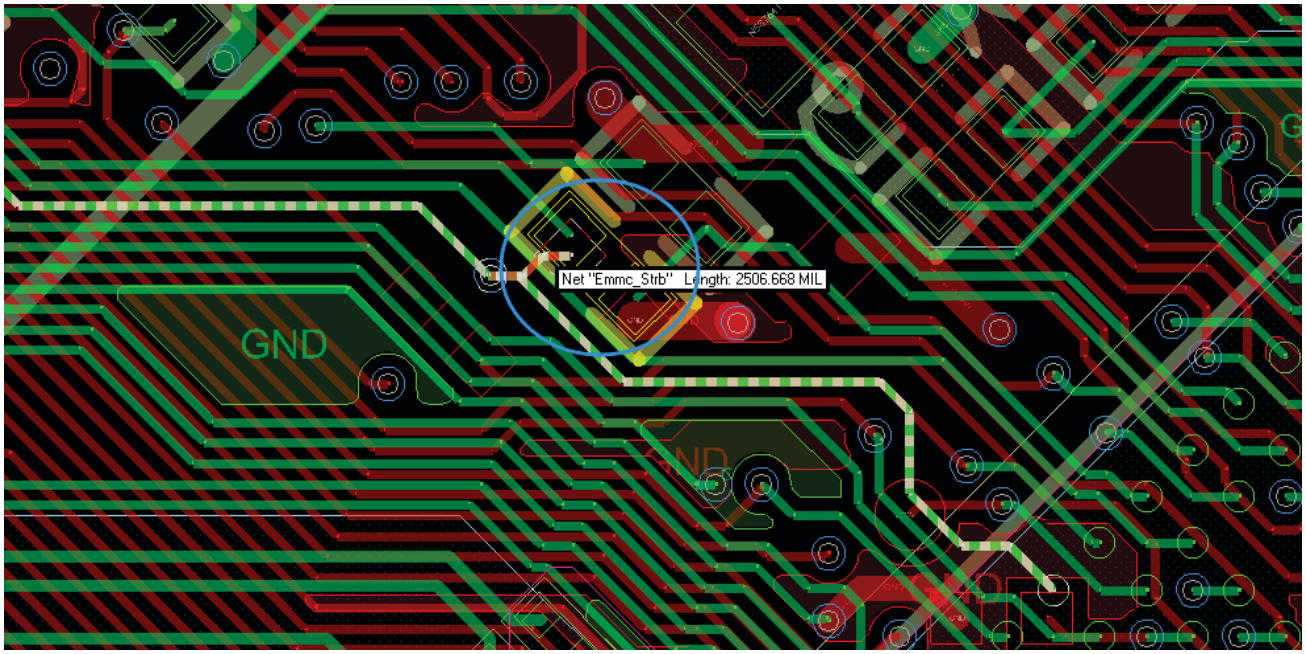


Figure 4-23 eMMC Strobe Resistor

eMMC layout requirements shown as Table 4-14:

Table 4-14 RK3399 eMMC Layout Requirement

Items	Layout Requirements
Trace Impedance	50Ω ±10% single ended
Max skew between data signal and clock	<20ps
Max trace length	<3.93inchs
The minimum spacing of EMMC Signals	At least 2 times the width of EMMC trace.
The minimum spacing between EMMC and other Signals	At least 3 times the width of EMMC trace.

4.2.4 PCIe Design

PCIe layout requirements as follow:

- The TXn[0:3] differential pairs order of PCIe can be adjusted according to the actual requirements,such as the TX0 of RK3399 can be connected to TX2 of device; the RXn[0:3] is the same too.But the P/N of the difference pairs could not be swapped
- The AC coupling capacitor should be placed close to PCIe connector
- The recommended package of AC coupling capacitor is using 0201 to reduce the impedance change in traces
- It is recommended to parallel layout of PCIe signals.Do not place any other signal traces and vias between them
- The differential pairs group should be shielded by GND traces, there is no need the GND shield traces between the differential pairs.

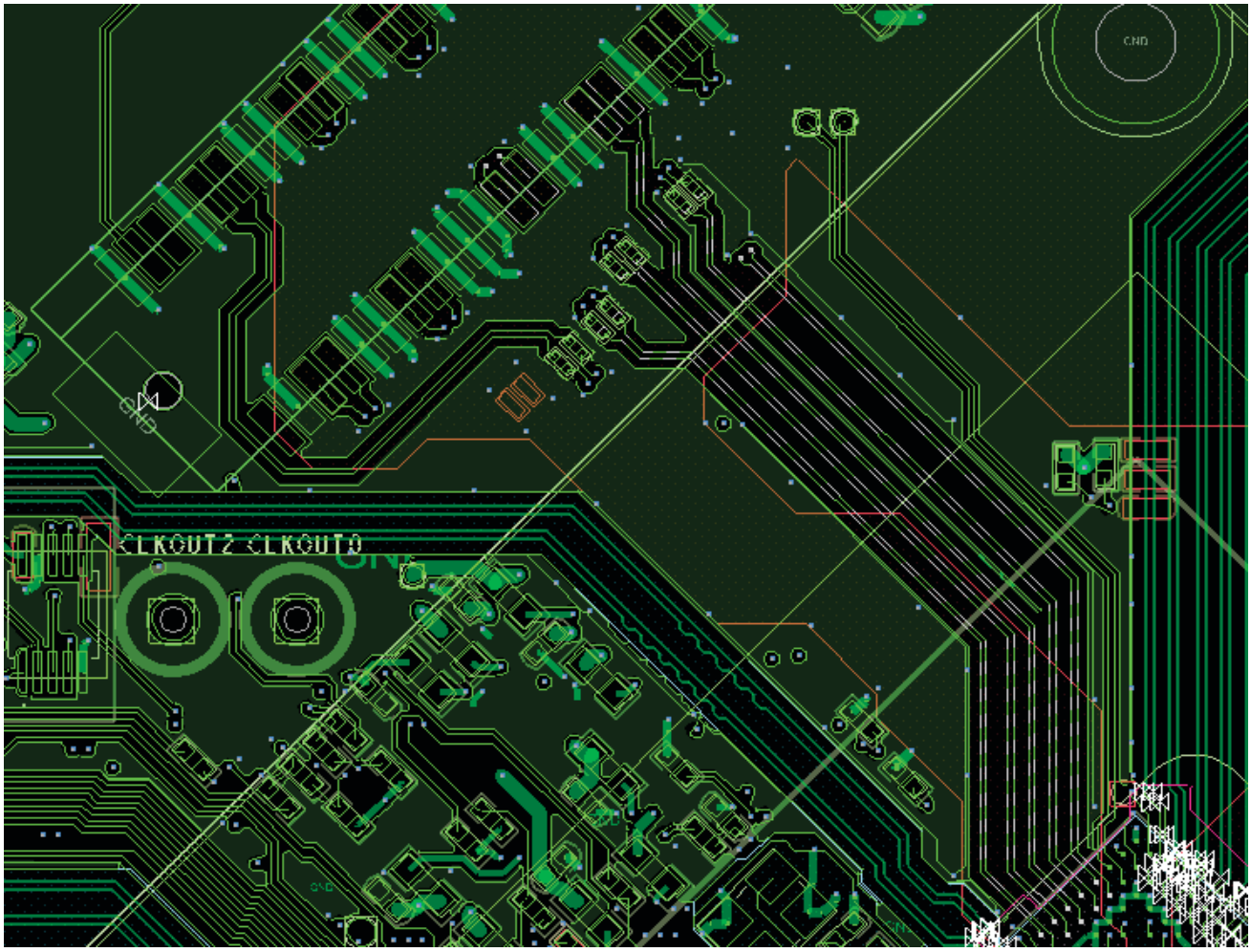


Figure 4-24 PCIe Layout Requirements

- The TX and RX differential pairs have lane-to-lane de-skew function, so they do not require strictly equal length.

PCIe layout requirements are shown as Table 4-15:

Table 4-15 RK3399 PCIe Layout Requirement

Items	Layout Requirements
Trace Impedance	100Ω ±10% differential
Max intra-pair skew	<4ps
Max inter-pair skew	<1.6ns
Maximum signal line length (coupled traces) TX and RX	<14 inchs
AC coupling capacitors	100nF ±20%, discrete 0201 package preferable
Minimum pair to pair spacing	>3 times the width of the trace. Try to increase spacing between pairs whenever it is possible.
Length matching between reference clock differential pairs REFCLK+ and REFCLK- (intra-pair)	<4ps
The minimum spacing between PCIE and other Signals	At least 3 times the width of PCIE trace
Maximum allowed via	4

4.2.5 USB 2.0 Design

USB 2.0 layout requirements are shown as below:

- The ESD parts must be placed close to USB connector.

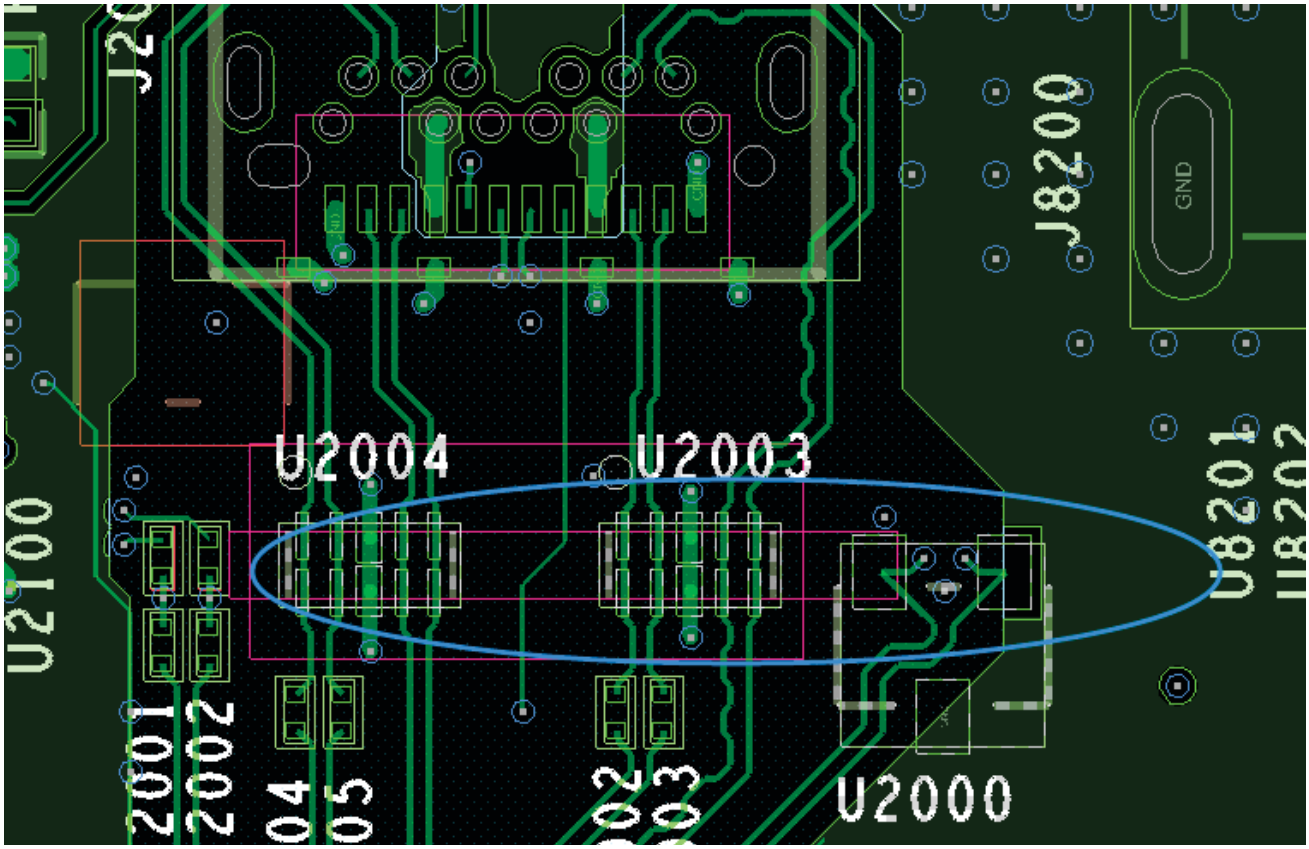


Figure 4-25 USB ESD Parts

- The USB connector should be placed close to SOC, to reduce the length of traces.
- The USB signal traces must be followed strictly by differential pair's rules requirements.The turning corners of signal traces should be as far as possible with arc or obtuse angle, not for right angle or

acute angle, shown as Figure 4-26.

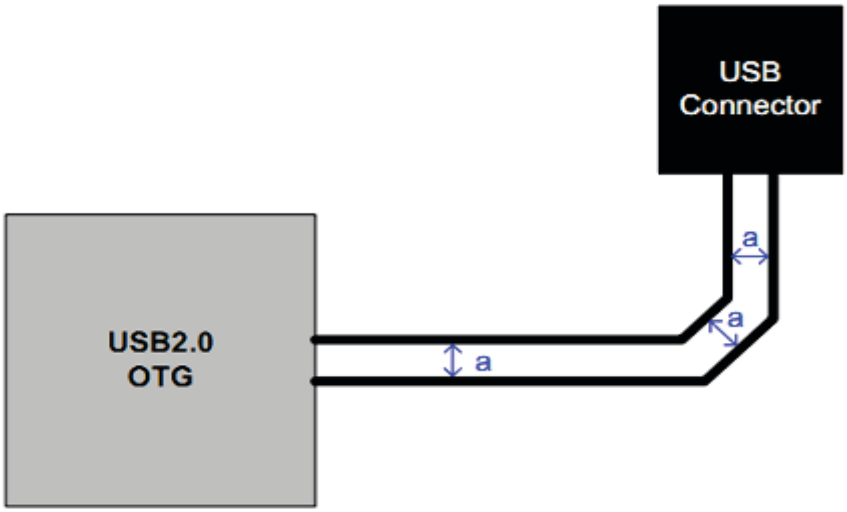


Figure 4-26 USB Layout Requirements

- In order to suppress EMI,the USB signal traces is recommended to be placed inner layer and ensure the reference plane is continuous and complete,otherwise,it will cause discontinuities in the traces impedance and increase the external noise on them.shown as Figure 4-27.

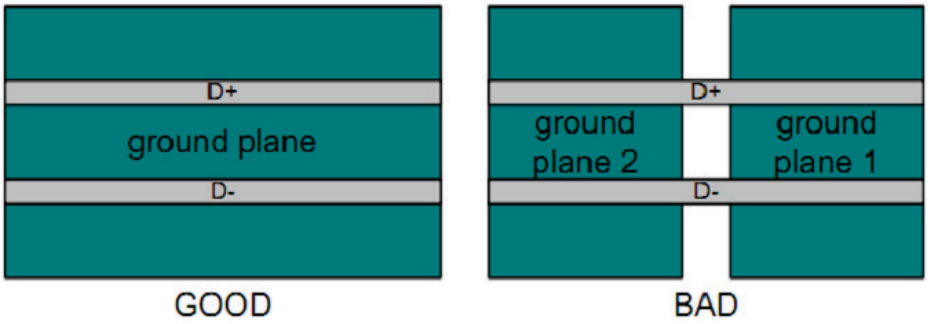


Figure 4-27 USB Signal Trace Reference Plane

- The USB traces at least need to be maintained clearance of 3W with other signals. Shown as Figure 4-28.

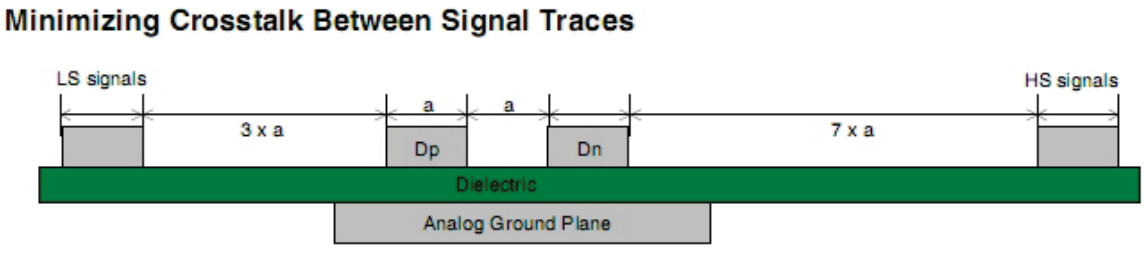


Figure 4-28 USB Layout

- To reduce the signal swap layers as possible in layout, via will cause the trace impedance to be discontinuous.
- The power traces width of USB 2.0 should be as wide as possible, it is necessary to consider the maximum current that may occur.

USB2.0 layout requirements are shown as Table 4-16:

Table 4-16 RK3399 USB2.0 Layout Requirement

Items	Layout Requirements
Trace Impedance	90Ω ±10% differential
Max intra-pair skew	<4ps
Max trace length on carrier board	<6 inchs
Maximum allowed via	6

4.2.6 USB 3.0 Design

USB 3.0 signals layout can basically refer to the section of 4.2.5.Please also note:

- USB 3.0 work mode is full duplex, so it does`t needs equal length between SS_TX and SS_RX.
- The SS_TX signal of USB 3.0 should add a 100nF AC coupling capacitor; they should be placed symmetrically and close to the USB connector.

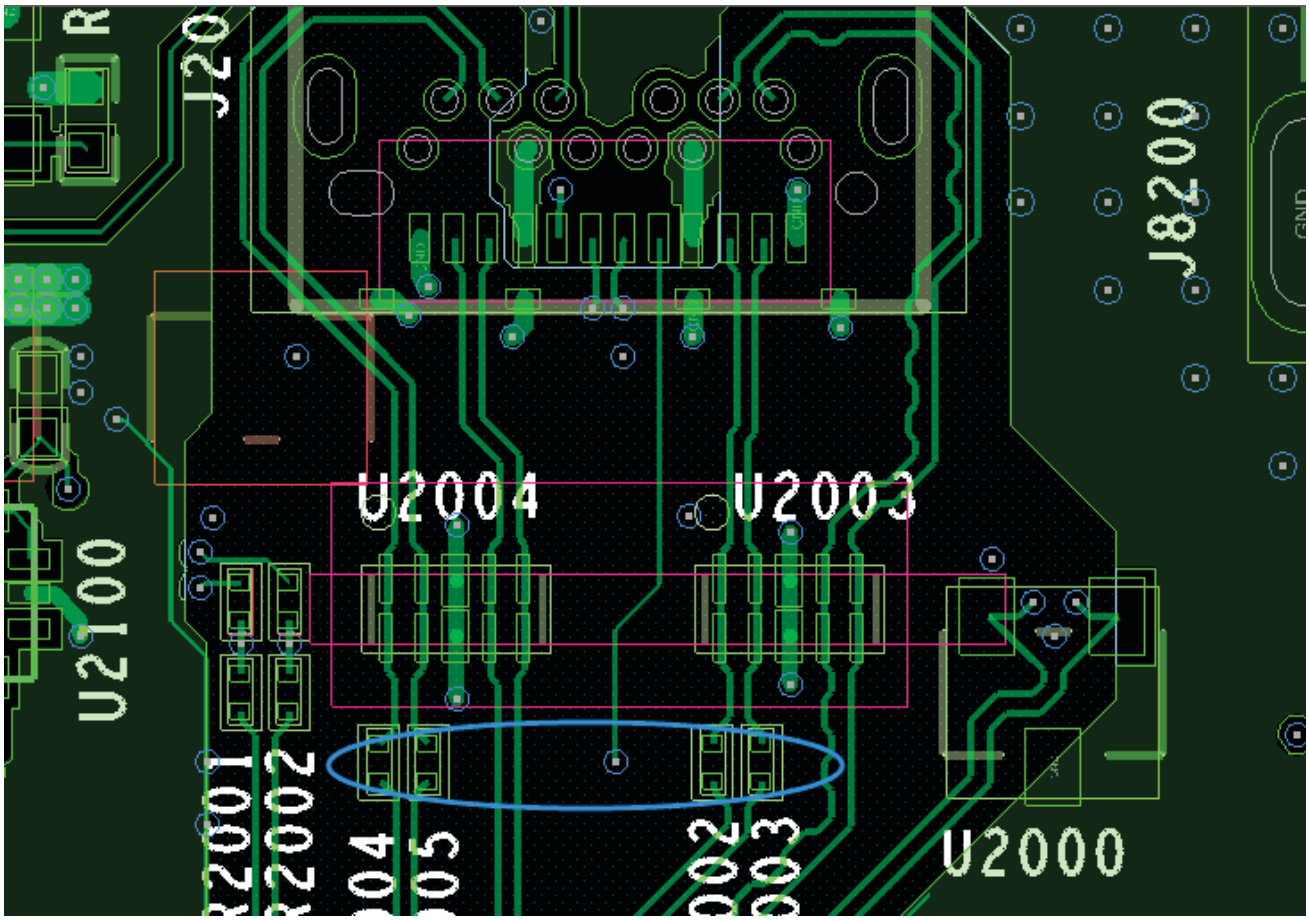


Figure 4-29 USB TX Coupling Capacitors Place Requirements 1

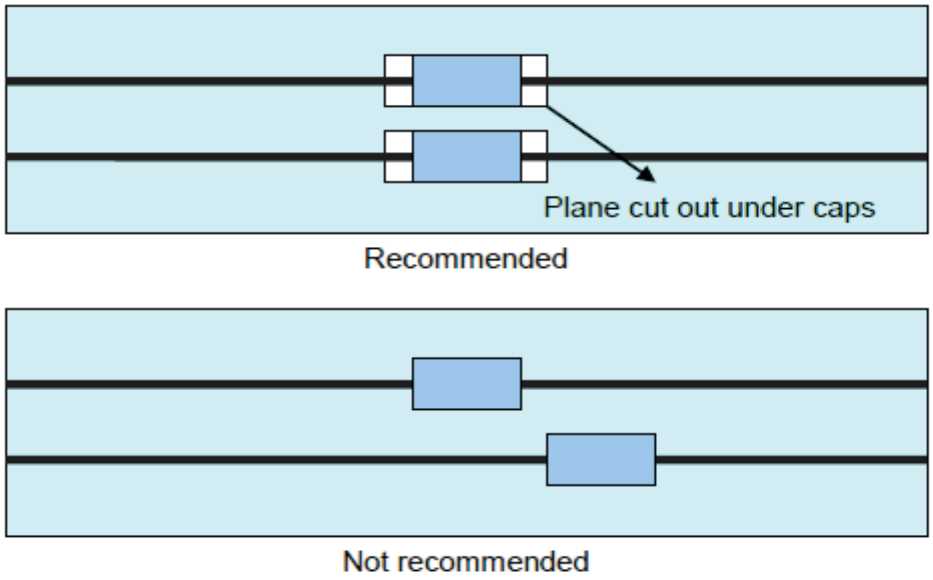


Figure 4-30 USB Coupling Capacitors Place Requirements 2

- The SS_TX and SS_RX signals must be followed strictly by differential pair's rules requirements, to ensure the continuity of trace impedance.

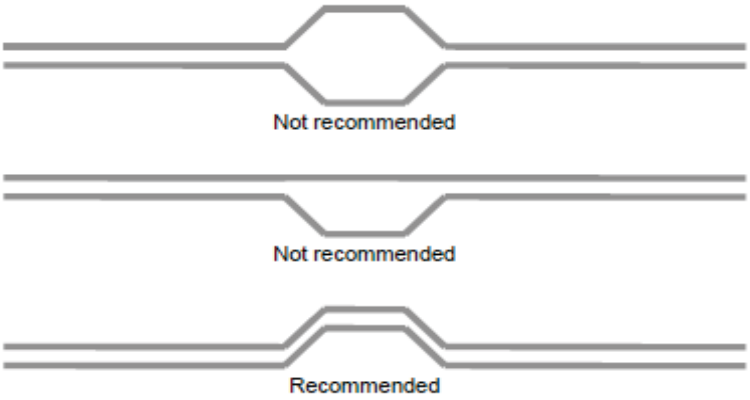


Figure 4-31 USB Signals Layout Requirements

- The delayed serpentine traces of SS_TX and SS_RX signal should be placed as close as possible to the source.Shown as Figure 4-27.

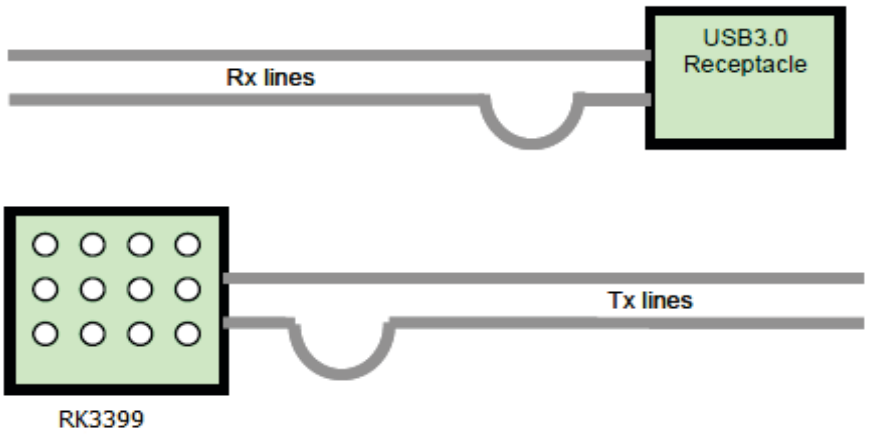


Figure 4-32 USB Signals Delay Requirements 1

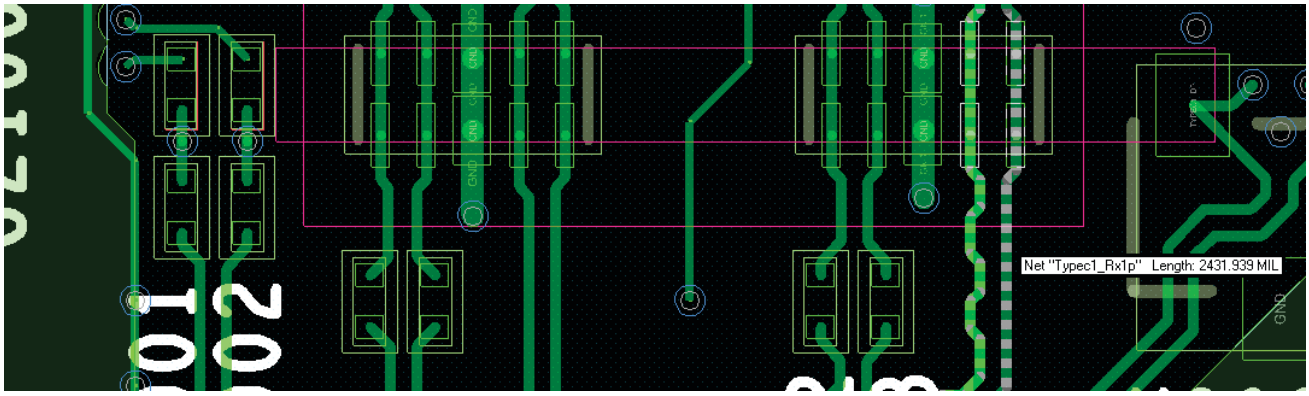


Figure 4-33 USB Signals Delay Requirements 2

- In order to suppress EMI, the USB signal trace is recommended to be placed inner layer and ensure the reference plane is continuous and complete, otherwise, it will cause discontinuities in the traces impedance and increase the external noise on them. If the differential pairs group is routed on the surface layer, it should be shielded by GND traces; there is no need the GND shield traces between the differential pairs.Shown as Figure 4-29.

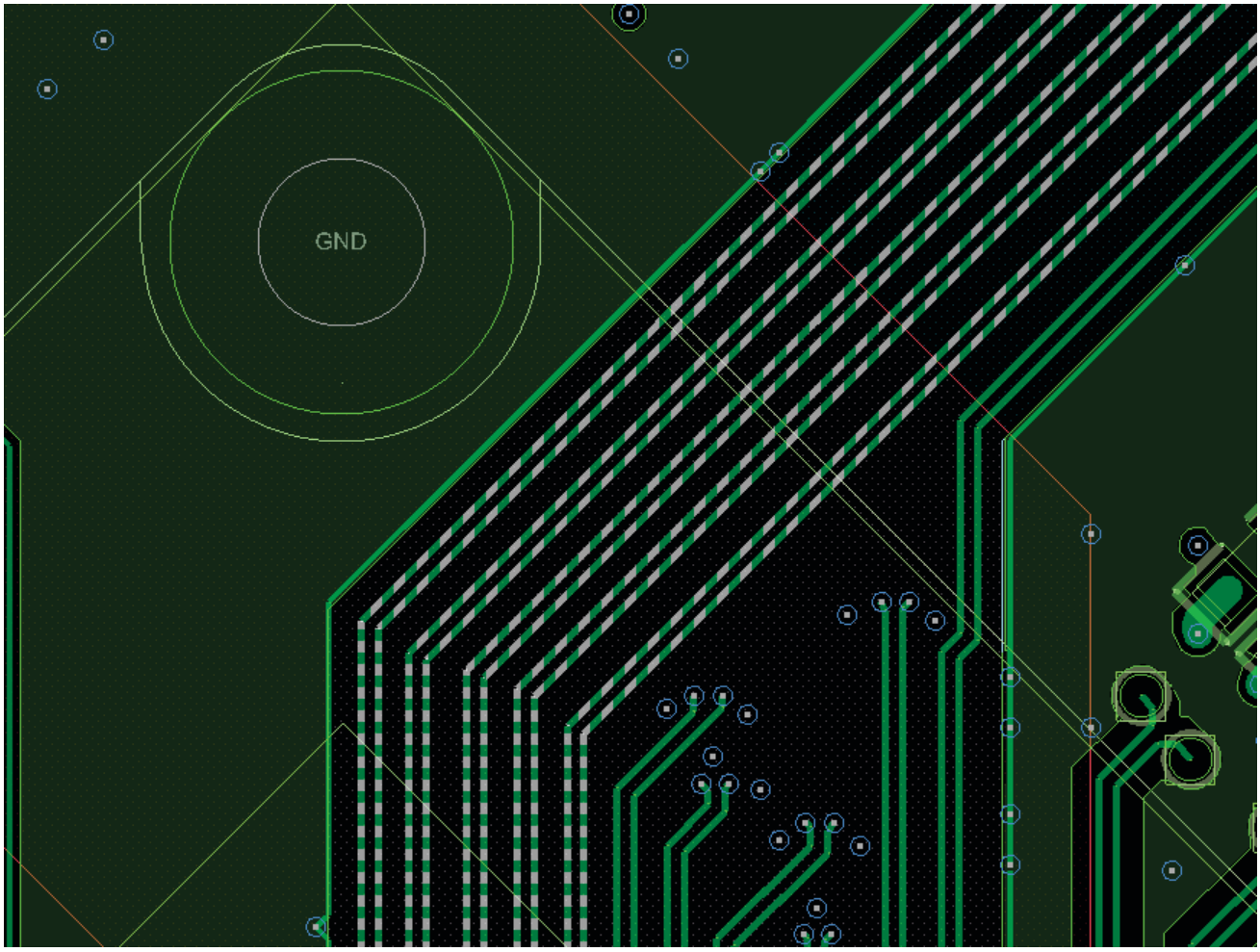


Figure 4-34 USB Signal Trace Shielding Requirements

USB3.0 signals layout requirements, shown as Table 4-17:

Table 4-17 RK3399 USB3.0 Layout Requirements

Items	Layout Requirements
Trace Impedance	90Ω ±10% differential
Max intra-pair skew	<4ps
Max trace length skew between RX and TX data pairs	<1.6ns

Max trace length on carrier board	<6inchs
AC coupling capacitors	100nF ±20%, discrete 0201 package preferable
Minimum pair to pair spacing	>3 times the width of the trace. Try to increase spacing between pairs whenever it is possible.
The minimum spacing between USB and other Signals	At least 3 times the width of USB trace.
Maximum allowed via	4

4.2.7 HDMI Design

HDMI layout notes:

- The reference clock of the HDMI TX signal is HDMI TXC, the 4 difference pairs, including the clock signal, needs to have equal length.
- The ESD parts should be placed close to HDMI connector.

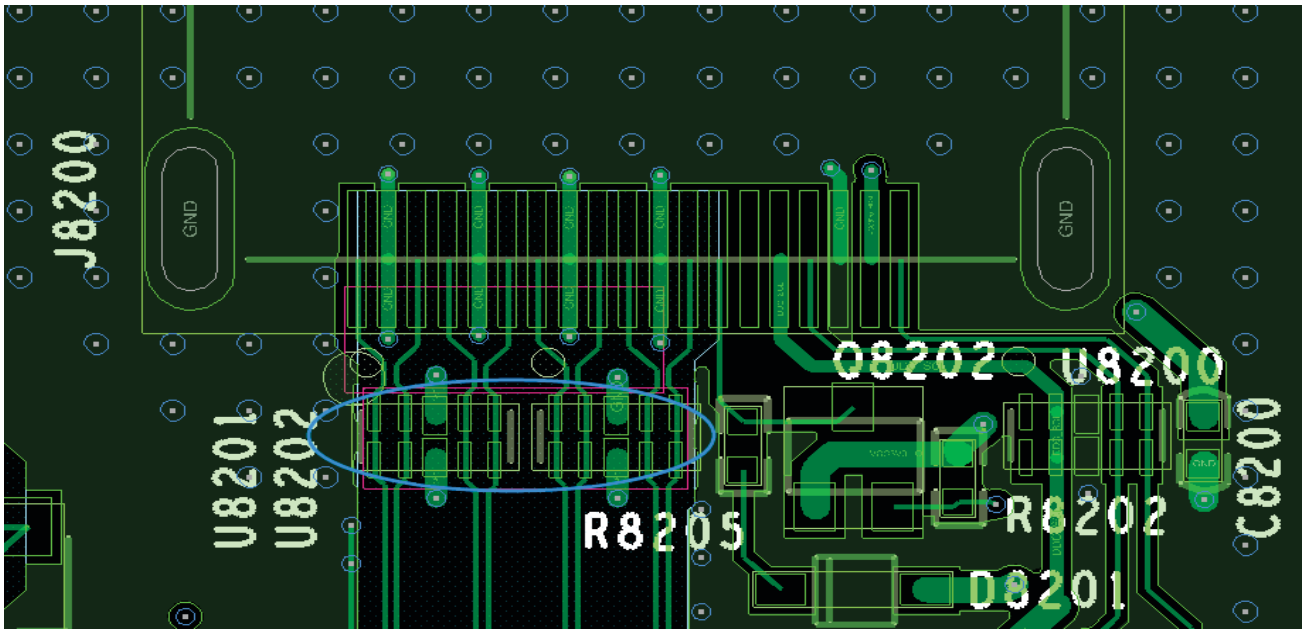


Figure 4-35 HDMI ESD Layout Requirements

- The reference plane of the HDMI signals should be continuous and complete; otherwise, it will cause discontinuities in the traces impedance and increase the external noise on them. If the differential pairs group is routed on the surface layer, it should be shielded by GND traces, there is no need the GND shield traces between the differential.

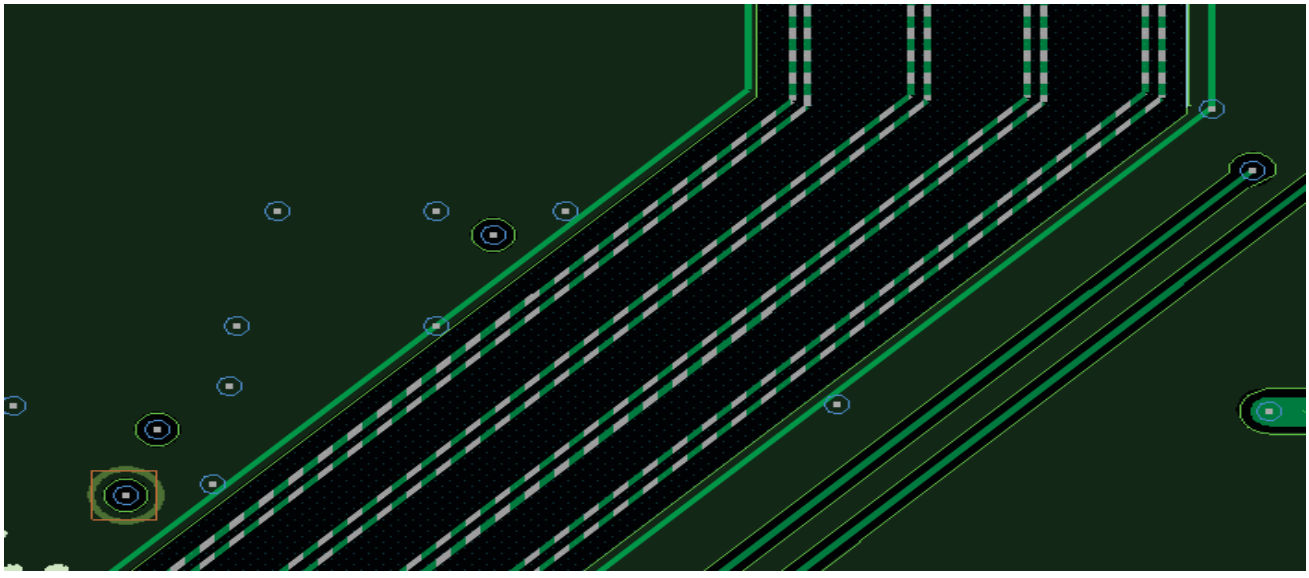


Figure 4-36 HDMI Signals Layout Requirements

- Use a cable with shielded, to improve EMI problems.
- The HDMI signals can be fan-outed in order, and be connected directly to HDMI connector.It is necessary to reduce the swap layer in layout to avoid impedance discontinuities.If it is not avoidable because of the mold structure, the impedance change is recommended to be controlled within 10%.and a GND via should be placed close to the signal swap via.

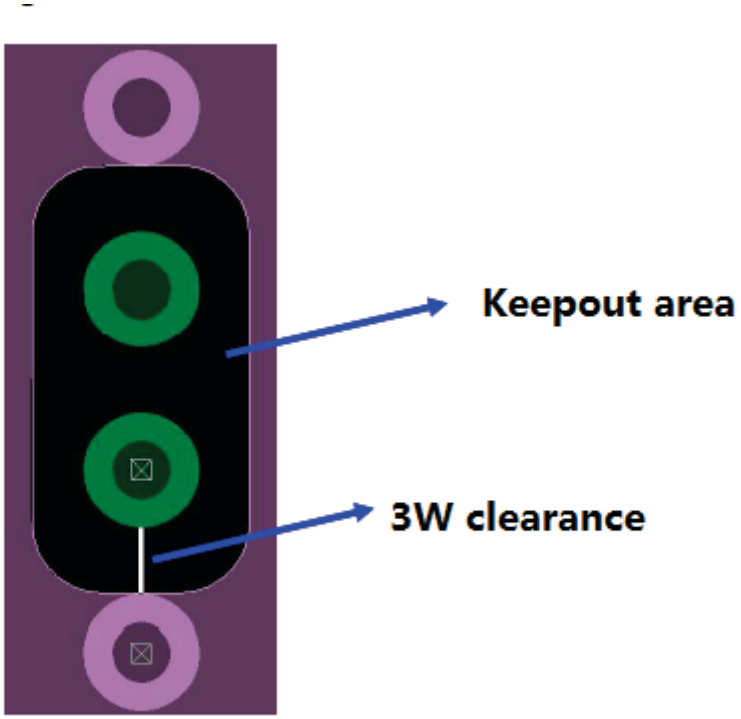


Figure 4-37 HDMI Signals Swap Via Requirements

HDMI layout requirements are shown as Table 4-18:

Table 4-18 RK3399 HDMI Layout Requirements

Items	Layout Requirements
Trace Impedance	100Ω ±10%
Max intra-pair skew	<4ps
Max trace length skew between clock and data pairs	<80ps
Max trace length on carrier board	9.8 inch
Minimum pair to pair spacing	>3 times the width of the trace. Try to increase spacing between pairs whenever it is possible
The minimum spacing between HDMI and other Signals	At least 3 times the width of HDMI trace
Maximum allowed via	4

4.2.8 eDP Design

eDP layout notes:

- The reference clock of eDP is built into data and the the clock signal is restored at the receiving end, so the 4 sets of data differential pairs need to have equal length.
- The coupling capacitor of eDP signals should be placed close to RK3399.

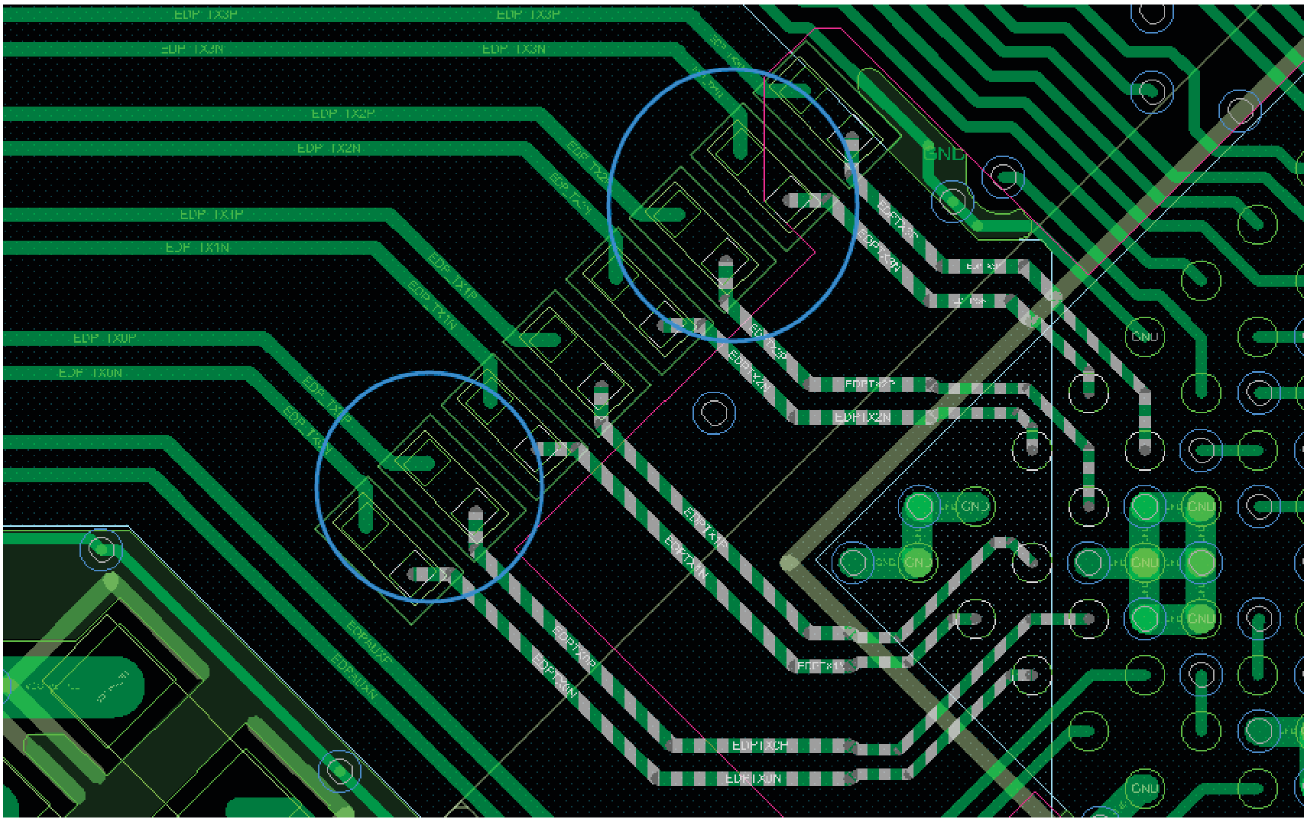


Figure 4-38 eDP Coupling Capacitor

- In order to suppress EMI, the eDP signal traces is recommended to be placed inner layer and ensure the reference plane is contiguous and complete, otherwise, it will cause discontinuities in the traces impedance and increase the external noise on them. If the differential pairs group be routed on the surface layer, it should be shielded by GND traces; there is no need the GND shield traces between the differential pairs.

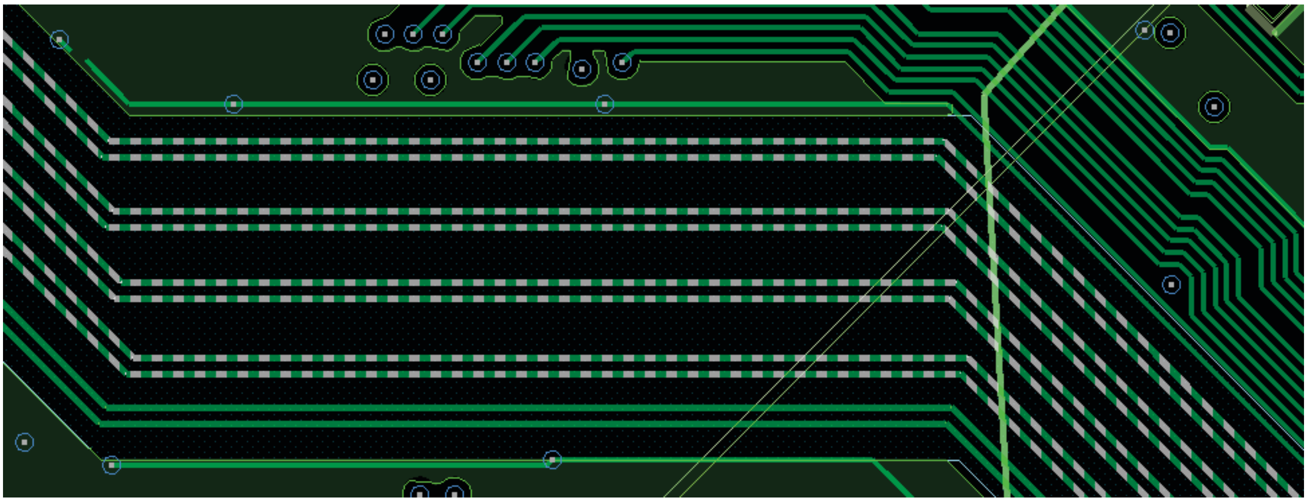


Figure 4-39 eDP Layout

eDP layout requirements are shown as Table 4-19:

Table 4-19 RK3399 eDP Layout Requirements

Items	Layout Requirements
Trace Impedance	100Ω ±10% differential
Max intra-pair skew	<4ps
Max trace length on carrier board	<6inch
Minimum pair to pair spacing	>3 times the width of the trace.Try to increase spacing between pairs whenever it is possible.
AC coupling capacitors	100nF ±20%, discrete 0201 package preferable
The minimum spacing between eDP and other Signals	At least 3 times the width of eDP trace.
Maximum allowed via	4

4.2.9 DP Design

DP signals layout can basically refers to the section of 4.2.6.Please also note:

- The reference clock of DP is built into data and the the clock signal is restored at the receiving end, so the 4 sets of data differential pairs need to have equal length.
- The coupling capacitor of DP signals should be placed close to RK3399.
- In order to suppress EMI, the DP signal traces is recommended to be placed inner layer and ensure the reference plane is contiguous and complete, otherwise, it will cause discontinuities in the traces impedance and increase the external noise on them. If the differential pairs group be routed on the surface layer, it should be shielded by GND traces; there is no need the GND shield traces between the differential pairs.
- When USB3.0 use as DP output,the inpadence of DP differential signals is 100ohm; When USB3.0 use as Type- C output, in order to maintain compatibility with the USB protocol, the inpadence of DP differential signals is 90ohm.

DP layout requirements are shown as Table 4-20:

Table 4-20 RK3399 DP Layout Requirements

Items	Layout Requirements
Trace Impedance	100Ω ±10% differential(DP ouput mode) 90Ω ±10% differential(Type-C mode)
Max intra-pair skew	<4ps
Max trace length on carrier board	<6inch
Minimum pair to pair spacing	>3 times the width of the trace.Try to increase spacing between pairs whenever it is possible.
AC coupling capacitors	100nF ±20%, discrete 0201 package preferable
The minimum spacing between DP and other Signals	At least 3 times the width of DP trace.
Maximum allowed via	4

4.2.10 MIPI DSI Design

MIPI DSI layout notes:

- In order to suppress EMI, the MIPI DSI signal traces is recommended to be placed inner layer and ensure the reference plane is contiguous and complete, otherwise, it will cause discontinuities in the traces impedance and increase the external noise on them. If the differential pairs group be routed on the surface layer, it should be shielded by GND traces; there is no need the GND shield traces between the differential pairs.
- The delayed serpentine traces of MIPI DSI signal should be placed as close as possible to the source.Shown as Figure 4-35.

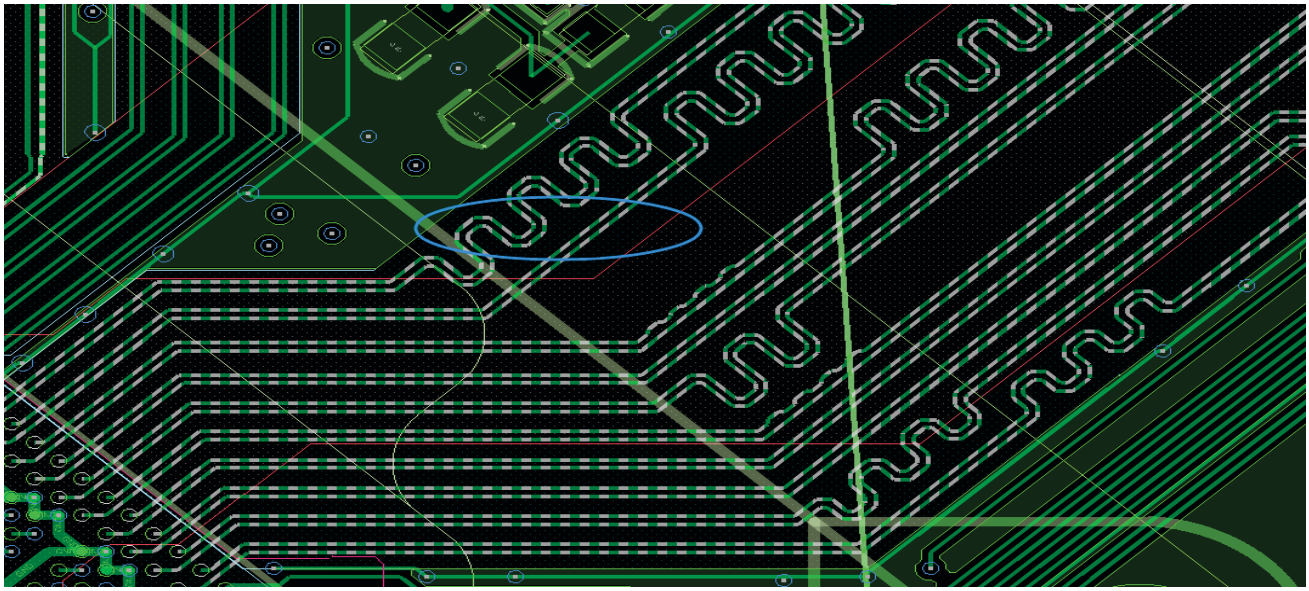


Figure 4-40 MIPI DSI Layout

MIPI layout requirements are shown as Table 4-21:

Table 4-21 RK3399 MIPI Layout Requirements

Items	Layout Requirements
Trace Impedance	100Ω ±10% differential
Max intra-pair skew	<4ps
Max trace length skew between clock and data pairs	<7ps
Max trace length	<7.2inch
Maximum allowed via	Minimize the number of via in each lane
Minimum pair to pair spacing	>3 times the width of the trace.Try to increase spacing between pairs whenever it is possible.
The minimum spacing between Mipi and other Signals	At least 3 times the width of Mipi trace.

4.2.11 SDIO/SDMMC Design

SDIO/SDMMC layout notes:

- The CLK signal should be shielded by GND. DATA alignment spacing should comply with 3W rules and ensure the reference plane is contiguous and complete.

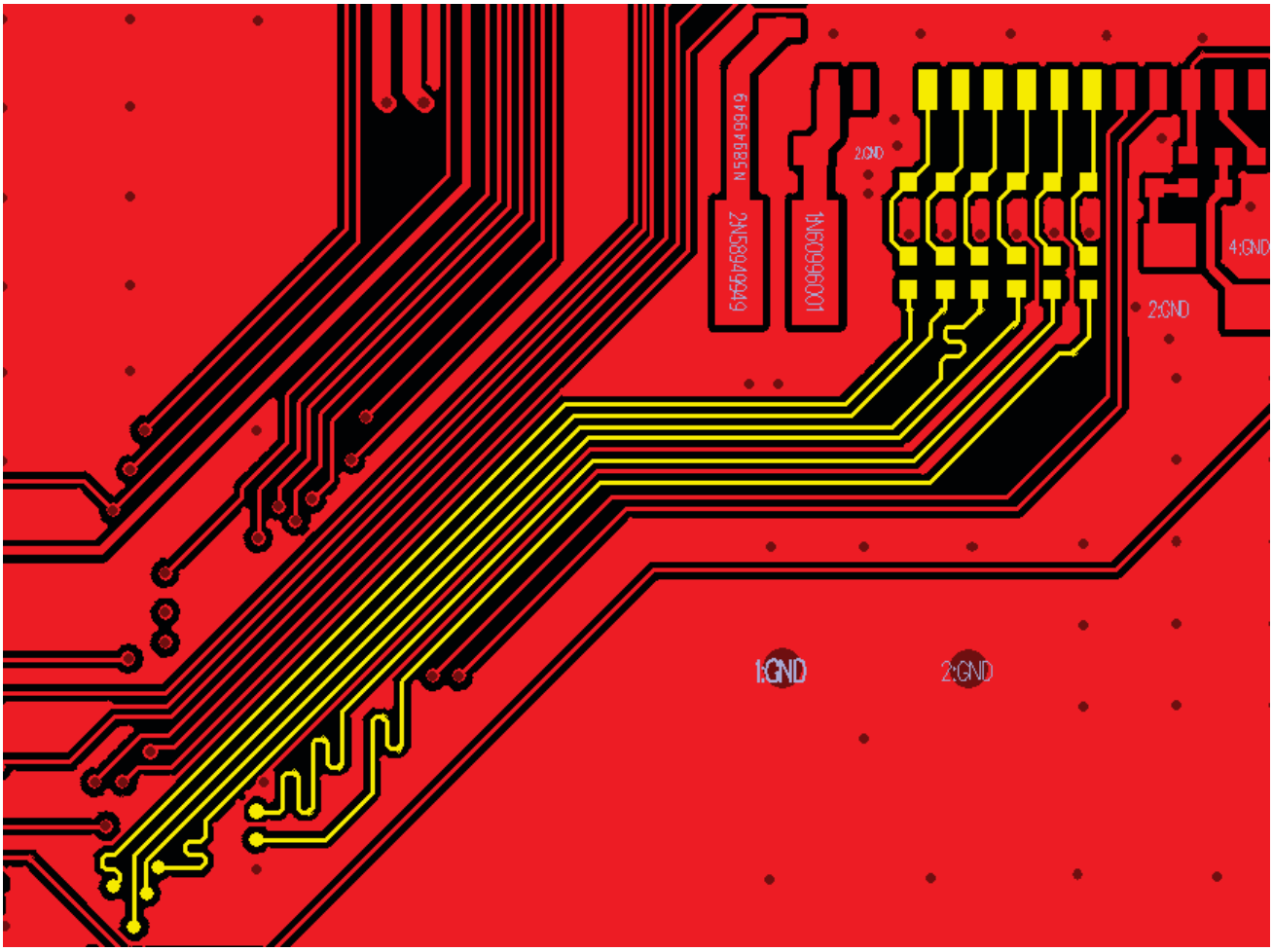


Figure 4-41 SDIO/SDMMC Layout 1

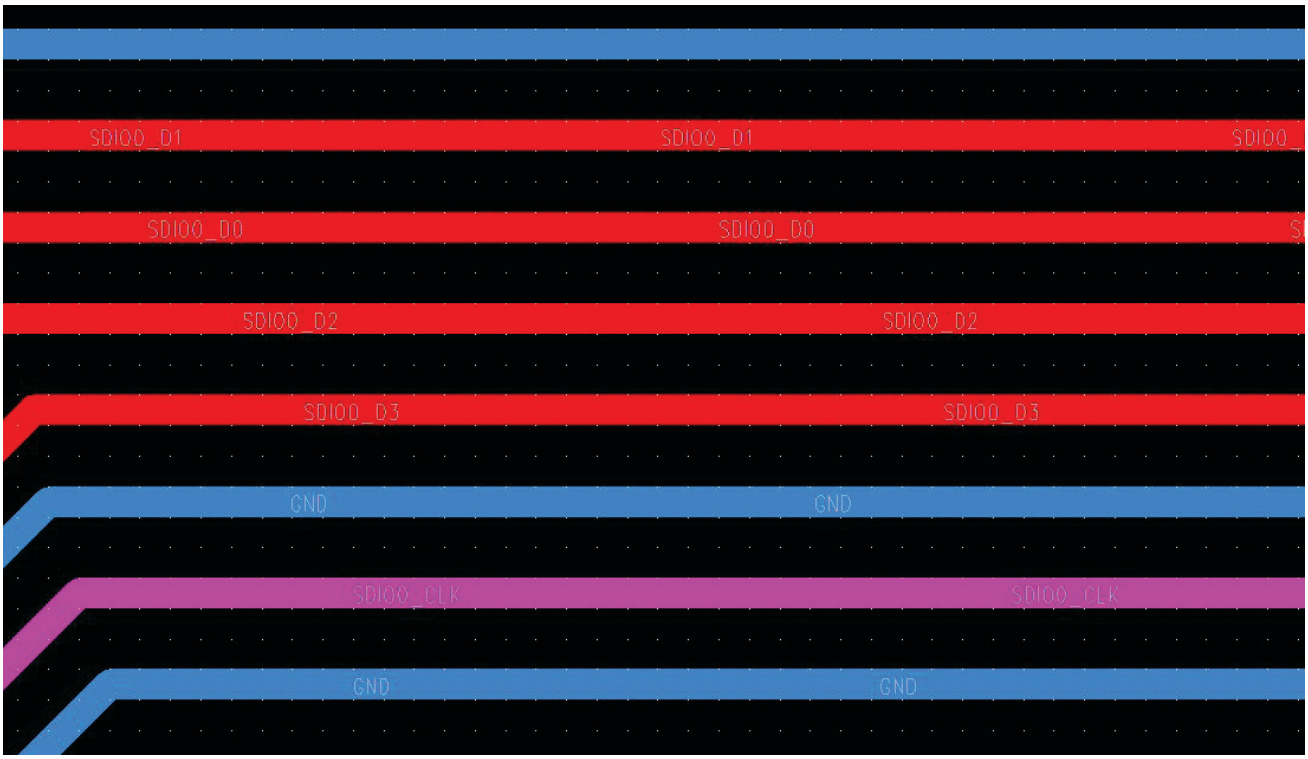


Figure 4-42 SDIO/SDMMC Layout 2

- The load capacitor including SD card and PCB, the load capacitor of SD card in protocol should be less than 10 pF.

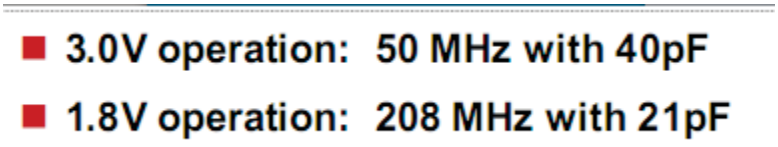


Figure 4-43 SDMMC Loading Capacitor

3. Card capacitance range is defined as follows:

Capacitance	Min	Max	Units	Notes
C_{CARD} (C_{DIE} + C_{PKG})	5	10	pF	---

Table 6-10 : Card Capacitance Range

Figure 4-44 SD Card Load Capacitor

SDIO/SDMMC layout requirements are shown as Table 4-22:

Table 4-22 RK3399 SDIO/SDMMC Layout Requirements

Items	Layout Requirements
Trace Impedance	50Ω ±10% single ended
Max skew between data signal and clock	<20ps
Max trace length	<3.93 inch
The minimum spacing of SDIO Signals	At least 2 times the width of SDIO trace.

4.2.12 MAC Design

- The shorter traces of RGMII, the better EMI, and so PHY should be placed as close as possible to RK3399. The length of RGMII traces must be less than 6 inch.
- The series resistor should be placed close to PHY to improve EMI.Shown as Figure 4-40.
  - The MAC_RXCLK should be shielded with GND traces.
  - Layout alignment spacing should be complied with 3W rules.
  - The traces length of RXD [0:3], RXCLK, RXDV should be equal, the difference should be less than 100 mil.The traces length should be less than 6 inch.
  - The reference plane is contiguous and complete, could not be directly parallel to other signal traces.

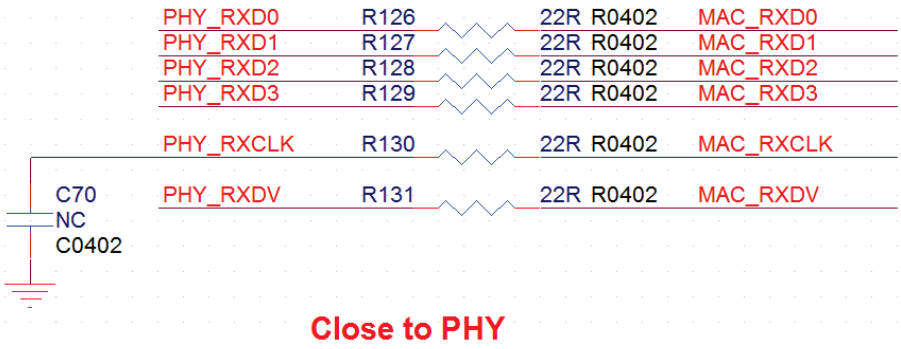


Figure 4-45 MAC RX Series Resistor

- The series resistor should be placed close to RK3399，shown as Figure 4-46.
  - The PHY_TXCLK needs to be shielded by GND traces.
  - Layout alignment spacing should to be complied with 3W rules.
  - The traces length of TXD [0:3], TXCLK, TXEN need to be equal, the difference should be less than 100 mil.The traces length needs to be less than 6 inch.

- The reference plane of signal traces should be contiguous and complete, and could not be directly parallel to another signal traces.

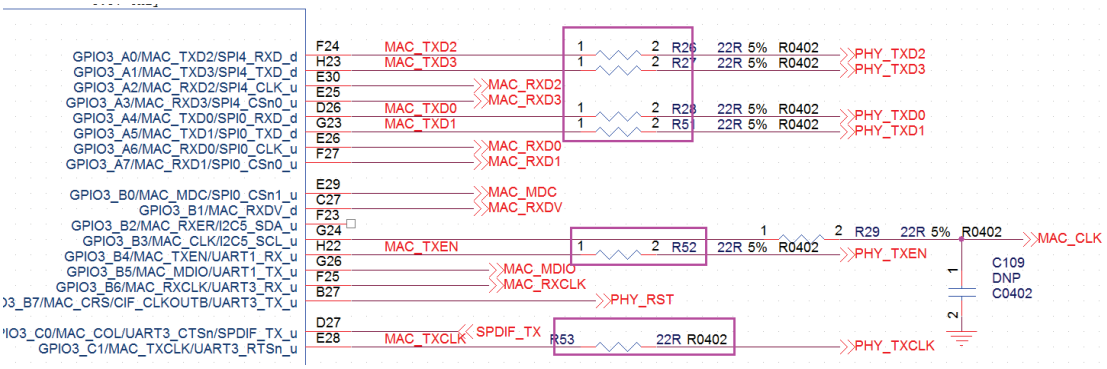


Figure 4-46 MAC TX Series Resistor

- R102 needs to be placed close to PHY, and needs to be shielded by GND traces, and the reference plane needs contiguous and complete.

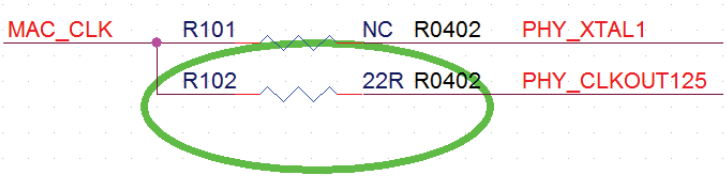


Figure 4-47 MAC CLK Branch Resistor

- The decoupling capacitor should be placed close to RK3399 power pin.Shown as Figure 4-48.

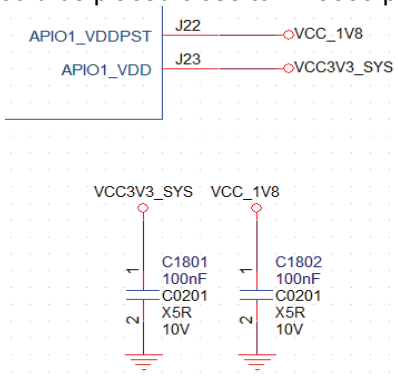


Figure 4-48 MAC Power Decoupling Capacitor

4.3 RF PCB Design

4.3.1 WIFI/BT Design

WIFI module communicates with RK3399 via SDIO interface. BT module communicates with RK3399 via UART and PCM interface.

For layout, please note the WIFI/BT module must be far from the traces and connectors of high-speed signals, such as DDR, HDMI and USB and so on.The crystal circuit needs to be placed close to the module, avoid being interfered. There is no any other signal traces could be placed in the area of crystal circuit.

The max frequency of SDIO3.0 is up to 208 MHz, and so the SDIO signals must avoid being interfered in layout.Shown as Figure 4-49. The reference plane of signal traces needs to be contiguous and complete, could not be directly paralleled to other signal traces.The data signal group needs to be shielded with GND traces, the clk needs to be shielded alone with GND traces. Layout alignment spacing should be complied with 3W rules.

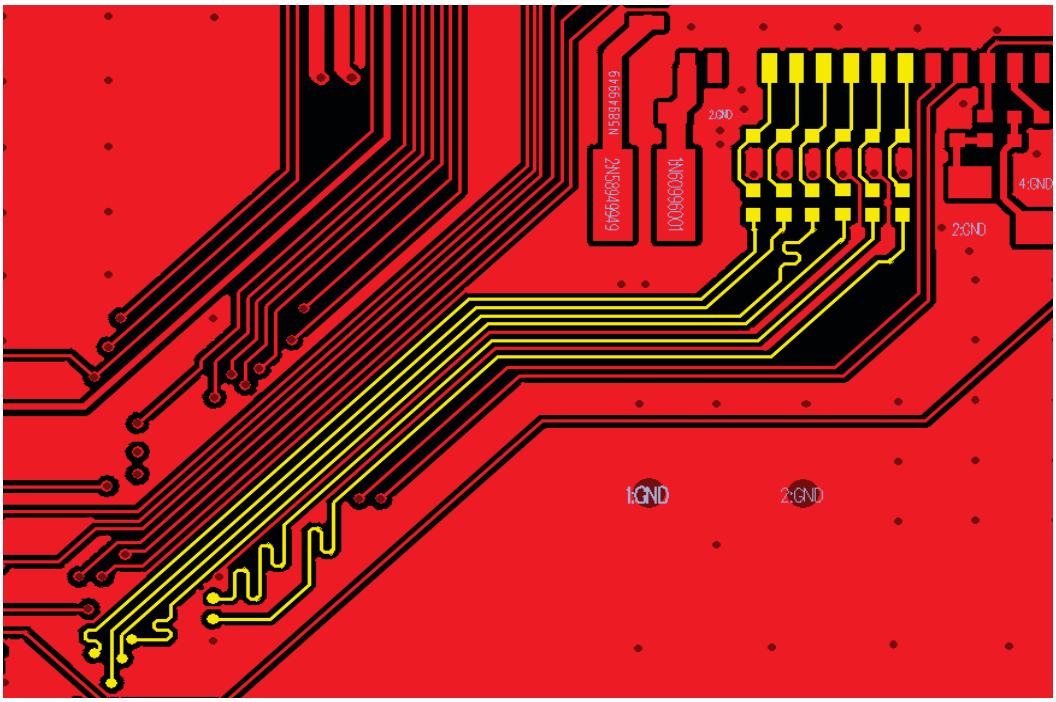


Figure 4-49 WIFI SDIO Layout

The speeds of UART interface can be up to 4Mbps, and so the reference plane of signal traces needs to be contiguous and complete.

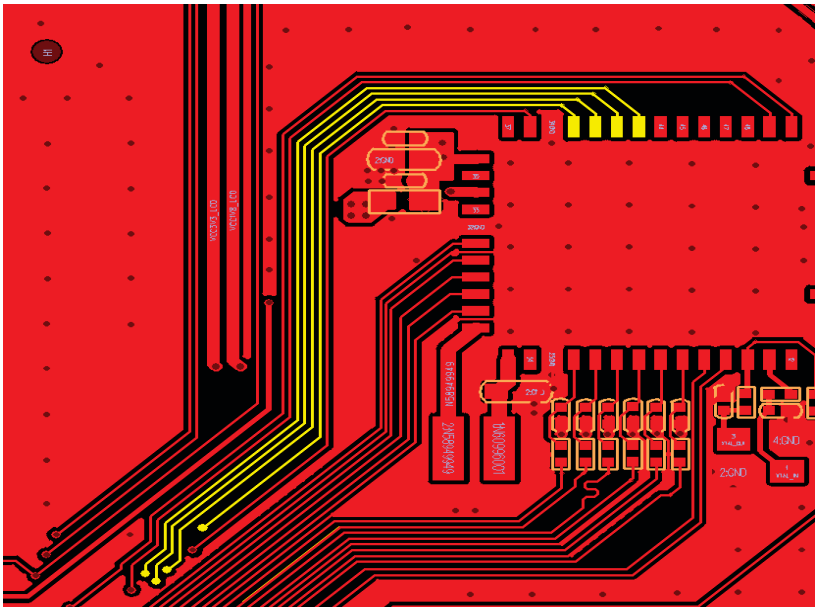


Figure 4-50 BT UART Layout

The reference plane of I2S/PCM needs to be contiguous and complete, the signals should be shielded by GND and avoid being interfered.

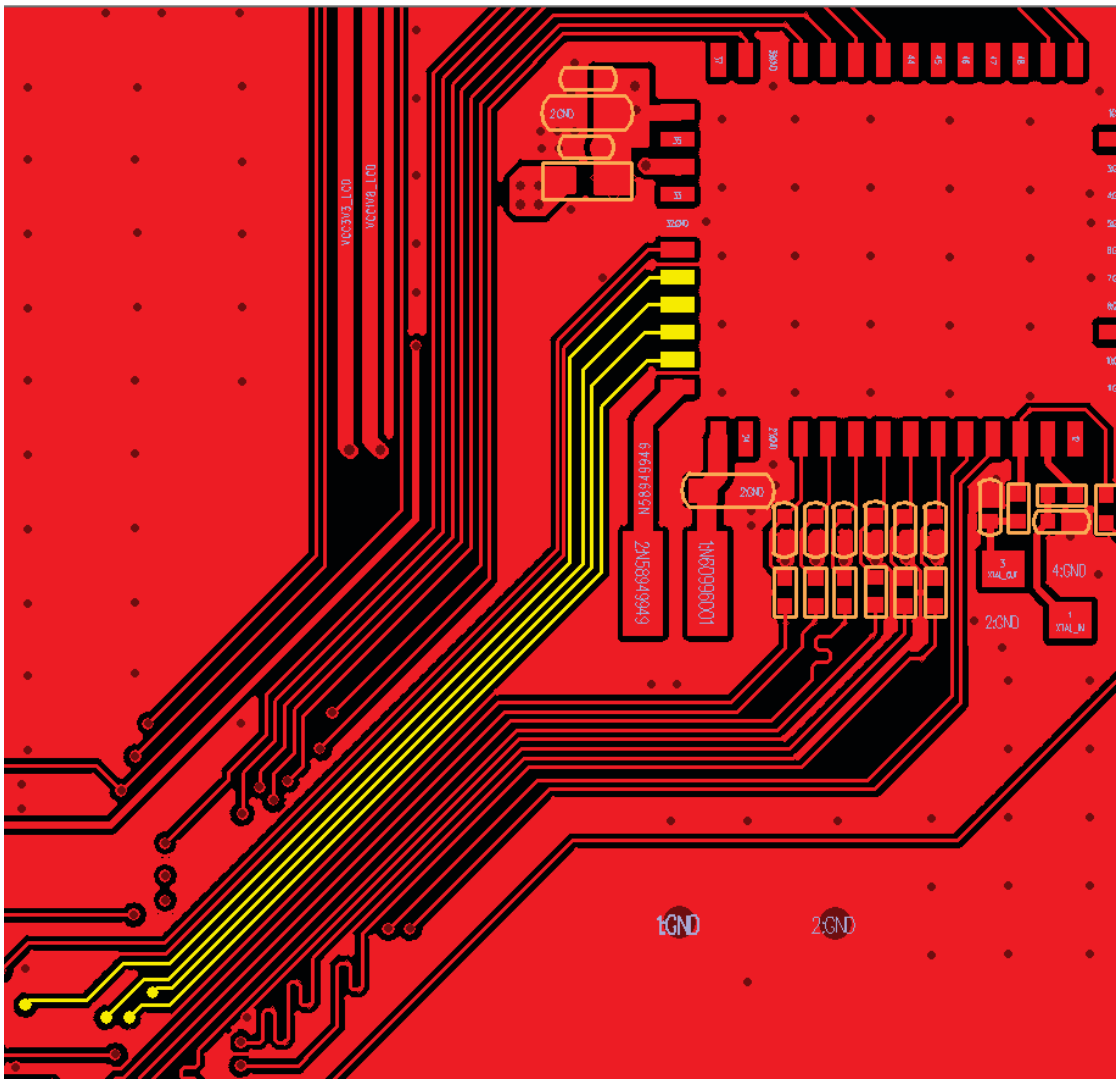


Figure 4-51 BT PCM Layout

If using a 2X2 MIMO antenna interface, the direction of RF traces needs to take into account the position of the two antennas. The position of the two antennas needs to be as far as possible and to consider vertical placement to avoid mutual interference.

The ANT RF traces needs 50 ohm impedance. To reduce interference and reduce trace loss, the adjacent layer of the ANT RF trace needs be keep-out, such as RF traces on the 1th layer, and the 2nd layer is keep-out which reference 3th layer to do impedance design, and the reference layer (keep the same reference plane) needs to be contiguous, can not cross the power and other signal traces, avoid being interfered. The reserved parts need to be added on RF traces for debug matching. As shown in Figure 4-52, the highlighted yellow signal line is the ANT RF trace.

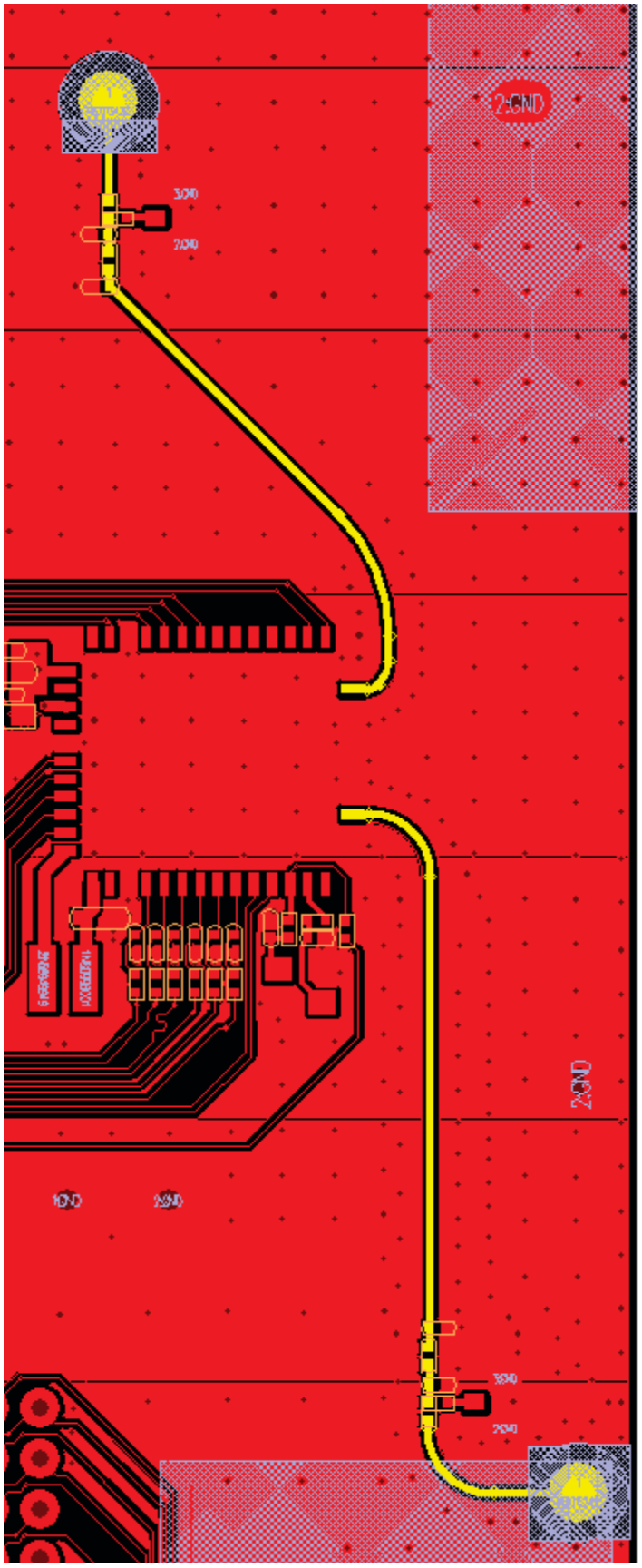


Figure 4-52 RF Traces Layout

4.3.2 Antenna Circuit

- 4.3.2.1 Overview

Due to the rapid development of wireless communication, as the wireless transmission and reception front-end part - antenna, its performance on the entire system communication quality is essential. According to the different use of the platform and different application terminals, its performance and cost control requirements are more and more demanding. Thus, the antenna miniaturization, multi-band and multi-antenna technology have become a hot and difficult PCB design.

- 4.3.2.2 Antenna Type Selection

With the intensification of market competition, integration is the direction of the development of hardware equipment. Antenna is also evolved from external to embedded, according to the actual different application. The following four kind's antenna can be selected.

- On Board Type: PCB etching one molding, limited performance, very low cost, used in Bluetooth, WIFI module integration.
- SMT Package Type: Material with ceramic, metal, PCB, the performance cost is moderate, suitable for large quantities of embedded RF module.
- IPX External Type: The use of PCB or FPC + Cable combination, excellent performance, cost is moderate, widely used in OTT, terminal equipment.
- External Type: Plastic rod antenna, high performance, independence, high cost, used in terminal equipment, without considering the EMC.

- 4.3.2.3 RK Universal Antenna Design

Rockchip had design 4 universal on-board antenna,witch are ANT1227SD, ANT1227SS, ANT2885S, ANT4411D（Shown as Figure 4-48）,suitable for different platforms and terminals. RK universal antennas have good performance and wide applicability; can make a flexible and rapid optimization of the adjustment according to the actual environment of PCB, which will greatly improve the work efficiency.

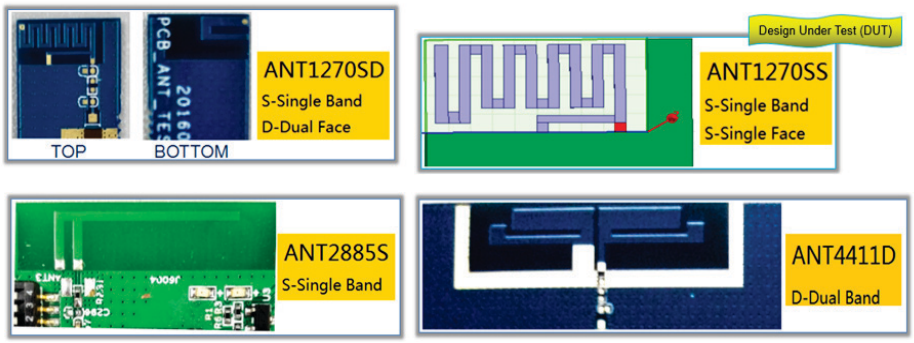


Figure 4-53 RK Universal Antenna

The Layout Engineer can import the package of the selected antenna into the PCB. According to the "Design Guidelines", the engineer can refer to the antenna layout in the PCB. Finally, it is recommended that the designed PCB be sent to the antenna engineer to simulate the performance to optimize the best parameters in the current design.

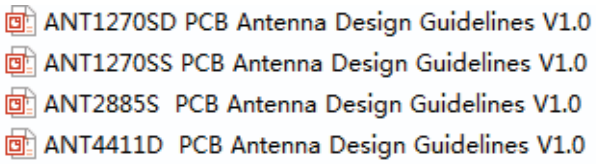


Figure 4-54 RK Universal Antenna design Guidelines

- 4.3.2.4 Antenna Specifications

Table 4-23 BT/WIFI Antenna Specifications

Applicable Standards	BT/IEEE 802.11 b/g/n	IEEE 802.11 a/b/g/n/ac
Frequency Range	2.4 to 2.49 GHz	2.4 to 2.49 GHz, 5.15 to 5.85 GHz
Maximum Gain	3-4dBi	5-6dBi
Antenna Size	10*5.0*1.0-1.6 (mm)	40*9*1.0-1.6 (mm)
Package Size	12*7.0(mm)	44*11(mm)
Antenna Efficiency	50-60%	50-70%
VSWR	2:1	
Input Resistance	50 Ohms	
Temperature	-40° to +75°C	
Humidity	0 to 95%,No crystal dew	

For MIMO antennas, in addition to the need to meet the above performance, a very important indicator is the isolation between two or more antennas (S21 <-10 dB), which is the difficulty of the current miniaturized MIMO antenna design.

In addition, there is an ECC indicator, in the WIFI band if S11 and S21 meet the requirements, generally no problem. However, for more than four antennas need to focus on the layout between the antennas.

4.4 Power Supply Design

4.4.1 RK3399 Power

- 4.4.1.1 GND

There is a need of a complete GND layer adjacent SOC, for cooling and ensuring power integrity.

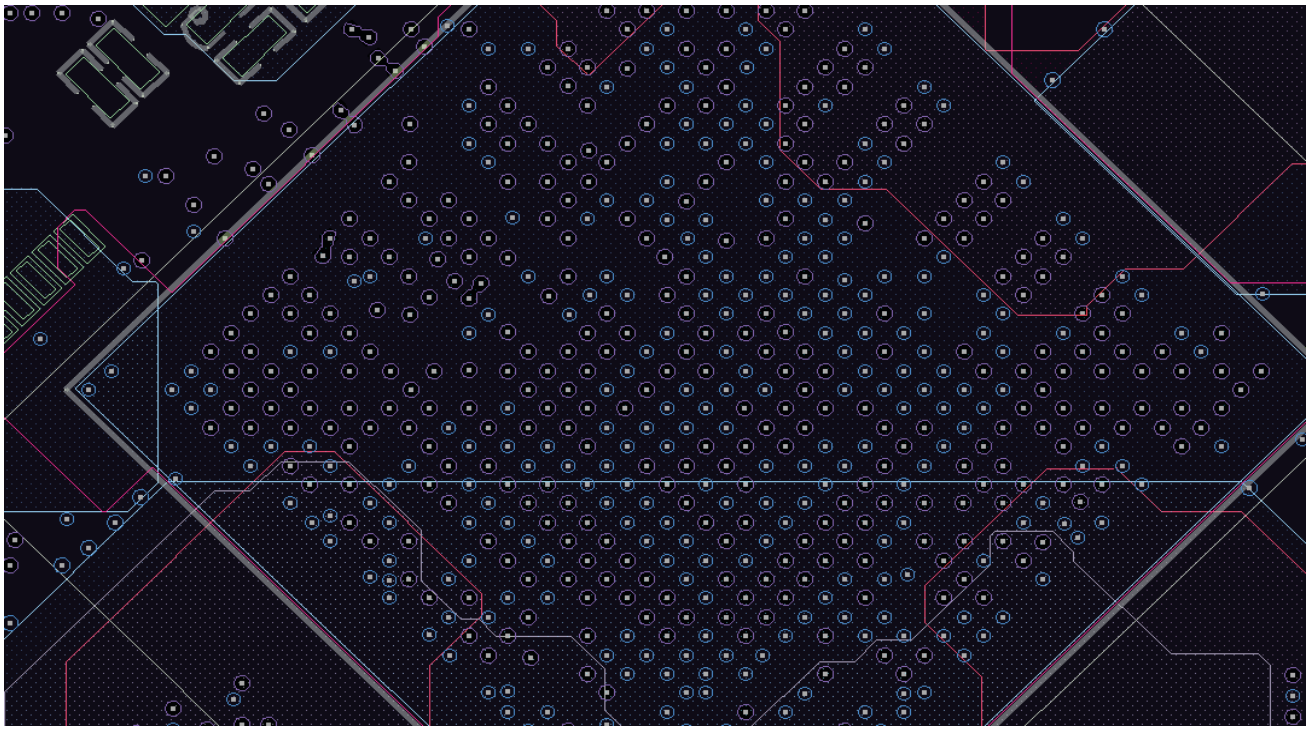


Figure 4-55 Complete GND layer

Every GND pin needs via, shown as Figure 4-51.

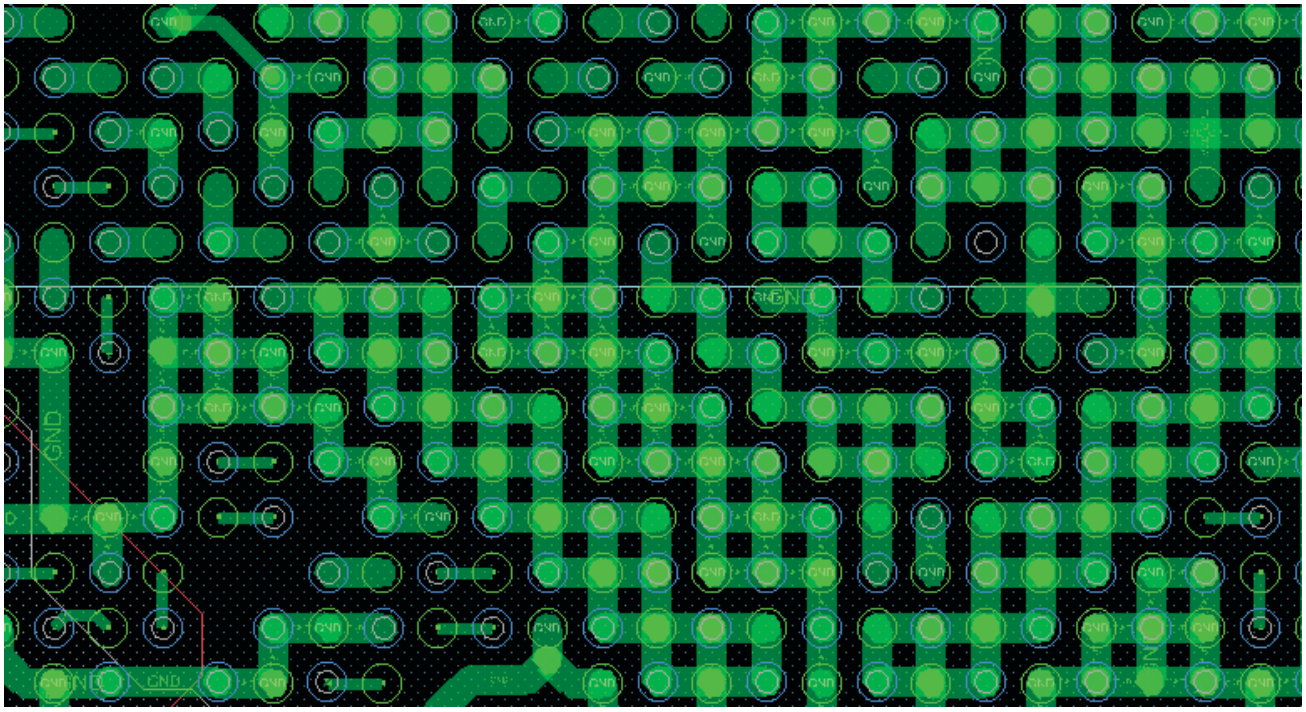


Figure 4-56 GND Via

- 4.4.1.2 SOC Power Supply

The high-current power supply,such as VDD_CPUB, VDD_CPUL, VDD_GPU, VDD_LOG, VDD_CENTER, should to be connected to power pin of SOC use the copper,and should be placed as more vias as possible connected to power pin.

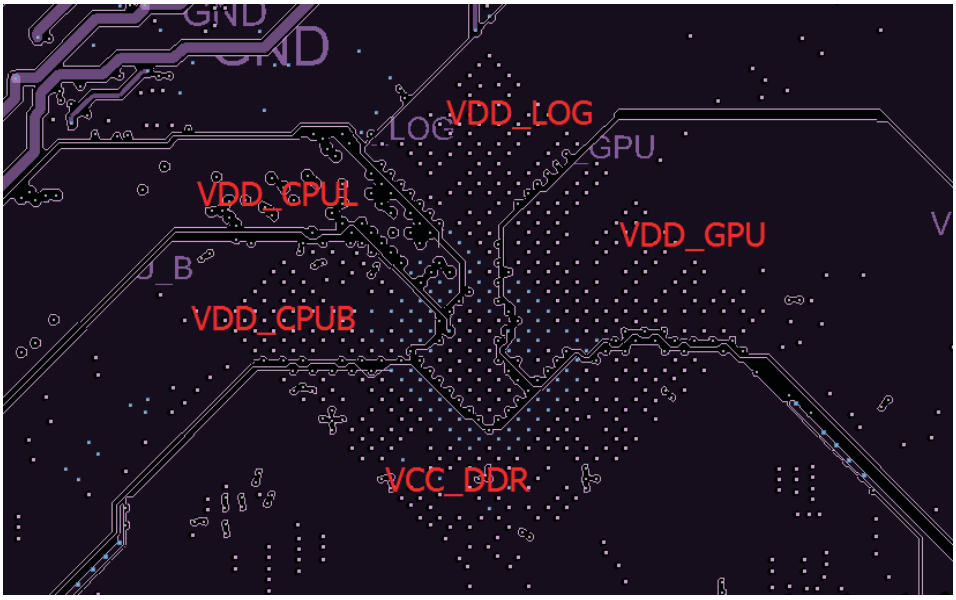


Figure 4-57 SOC Power Supply Copper

It is the best to use double-sided paste structure, even if only place a few 0201 decoupling capacitors can also improve power performance.For the PCB which can only be supplied with single side paste,place the decoupling capacitor as close to the SOC as possible,and place as more vias as possible.

- 4.4.1.3 DDR SDRAM Power Supply

The copper of VCC_DDR is best to be placed under SDRAM, it will be easy to place the decoupling capacitor, while not affecting the signal traces.

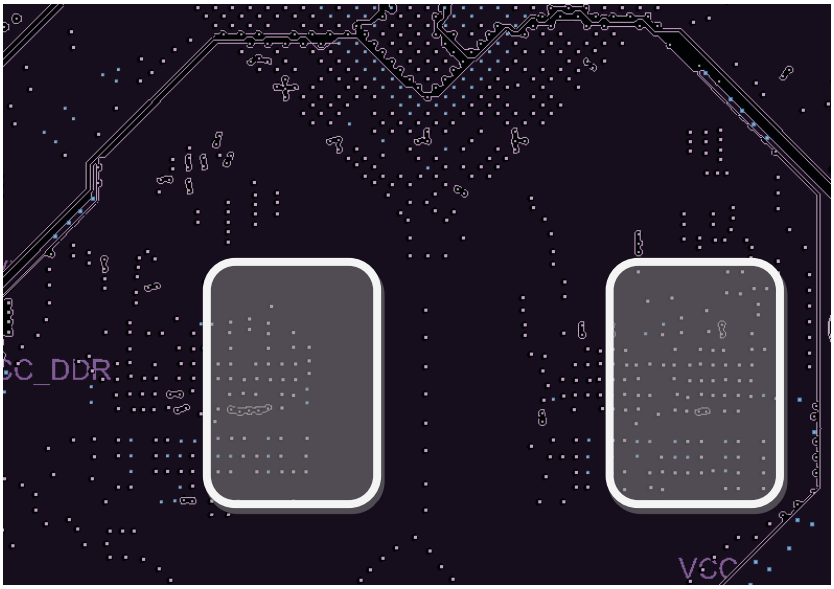


Figure 4-58 Reference Plane for DDR

- 4.4.1.4 Lower-current Power Supply

Little package decoupling capacitor should be placed close to power pin.Shown as Figure 4-59.

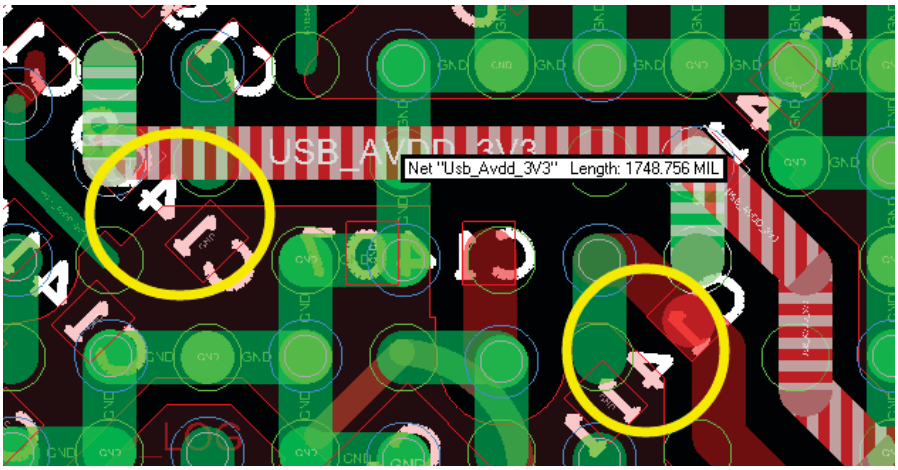


Figure 4-59 Decoupling Capacitor

4.4.2 PMIC

- Should place as more vias as possible on EPAD, it is recommended to use 4*4 0.8/0.5mm or 5*5 0.5/0.3mm or 6*6 0.4/0.2mm vias.

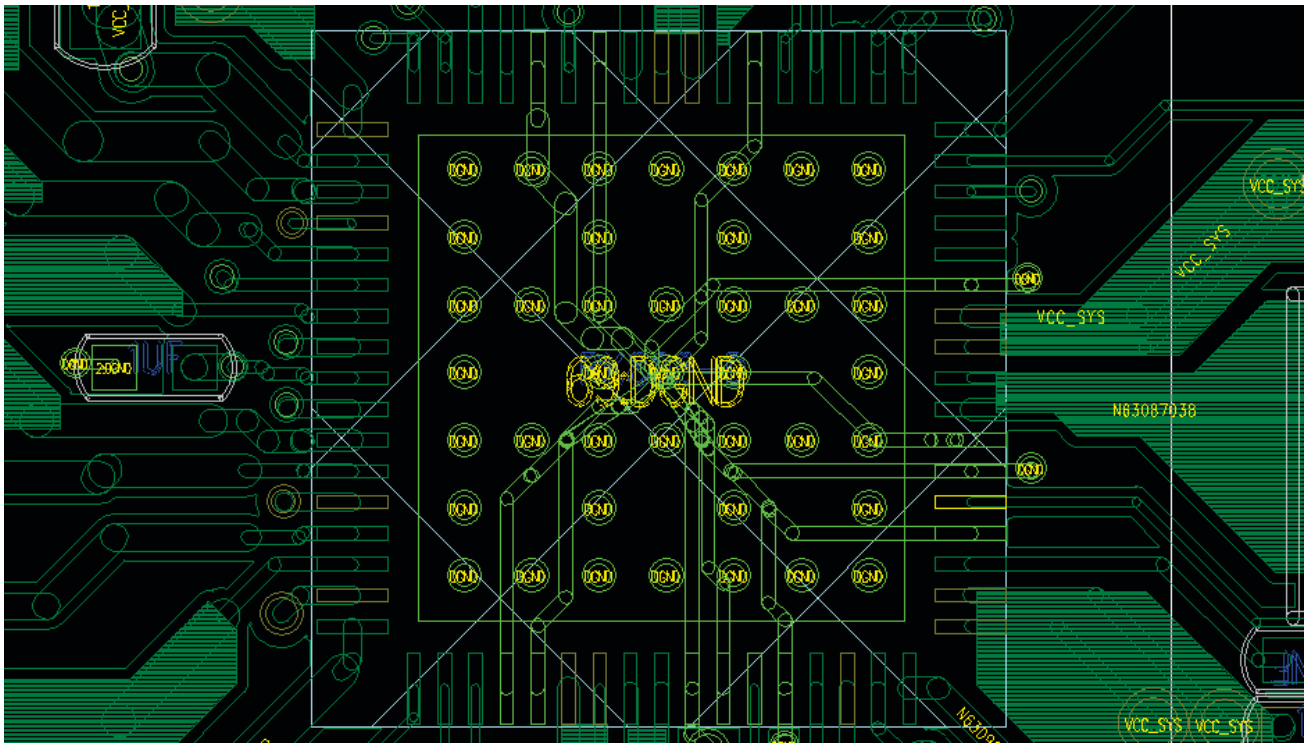


Figure 4-60 PMIC EPAD Vias

- DC-DC input and output：The input capacitor of VCC needs to be placed close to power input pin,the output capacitor close to inductor.The capacitor should have enough vias to ensure the low ESR,and the decoupling effect can be ensured.In particular,the negative end of the capacitor is easy to be ignored by the layout engineer.

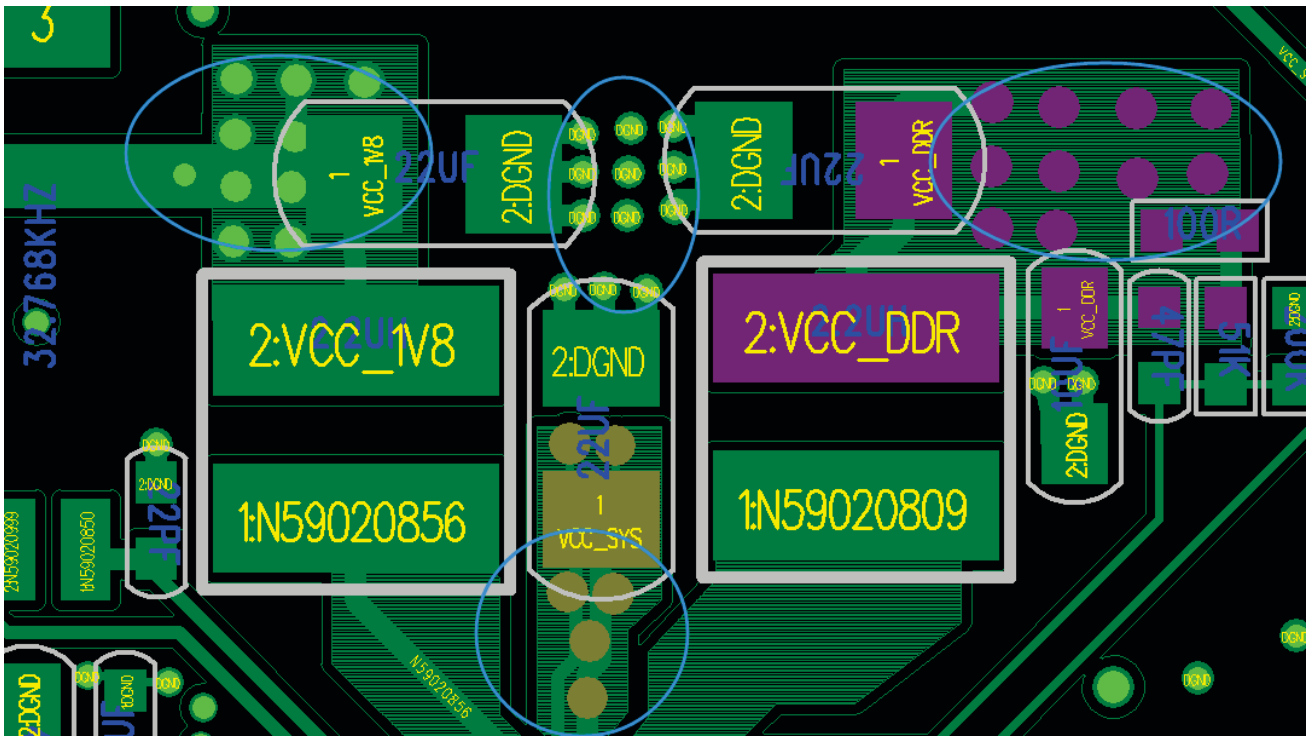


Figure 4-61 DC-DC Decoupling Capacitor Vias

- The 32.768 crystal traces need to be shielded by GND traces, avoid being disturbed.

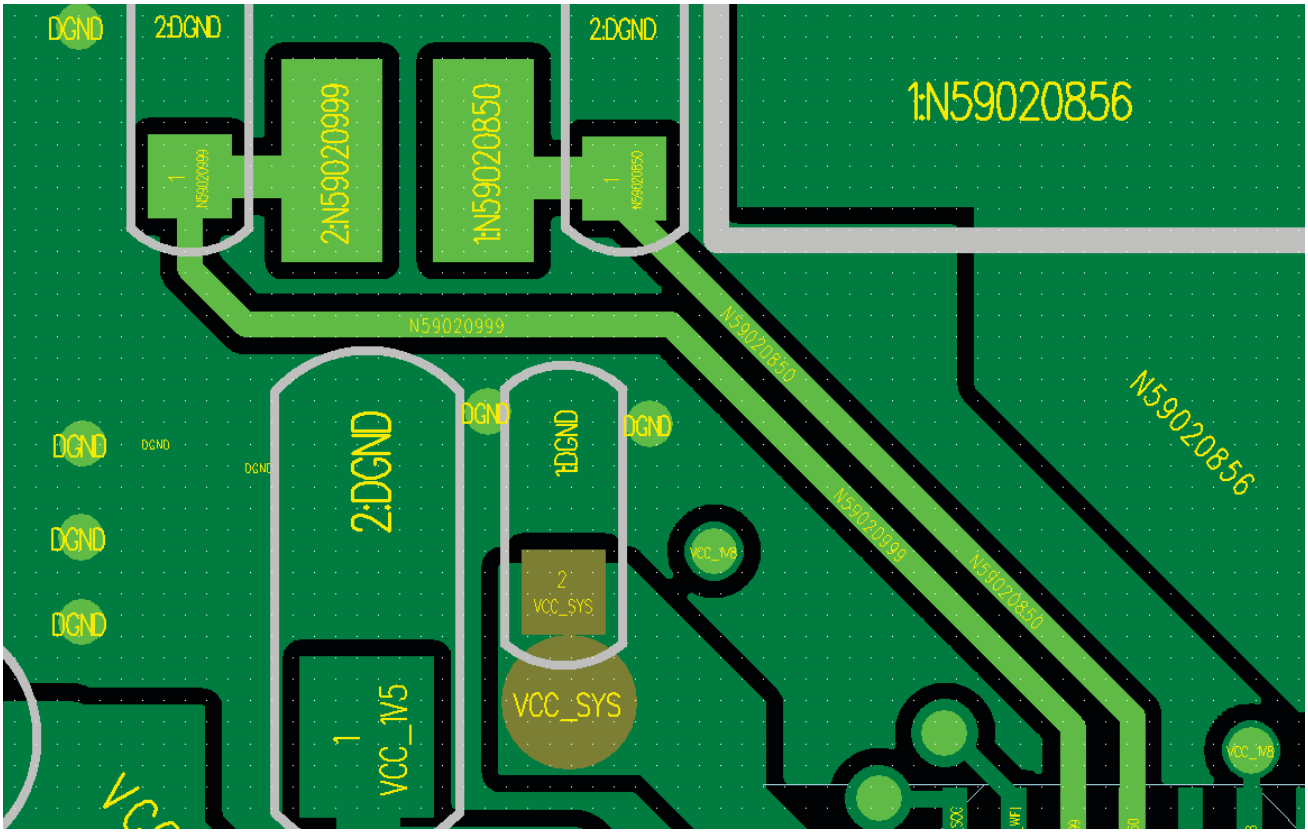


Figure 4-62 RTC Traces

- The distance between two adjacent inductors should be more than 2mm, to avoid the mutual inductance (especially boost and charge inductance of RK818-3).

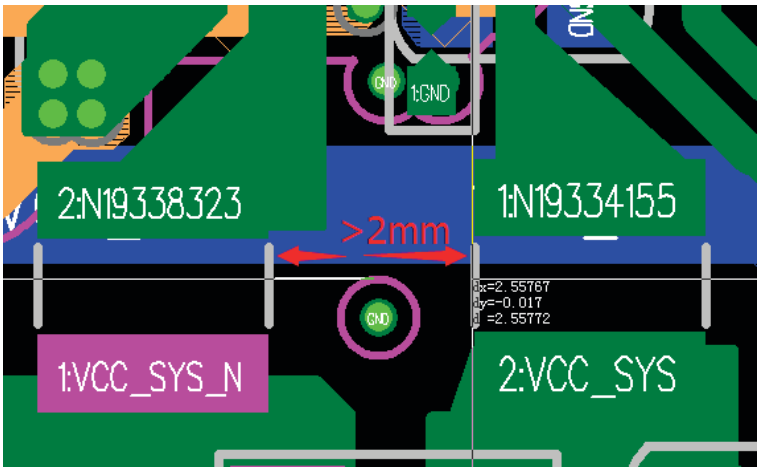


Figure 4-63 DC-DC Inductors Layout

- The traces width of LDO should be designed according to the load current, the decoupling capacitor should be placed close to PMIC.

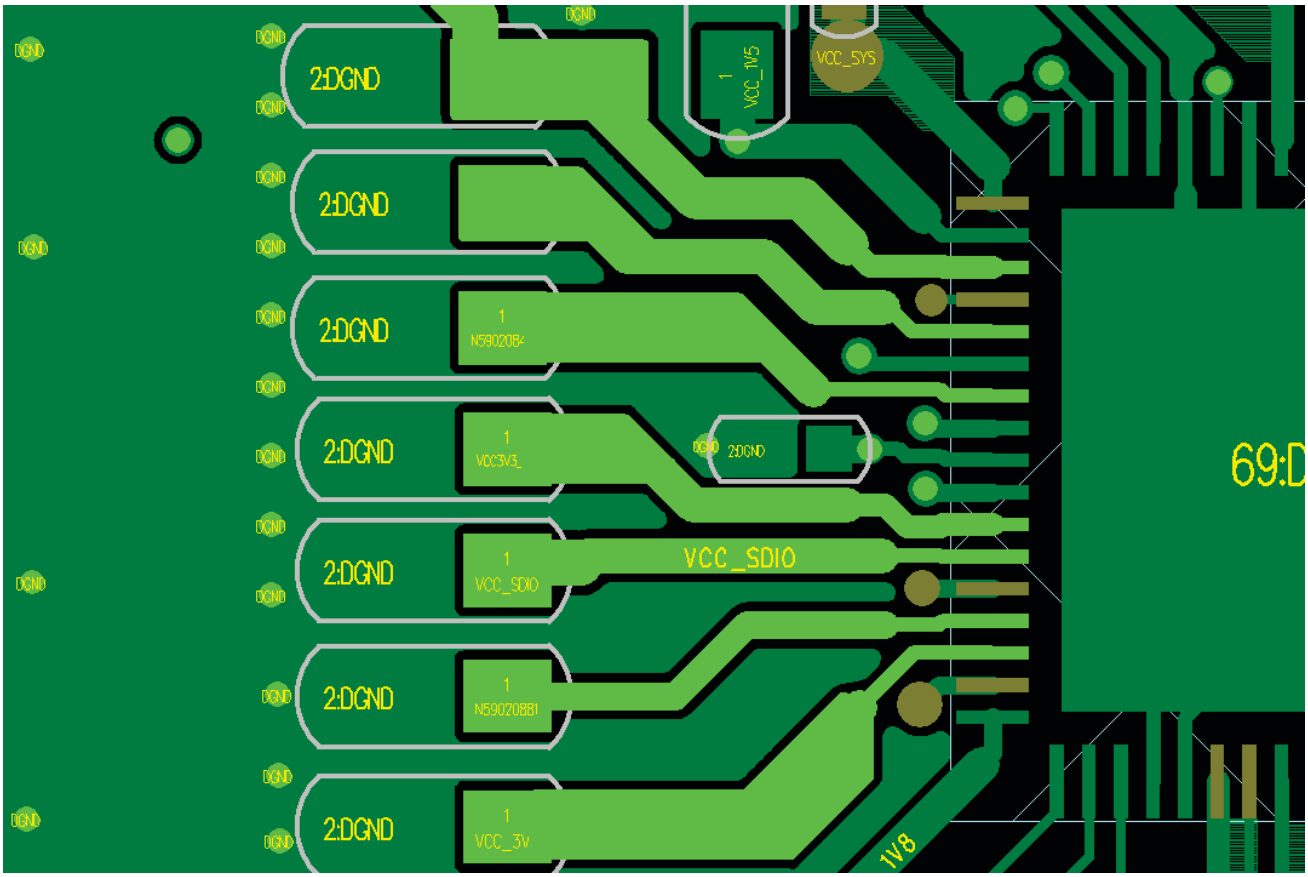


Figure 4-64 LDO Layout

- The 10mR current sampling resistor of RK818-3 should be placed close to battery connector. The SNSN / SNSP signals should be routed according to differential pair's rules, no impedance requirements. It is important to note that since the SNSN is a negative side of the 10mR resistor, the 0R resistor connected to the SNSN can not be directly connected to another GND and grounded via the ground end of the 10mR resistor (Shown as Figure 4-60).

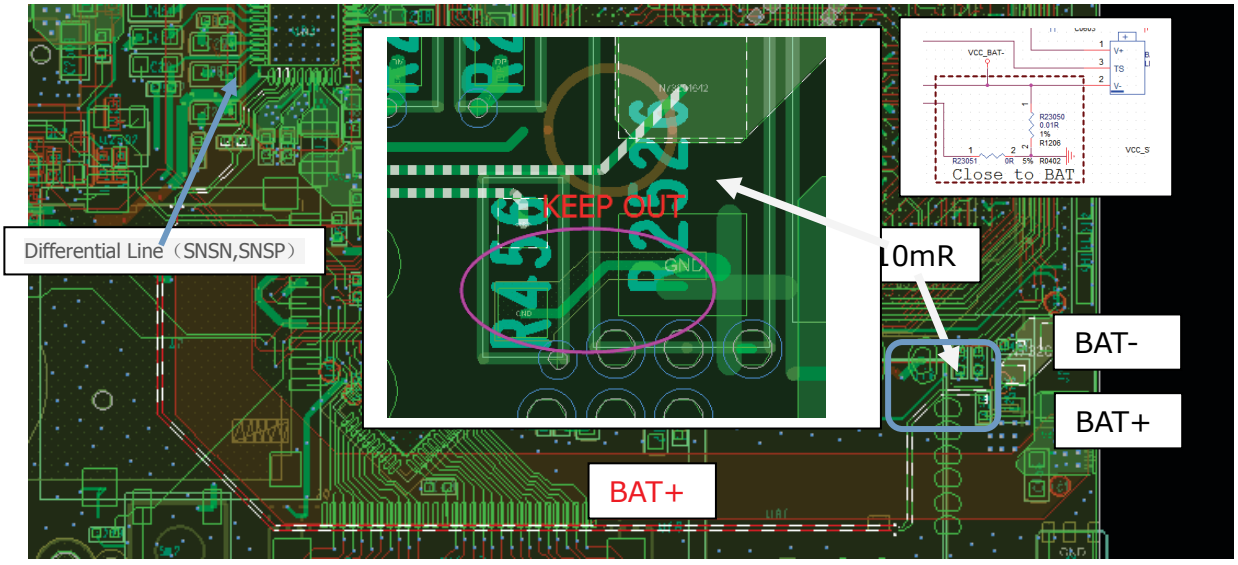


Figure 4-65 RK818-3 Current Sampling Resistor Layout

- The traces of VBAT+ and VCC_SYS need to be considered 3-5 A load-current capability, could not have too much voltage drop, so the power vias need enough large aperture and enough more quantity. The Q23008 in Figure 4-66 is also used to reduce the internal power-path impedance of RK818-3, which can make the main power circuit impedance smaller, give full play to the battery performance.

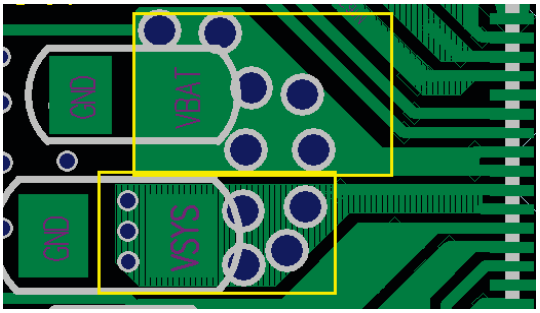


Figure 4-66 VBAT Power Vias

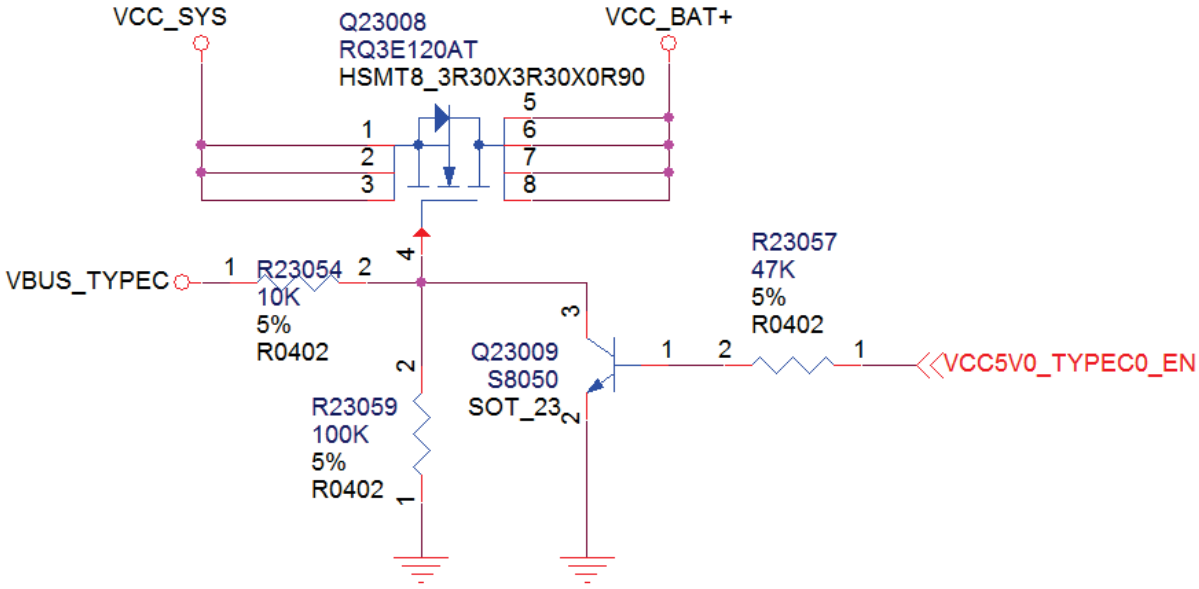


Figure 4-67 VBAT Power-path

4.4.3 DC-DC

The peak current of RK3399`s BigCPU/GPU is around up to 4.3A. To reduce the power ripple, it should be placed as more vias as possible next to the input and output capacitors. It is recommended to place more than15pcs 0.2mm vias (especially the negative capacitance of the capacitor also need to pass the corresponding via, which is easily ignored), it is recommended to use SYR837 / SYR838 buck IC, it is WLCSP package and the size is relatively smaller. The copper needs to be keepout under the buck IC in order to improve the welding yield and then use thick copper mesh to connect to buck IC pins (similar to thermal pad connection).

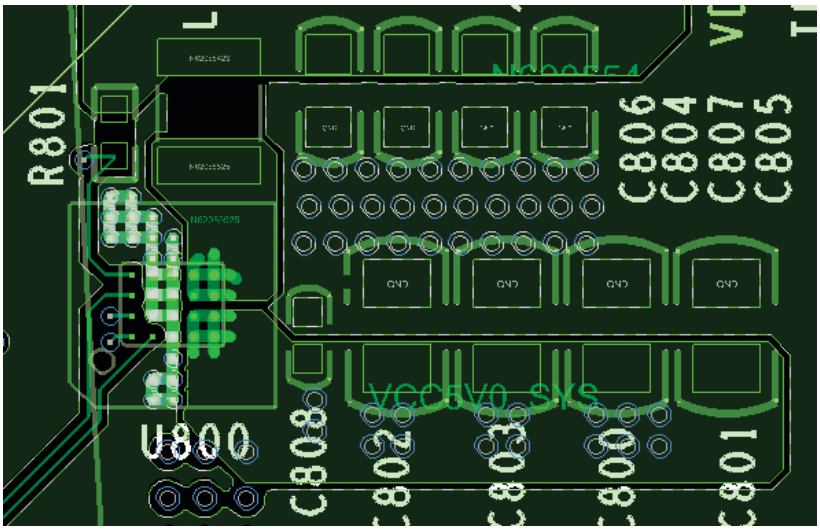


Figure 4-68 RK3399 High-current Vias Layout

4.4.4 Charging Management

- 4.4.4.1 RK818-3 Charging Path
- RK818-3 charging path shown as below.RK818-3 supports maximum 5V/3A charge current, should note the trace widths and via numbers in layout.

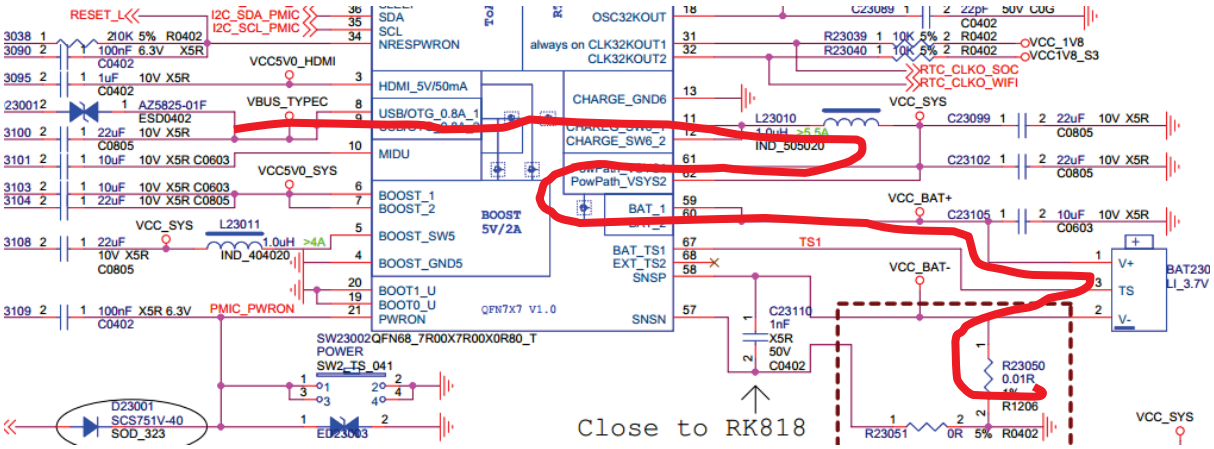


Figure 4-69 RK818-3 Charging Path

- 4.4.4.2 RK808-D Charging Circuit

In RK808-D power solution, it uses BQ25700 charge IC with power- path management, which supports multi-cell battery charging.The input voltage is 5V-20V, and supports reverse discharge, which meet with the TYPE-C PD standard.

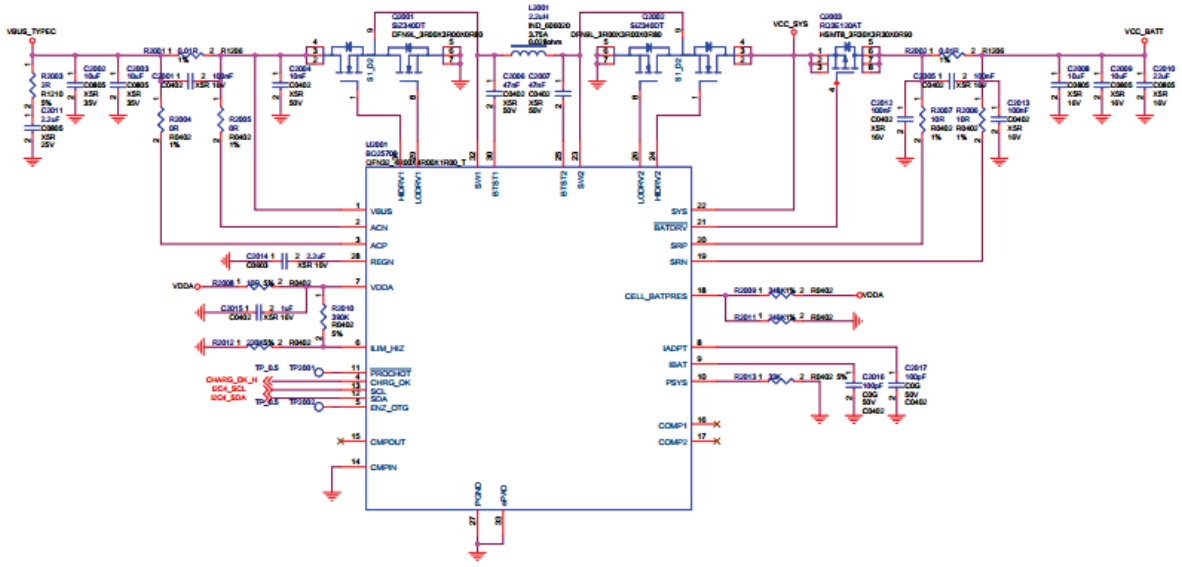


Figure 4-70 RK808-D Charging Solution

The ACN/ACP and SRP/SRN current sampling signal must be connected to the respective 0.01ohm sampling resistor according to the differential pairs rule,no impedance requirements.But they must be placed close to the resistor pads to ensure the sampling accuracy.It is necessary to increase vias number near the GND pin of NMOS to improve the DC-DC conversion efficiency.

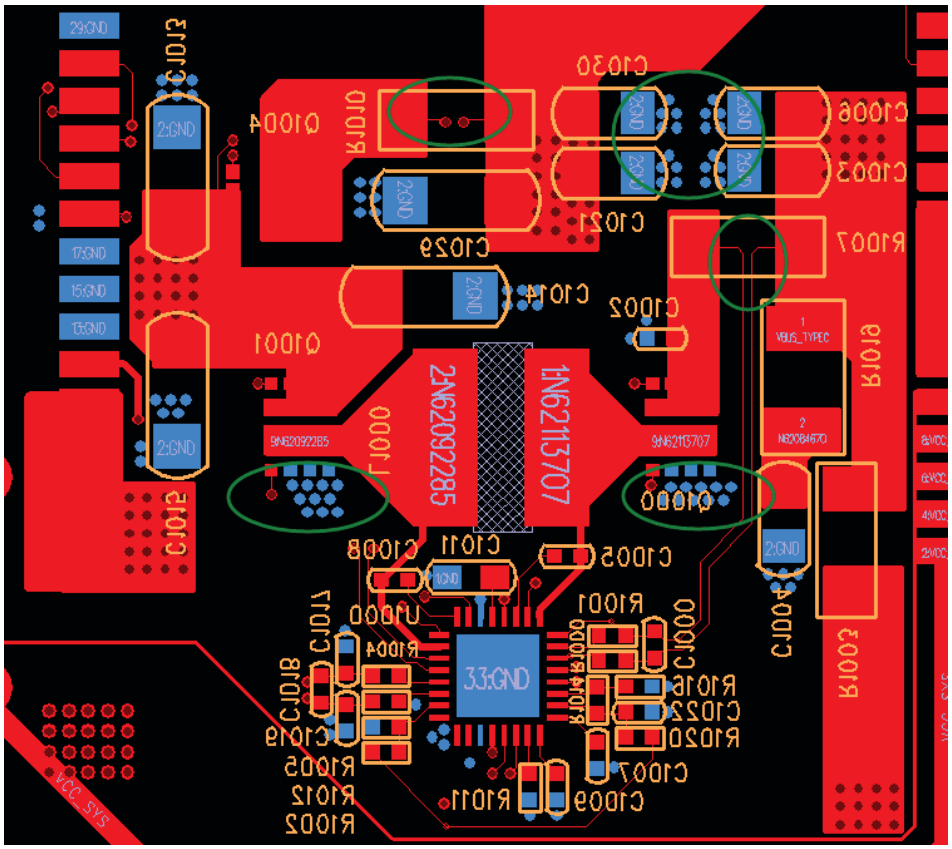


Figure 4-71 RK808-D Charging Circuit Layout

4.4.5 Remote Feedback Compensation Design

The DCDC may be placed for some distance away from RK3399, so it usually uses far end sampling voltage to compensate for traces loss. It generally the current is greater than 1A will use this method, such as VDD_GPU, VDD_CPU_B, VDD_CPU_L, VDD_CENTER and so on.

As shown in Figure 4-72 and Figure 4-73.The VDD_CPU_L of VFB2 should feedback from near RK3399, and use the accompanying traces.

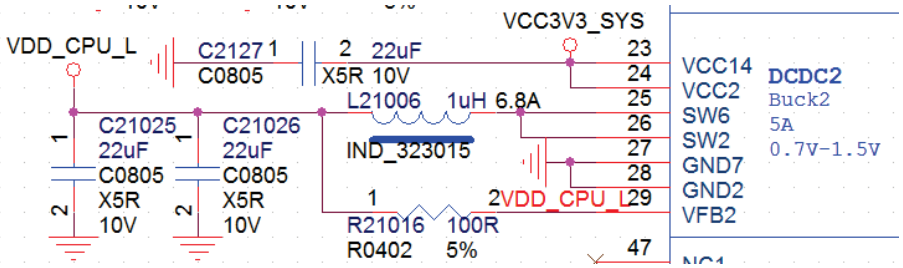


Figure 4-72 PMIC Feedback Design

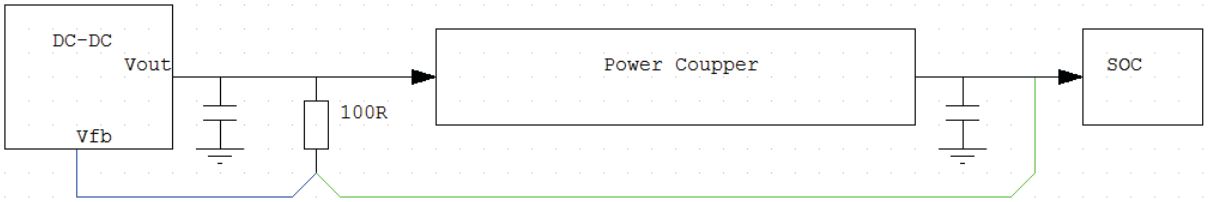


Figure 4-73 DC-DC Feedback Design

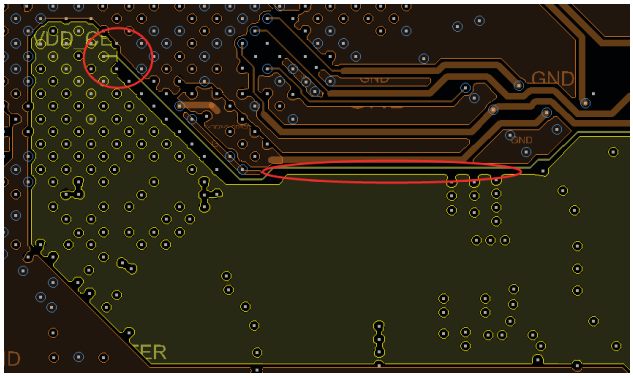


Figure 4-74 PMIC Feedback Traces

Chapter5 Thermal Design

5.1 Thermal Simulation

In this report, we present the thermal characteristic for RK3399 828-pin EHS-FCBGA mounted on 8 PCB and JEDEC PCB using the Finite Element Modeling (FEM) method. The report is based on the JEDEC JESD51-2 standard; the system design and environment for the application may be different from the JEDEC JESD51-2 standard and need to be analyzed according to the application conditions.

Notes:

Thermal resistance is the reference value of the PCB without the heat sink, the specific temperature is related to the board design, size, thickness, material and other physical factors.

5.1.1 Result Summaries

Thermal simulation report shown as Table 5-1; it could be easy to get conclusion that EVB thermal resistance coefficient is better than JEDEC.

Table 5-1 RK3399 Thermal Simulation Report

Package (EHS-FCBGA)	Power(W)	$\theta_{JA}(℃/W)$	$\theta_{JB}(℃/W)$	$\theta_{JC}(℃/W)$
JEDEC PCB	6.25	11.9	7.5	0.38
EVB PCB	6.25	9.8	5.3	0.38

5.1.2 PCB Description

The PCB description for thermal simulation is shown as Table 5-2.

Table 5-2 RK3399 PCB Description

JEDEC PCB	PCB Dimension（L x W）	101.6 x 114.3 mm
	PCB Thickness	1.6mm
	Number of Cu Layer	8-layers L1/L6-0.045mm，L2~L5-0.035mm
EVB PCB	PCB Dimension（L x W）	130 x 115mm
	PCB Thickness	1.6mm
	Number of Cu Layer	8-layers L1/L6-0.030mm，L2~L5-0.017mm

5.1.3 Terminology

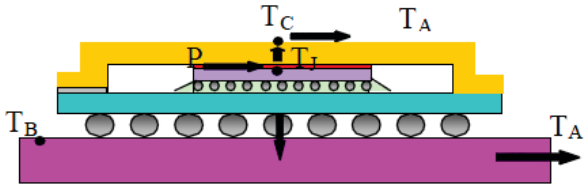
The terminology in this chapter is explained as following:

- TJ: The maximum junction temperature
- TA: The ambient or environment temperature
- TC: The maximum compound surface temperature
- TB: The maximum surface temperature of PCB bottom
- P: Total power input

The thermal parameter can be define as following

1. *Junction to ambient thermal resistance,* θ_{JA}**, defined as:**

$$\theta_{JA} = \frac{T_J - T_A}{P} \quad ; \qquad (1)$$

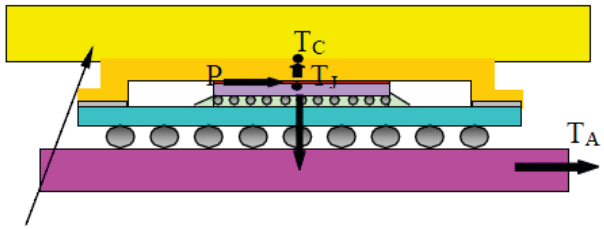


Thermal Dissipation of EHS-FCBGA

Figure 5-1 θJA

2. *Junction to case thermal resistance,* θ_{JC}**, defined as:**

$$\theta_{JC} = \frac{T_J - T_C}{P} \quad ; \qquad (2)$$

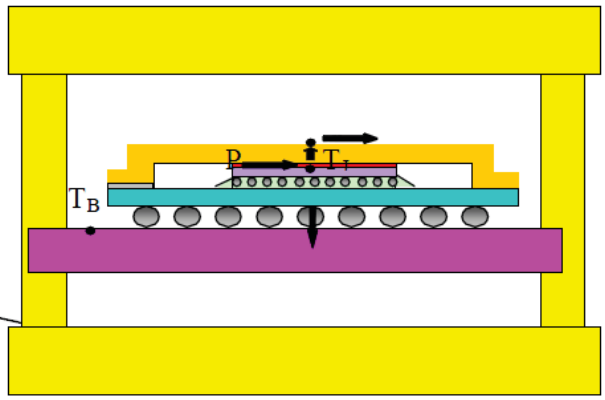


Attach a block with constant temperature onto package.

Figure 5-2 θJC

3. *Junction to board thermal resistance,* θ_{JB}**, defined as:**

$$\theta_{JB} = \frac{T_J - T_B}{P} \quad ; \qquad (3)$$



Attach a block with constant temperature

Figure 5-3 Θjb

5.2 Universal Heat Dissipation Method

RK3399 maximum power will reach 6.5W, the good heat dissipation on the RK3399 product is particularly important for performance improvement, system stability and product safety.

5.2.1 Common Way of Heat Dissipation

As we all know, any place where the temperature difference exist, there will be heat transfer, the heat will be transferred from the high temperature part to the low temperature part until reach the same temperature. The conduction process of heat can be divided into steady-state process (the temperature does not change with time) and unsteady process (the temperature changes with time). The heat conduction is common in the following three ways.

- 5.2.1.1 Conduction

  There is no relative displacement between the parts of the object, relying micro-particles thermal movement to generate the heat conduction, such as molecules, atoms, free atoms and so on. Such as the movement of the heat inside the object from the high temperature part to the low temperature part.

- 5.2.1.2 Convection

  Fluid (including the liquid and the gas) is in the process of flowing, the phenomenon of heat conduction which from the higher temperature to the lower temperature. Convection is divided into forced convection and free convection. The former is the movement of the fluid in the external power driven, such as pump, fan, pressure and so on; the latter is the movement of the fluid under the action of buoyancy, due to the inhomogeneity of the density induced by the uneven temperature distribution.

- 5.2.1.3 Radiation

  Objects via electromagnetic waves to conduct energy, do not need the material as a medium.

5.2.2 System Common Heat Dissipation Method

Common heat dissipation methods are active cooling and passive cooling two ways.

Active Cooling: that is, use the external equipment to force cooling the heat away from the heat sink away, such as fans, etc.; its advantages are high cooling efficiency, small size; the disadvantage is the introduction of noise and power consumption. This method is generally used for the relatively large heat generated by the device, such as PC.

Passive Cooling: That is, via the heat sink to increase the surface area of the CPU, to speed up the heat transfer and convection; from the cooling effect point of view, the passive cooling is not better than the active cooling. But In the case of heat is not great, basically can take this way of cooling, the advantage is low cost, reduce noise, no power supply, energy conservation.

5.2.3 Heat Dissipation Design

In RK3399 products, RK3399 is the part which generates largest heat, all heat dissipation methods is mainly for the chip. In addition to RK3399, the other major heat sources are: PMIC, charging IC, backlight IC and inductance. Please note that the heat source should be placed disperse, do not pile up together.

The high-current power supply traces (such as DC input traces, the battery to the PMU power traces) also affect the whole product heat; the power trace should be as short and wide as possible.

For the shell product which both ends are plastic and middle is metal, please note that the main heat source must be placed in the bottom of the shell metal part in layout, away from the RF and GPS modules.

- 5.2.3.1 PCB Heat Dissipation

  The following three ways to enhance heat dissipation:
  - Place vias on PAD of heating parts.
  - Has a continuous copper on the PCB surface.
  - Increase the copper thickness.

- 5.2.3.2 Structural Heat Dissipation

  Structural thermal dissipation can be used for actively cooling, that is, add the heat sink. According to the heat radiation diffusion characteristics, CPU use the heat sink, the best way is heat source as the center, the use of square or circular heat sink, make sure to avoid the long strip of heat sink.

  Commonly used heat sink:

- According to the material distinguish: Aluminum alloy, copper alloy, aluminum-copper alloy, thermal grease, graphite, nano-carbon, ceramics and so on.
- According to the process distinguish: aluminum extrusion process, casting process, mechanical pressing process, cutting process.

The thermal conductivity of each material is different, current commonly used the cooling material is generally copper and aluminum alloy; copper heat dissipation is good, but the price is more expensive, pure aluminum is too soft, can not be used directly, so generally use aluminum alloy, Low price, light weight, but the thermal conductivity is much worse than the copper; based on low cost to consider the selection of aluminum alloy material heat sink. Refer to the following recommendations for the selection of the heat sink process type:

- Extruded fins are better than cast aluminum fins. Cast aluminum heat sinks in the proportion of aluminum metal 25-30%, the other for the carbon and other metals alloy. The proportion of metal aluminum in the extruded heat sink is 70% to 80%, and the other is alloy of carbon and other metals. So aluminum extrusion heat sink high purity, thermal conductivity, density, low price.
- In natural cooling conditions, the black aluminum heat sink cooling effect is 3 to 8% better than the silver-white; this is because the black heat radiation effect is stronger than the white.
- The surface treatment of the heat sink has electrophoretic paint or black oxygen polarization treatment, the purpose is to improve the cooling efficiency and insulation properties. In the natural cooling can be increased by 10-15%, in the ventilation cooling can be increased by 3%, electrophoretic paint can withstand pressure 500-800V.
- Heat sink manufacturers will give different types of heat sink thermal resistance or give the relevant curve, and given different heat dissipate condition with different thermal resistance.

5.2.4 Heat Sink Size Calculation

The structure of aluminum extrusion heat sink is shown as Figure 5-4.

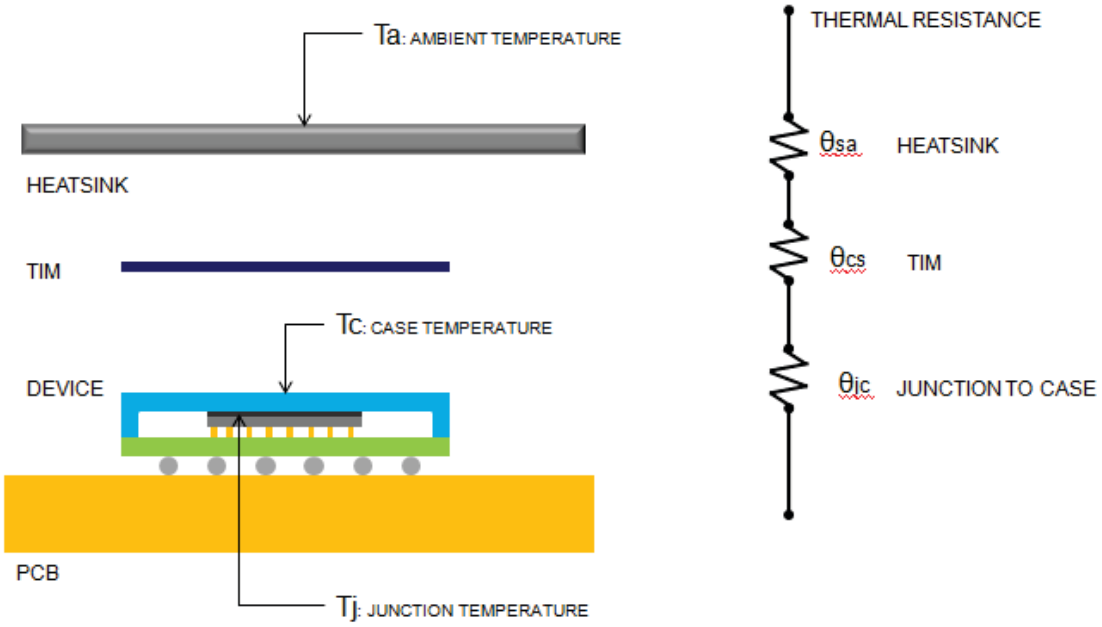


Figure 5-4 Heatsink Structure

Formula 1:

R= 1/hA

Variable descriptions:

A：Heatsink area

h：Heat conduction coefficient (related with the heat sink material, thickness, density, temperature, wind speed and other parameters)

From the above formula, the larger the heat sink area is, the smaller the thermal resistance is, and the following empirical data are obtained:

2mm thickness of aluminum heat sink, surface area (square centimeters) and thermal resistance (℃ / W) of the corresponding relationship is as follows:

- 500 cm^2 correspond to 2.0℃/W
- 250 cm^2 correspond to 2.9℃/W
- 100 cm^2 correspond to 4.0℃/W
- 50 cm^2 correspond to 5.2℃/W
- 25 cm^2 correspond to 6.5℃/W

Formula 2:

Q=Tj-Ta/（θsa+θcs+θjc）

According to the formula 2 can be deduced the chip heat sink required thermal resistance formula 3:

θsa=(Tj-Ta)/Q-(θcs+θjc)

Variable descriptions:

Tj：Maximum working junction temperature（125℃）

Ta：Maximum working ambient temperature（55℃）

Q：RK3399 power consumption（6.5W）

θsa：Heat sink thermal resistance (need to consider the ambient wind speed)

θcs：Thermal resistance of the thermally conductive medium TIM (thermal interface material) (0.11 ° C / W, κ = 2 W / mC 100 μm thickness)

θjc：SOC package thermal resistance (8 layers JEDEC PCB board 0.38 ℃ / W)

The above formula 3 to get the heat sink thermal resistance requirements, and then compare the thermal resistance data of the heat sink, you can get the required heat sink heat dissipation area.

For example: in the ambient temperature of 55 ℃, the product temperature rise 15 ℃, use a thermal resistance of 0.11 ℃ / W thermal adhesive, the heat sink size which is wanted, available from the formula 3:

θsa =(125-55-15）/ 6.5-(0.38+0.11)=7.8(℃/W)

The results: It needs to choose more than 25 cm^2 cooling area of heat sink to meet the conditions.

Notes:

The above is the ideal calculation, the actual situation in accordance to the use environment, the coverage of thermal paste, etc., the results will be different.Different heat sink type area and thermal resistance of the corresponding relationship will be very different, need to consult the corresponding heat sink manufacturers.

5.3 System Temperature Control

5.3.1 Temperature Control Strategy

In the Linux kernel, the definition of a set of temperature control framework linux Generic Thermal System Drivers, it can control the temperature of the system through different strategies, current commonly used in are the following three strategies:

- Power-allocator: Introduce PID (proportional - integral - derivative) control, according to the current temperature, dynamically assigned to the module power, and power converted to frequency, so as to achieve the effect of limiting the frequency according to the temperature.
- Step-wise: According to the current temperature, step by step to limit the frequency
- Userspace：Do not limit the frequency.

RK3399 built-in T-sensor to detect the chip temperature, the default use of Power-allocator strategy, the working state of the following circumstances:

- When the temperature exceeds the set value:
  - The temperature trend rises, then to set down frequency.
  - The temperature trend drops, then to rise up frequency.
- When the temperature drops to the set value:
  - The temperature trend rises and the frequency does not change.
  - The temperature trend drops and then to rise up frequency.
- When the frequency rises to the highest, the temperature is below the set value, CPU frequency is no longer limited by thermal control, and CPU frequency enters the system load frequency modulation.
- When the frequency is down, the chip is still over-temperature (such as poor heat dissipation) more than 95 degrees then the software will trigger a restart; when can not restart due to deadlock or other cause,leading to the chip temperature more than 100 ℃, it will trigger the chip internal OTP_OUT signal to PMIC direct shutdown. Refer to Section 3.2.5.1 for specific actions.
-

Notes:

The temperature trend is obtained by comparing the two temperatures which collected the before and the next. When the device temperature does not exceed the threshold, the temperature is collected every l seconds; when the device temperature exceeds the threshold, the temperature is collected every 20ms and limit the frequency.

5.3.2 Temperature Control Configure

RK3399 SDK can respectively provide temperature control strategy for Little-CPU A53, Big-CPU A72 and GPU, the specific configuration, please refer to our "Rockchip Thermal Development Guide”.

Chapter6 ESD/EMI Protection Design

6.1 Overview

The chapter gives recommendations for ESD / EMI protection design in the RK3399 product design to help customers improve the antistatic and electromagnetic interference levels of their products.

6.2 Terminology

The terminology in this chapter is explained as follows:

- ESD:Electro-Static discharge
- EMI:Electromagnetic Interference

6.3 ESD Protection

- To ensure a reasonable mold design; port and connector parts need to be reserved ESD devices.
- In the PCB layout should do a good job in the protection of sensitive parts, isolation.
- In PCB layout try to place RK3399 and the core components on the middle of the PCB, if it can not be placed in the middle of the PCB ,need to ensure that the shield is away from the PCB edge at least 2MM above, and to ensure that the shield can be reliably grounded.
- It should be layout according to the function module and the signal flow, the sensitive part should be independent, the parts which are easy to be interfered should be isolated.
- A reasonable placement of ESD parts is required, the general requirements is placed on the source, that is, ESD devices placed in the interface or the electrostatic discharge position.
- The parts need to be placed away from the edge of the PCB and a certain distance from the connector.
- The PCB surface must have a good GND loop; the connector in the surface must have a better GND connection loop. The shield should be connected with the surface GND, and in the position of the shield cover welding need to added more vias to GND. To do this, there is no any traces can be placed in the surface, and do not appear the copper trace cut off a wide range.
- The PCB surface edge should has a GND ring.
- When it is necessary, do a good isolation between the signal and the ground.
- More exposed copper, in order to strengthen the electrostatic discharge effect, or to add conductive cotton and other remedial measures.

6.4 EMI Protection

- There are three elements of electromagnetic interference: interference source, coupled channel and sensitive equipment. We can not handle sensitive equipment; can only deal with EMI by the interference source and the coupling channel. To solve the EMI problem, the best way is to eliminate the interference source, if it can not be eliminated, find the way to cut off the coupling channel or to avoid the antenna effect.
- The PCB interference source is generally difficult to be completely eliminated, can through filter, ground, balance, impedance control, improves signal quality (such as termination) and other methods to deal with. Various methods are generally used synthetically, but good grounding is the most basic requirement.
- The commonly used to deal with EMI is shielding materials, special filters, resistors, capacitors, inductors, beads, common mode inductance / magnetic ring, absorbing materials, spread spectrum parts and so on.
- The filter selection principle: If the load (receiver) is high impedance (the general single-ended signal interface is high impedance, such as SDIO, RBG, CIF, etc.), then select the capacitive filter device into the trace; if the load is low impedance (such as power output interface), then select the inductive filter part into the trace. The use of the filter can not make the signal quality beyond its SI permissible range. Differential interfaces typically use common mode inductors to suppress EMI.
- The PCB shielding measures to be a good grounding, or may cause radiation leakage or shielding measures to form the antenna effect, the connector shield needs to meet the relevant technical standards.
- RK3399 can be used spread spectrum function by modules. The degree of the spread spectrum depends on signal requirements of the relevant part. See RK3399 spread spectrum description for specific measures.
- EMI and ESD have a high degree of consistency on the requirements of LAYOUT, the layout request of ESD, most applicable for EMI protection. Also add the following requirements:
  - Ensure signal integrity as much as possible.

- The differential signal to do the same length and tight coupling to ensure that the differential signal symmetry; and minimize the differential signal and the clock dislocation, to avoid EMI caused by the common mode signal.
- Use plug-in electrolytic capacitors and other components with metal shell devices, should avoid the coupling interference signal to produce radiation. Also need to avoid the interference signal from the housing coupling to the other signal.

Chapter7 Welding Process

7.1 Overview

RK3399 for the ROHS directive certification products, that is, Lead-free products. This chapter regulates the basic settings of the temperature of the client when using the RK3399 SMT. It mainly introduces the process control of the customer when using re-flow soldering for RK3399; mainly lead-free process and mixed process.

7.2 Terminology

The terminology in this chapter is explained as follows:

- Lead-free: Lead-free process.
- Pb-free: Lead-free process; all parts (motherboard, all IC, resistance capacitors, etc.) are lead-free parts, and the use of lead-free solder paste pure lead-free process.
- Reflow profile: Reflow soldering temperature curve.
- ROHS: Restriction of Hazardous Substances.
- SMT: Surface Mount Technology.
- Sn-Pb: Tin-lead mixed process; refers to use lead solder paste and have both lead-free BGA and lead IC hybrid welding process.

7.3 Solder Re-flow Requirements

7.3.1 Solder Paste Composition Requirements

Solder alloy and flux specific gravity of 90%: 10%; volume ratio: 50%: 50%, solder paste refrigerate temperature is 2 ~ 10 ℃, should be used after the temperature restore to room temperature, the restore temperature time is 3 ~ 4 hours and make a good time recording.

7.3.2 SMT Re-flow Profile

As the RK3399 and other IC are environmentally friendly materials, it is recommended to use Pb-Free process. The reflow profile below is only recommended by the JEDEC J-STD-020D process, the user needs to adjust according to the actual production situation.

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)*	See classification temp in Table 4.1	See classification temp in Table 4.2
Time (t_p)** within 5 °C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Figure 7-1 Reflow Profile Classification

Package Thickness	Volume mm³ <350	Volume mm³ 350 - 2000	Volume mm³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Figure 7-2 Lead-free Process Device Package Heat-resistant Standard

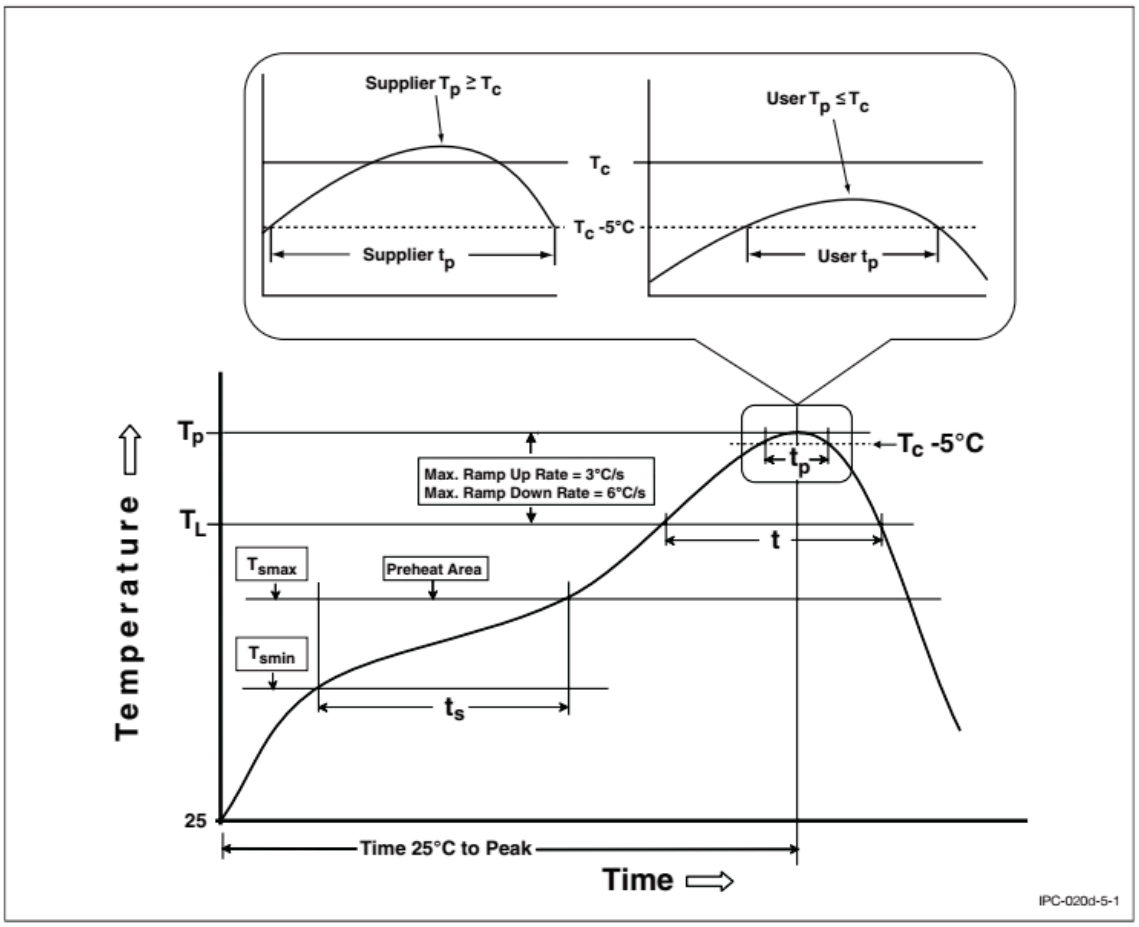


Figure 7-3 Pb-free Reflow Profile

7.3.3 SMT Recommended Reflow Profile

RK recommended SMT curve is shown in Figure 7-4:

Step 1 Board Preheat	Step 2 Soak Time	Step 3 Peak Reflow & Time Above 220 °C	Step 4 Cool Down
Start with solder joint temp ≤ 40°C	After nozzle is lowered prior to peak reflow (Soak Time: Paste dependant; consult paste manufacturer)	Solder Joint Temp 230 – 250°C Above ≥217°C 60 – 90 sec Max delta-t of solder joint temperature at peak reflow ≤10°C	Substrate MAX Temperature ≤260°C Die Peak Temperature ≤300°C
Rising Ramp Rate 0.5 – 2.5° C/ Sec.	Solder Joint Temp: 200 to 220°C		Cooling Ramp Rate -0.5 to – 2.0°C/sec
Board Preheat Solder Joint Temp: 125 – 150°C	Critical Ramp Rate (205 to 215°C): 0.35 – 0.75°C/sec.	Peak Temp Range, and Time Above ≥217°C spec's met.	PCB land/pad temperature needs to be at 100 – 130°C ±5°C when removing board from rework machine bottom heater at end of component removal operation or ≤80°C when using stand alone PCB Pre-Heater for PCB land/pad site dress operation.
Preheat with bottom heater, before nozzle is lowered	Nozzle has lowered to reflow component	Nozzle is down during peak reflow	Nozzle raises to home position when solder joint reaches peak temp range

Figure 7-4 Pb-free Reflow Profile Parameter

Chapter8 Packaging and Storage Conditions

8.1 Overview

The chapter provides of the RK3399 storage and use norms to ensure that the product is safe and correctly used.

8.2 Terminology

The terminology in this chapter is explained as follows:

- Desiccant: A material used to adsorb moisture.
- Floor life: The product allows the longest time in the environment, from unpacking the moisture barrier bag to SMT.
- HIC: Humidity Indicator Card.
- MSL: Moisture Sensitivity Level.
- MBB: Moisture Barrier Bag

8.3 Dry Vacuum Packaging

The dry vacuum packaging material of the product is as follows:

- Desiccant.
- HIC.
- MMB, aluminum foil, silver opaque, with a wet-sensitive grade logo.

Figure 8-1 RK3399 Dry Vacuum Packaging

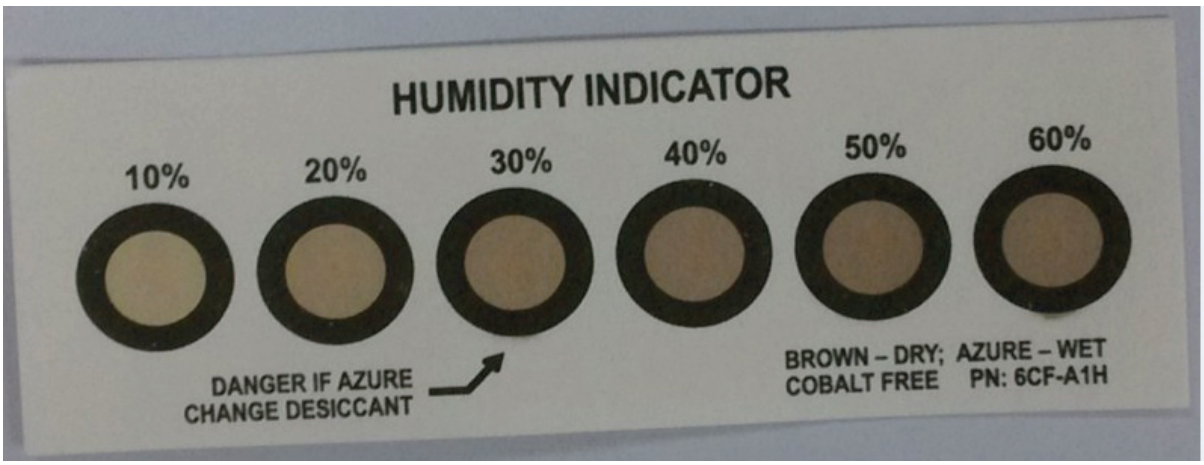


Figure 8-2 Humidity Indicator Card

8.4 Product Storage

8.4.1 Storage Environment

Product is vacuum packaged, environment temperature ≤ 30 ℃ and relative humidity 60% RH.

8.4.2 Shelf Life

In the temperature ≦ 40 ℃ and relative humidity <90%, up to 12 months.

8.4.3 Exposure Time

Under ambient conditions <30 ° C and relative humidity 60%, please refer to Table 8-1 below.
RK3399 MSL is grade 3, very sensitive to humidity. If you do not use after the unpacking for a long time, and in SMT without baked, will be likely to appear chip failure.

Table 8-1 Moisture Sensitivity Level（MSL）

MSL	Exposure Time Factory environmental conditions：≦30 ℃ /60 %RH
1	Unlimited at ≤300 ℃/85 %RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use, must be reflowed within the time limit specified on the label.

8.5 Moisture Sensitive Parts use method

The RK3399 must be baked in the following cases:

- Humidity indicator card at 23 ± 5 ℃,> 10% of the points have been discolored. (Please refer to the humidity indicator card for color change).
- continuous or cumulative exposure time of more than 72 hours in the factory environment ≦ 30 ℃ / 60% RH, or not stored in the <10% RH environment.

RK3399 after unpacking the time to re-baking please refer to the following table 8-2, 125 ℃ to be 9 hours, 90 ℃ to be 33 hours. So please use immediately after unpacking, if placed in the air for more than 72 hours, please bake and then use.

Table 8-2 RK3399 Re-bake Reference

Package Body	MSL	High Temp Bake @125℃ +10/-0℃		Medium Temp Bake @90℃+8/-0℃		Low Temp Bake @40℃ +5/-0℃	
		Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h	Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h	Exceeding Floor Life by > 72h	Exceeding Floor Life by ≤ 72h
Thickness ≥ 1.6mm	3	Bake 9 hours	Bake 7 hours	Bake 33 hours	Bake 23 hours	Bake 13 days	Bake 9 days

Notes:

The table shows the minimum baking time required after damp.
Re-bake the preferred low-temperature baking.