

Rockchip RK3288 Datasheet

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Revision History

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Chapter 1 Introduction

1.1 Overview

RK3288 are low power, high performance processor for mobile phones, personal mobile internet device and other digital multimedia applications, and integrates quad-core Cortex-A17 with separately NEON coprocessor.

Many embedded powerful hardware engines provide optimized performance for high-end application. RK3288 supports almost full-format; include H.265 decoder by 2160p@60fps, H.264 decoder by 2160p@24fps, also support H.264/MVC/VP8 encoder by 1080p@30fps, high-quality JPEG encoder/decoder, and special image preprocessor and postprocessor.

Embedded 3D GPU makes RK3288 completely compatible with OpenGL ES1.1/2.0/3.0, OpenCL 1.2 and DirectX 11. Special 2D hardware engine with MMU will maximize display performance and provide very smoothly operation.

RK3288 has high-performance dual channel external memory interface (DDR3/DDR3L /LPDDR2/LPDDR3) capable of sustaining demanding memory bandwidth, also provides a complete set of peripheral interface to support very flexible applications.

RK3288 LOT NO# end with "W" is upgraded version, could support HDCP2.2 and USB 1.1.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 MicroProcessor

- Quad-core ARM Cortex-A17 MPCore processor, a high-performance, low-power and cached application processor
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- Superscalar, variable length, out-of-order pipeline with dynamic branch prediction, 8-stage pipeline
- Include VFP v3 hardware to support single and double-precision add, subtract, divide, multiply and accumulate, and square root operations
- SCU ensures memory coherency between the four CPUs
- Integrated 32KB L1 instruction cache , 32KB L1 data cache with 4-way set associative
- 1MB unified L2 Cache
- Trust zone technology support
- Full coresight debug solution
 - Debug and trace visibility of whole systems
 - ETM trace support
 - Invasive and non-invasive debug
- Six separate power domains for every core to support internal power switch and externally turn on/off based on different application scenario
 - PD_A17_0: 1st Cortex-A17 + Neon + FPU + L1 I/D Cache
 - PD_A17_1: 2nd Cortex-A17 + Neon + FPU + L1 I/D Cache
 - PD_A17_2: 3rd Cortex-A17 + Neon + FPU + L1 I/D Cache
 - PD_A17_3: 4th Cortex-A17 + Neon + FPU + L1 I/D Cache
 - PD_SCU: SCU + L2 Cache controller, and including PD_A17_0, PD_A17_1, PD_A17_2, PD_A17_3, debug logic
- One isolated voltage domain to support DVFS

1.2.2 Memory Organization

- Internal on-chip memory
 - BootRom
 - Internal SRAM for security and non-security access
- External off-chip memory^①
 - Dual channel DDR3/DDR3L
 - Dual channel LPDDR2
 - Dual channel LPDDR3
 - Dual channel async Nand Flash(include LBA Nand)
 - Single channel async Nand Flash(include LBA Nand)
 - Dual channel sync ONFI/toggle Nand Flash

1.2.3 Internal Memory

- Internal BootRom
 - Size : 20KB
 - Support system boot from the following device :
 - ◆ 8bits Async Nand Flash
 - ◆ 8bits Toggle Nand Flash
 - ◆ SPI interface
 - ◆ eMMC interface
 - ◆ SDMMC interface
 - Support system code download by the following interface:
 - ◆ USB OTG interface
- Internal SRAM
 - Size : 100KB
 - Support security and non-security access
 - Security or non-security space is software programmable
 - Security space can be 0KB,4KB,8KB,12KB,16KB, ... up to 96KB by 4KB step

1.2.4 External Memory or Storage device

- Dynamic Memory Interface (DDR3/DDR3L/LPDDR2/LPDDR3)
 - Compatible with JEDEC standard DDR3-1333/DDR3L-1333/LPDDR2-1066/LPDDR3-1066 SDRAM
 - Support 2 channel, each channel 16 or 32bits data widths
 - Support up to 2 ranks (chip selects) for each channel, totally 4GB (max) address space, maximum address space for one rank of channel 0 is also 4GB, which is software-configurable.
 - 16bits/32bits data width is software programmable
 - Programmable timing parameters to support DDR3/DDR3L/LPDDR2/LPDDR3 SDRAM from various vendor
 - Advanced command reordering and scheduling to maximize bus utilization
 - Low power modes, such as power-down and self-refresh for DDR3/LPDDR2/LPDDR3 SDRAM; clock stop and deep power-down for LPDDR2 SDRAM
 - Embedded dynamic drift detection in the PHY to get dynamic drift compensation with the controller
 - Programmable output and ODT impedance with dynamic PVT compensation
 - Support one low-power work mode: power down DDR PHY and most of DDR IO except two cs and cke output signals, make SDRAM still in self-refresh state to prevent data missing.
- Nand Flash Interface
 - Support dual channel async Nand Flash, each channel 8bits, up to 4 banks
 - Support dual channel sync DDR Nand Flash, each channel 8bits, up to 4 banks
 - Support LBA Nand Flash in async or sync mode
 - Up to 60bits hardware ECC

- For ToggleNand Flash, support DLL bypass and 1/4 or 1/8 clock adjust, maximum clock rate is 75MHz
- For async Nand Flash, support configurable interface timing , maximum data rate is 16bit/cycle
- Embedded special DMA interface to do data transfer
- Also support data transfer together with general PERI_DMACH in SoC system
- eMMC Interface
 - Compatible with standard iNAND interface
 - Support MMC4.5 protocol
 - Provide eMMC boot sequence to receive boot data from external eMMC device
 - Support FIFO over-run and under-run prevention by stopping card clock automatically
 - Support CRC generation and error detection
 - Embedded clock frequency division control to provide programmable baud rate
 - Support block size from 1 to 65535Bytes
 - 8bits data bus width
- SD/MMC Interface
 - Compatible with SD3.0, MMC ver4.5
 - Support FIFO over-run and under-run prevention by stopping card clock automatically
 - Support CRC generation and error detection
 - Embedded clock frequency division control to provide programmable baud rate
 - Support block size from 1 to 65535Bytes
 - Data bus width is 4bits

1.2.5 System Component

- CRU (clock & reset unit)
 - Support clock gating control for individual components inside RK3288
 - One oscillator with 24MHz clock input and 5 embedded PLLs
 - Up to 2.2GHz clock output for all PLLs
 - Support global soft-reset control for whole SOC, also individual soft-reset for every components
- PMU(power management unit)
 - Multiple-configurable work modes to save power by different frequency or automatical clock gating control or power domain on/off control
 - Lots of wakeup sources in different mode
 - 4 separate voltage domains
 - 12 separate power domains, which can be power up/down by software based on different application scenes
- Timer
 - 8 on-chip 64bits Timers in SoC with interrupt-based operation
 - Provide two operation modes: free-running and user-defined count
 - Support timer work state checkable
 - Fixed 24MHz clock input
- PWM
 - Four on-chip PWMs with interrupt-based operation
 - Programmable pre-scaled operation to bus clock and then further scaled
 - Embedded 32-bit timer/counter facility
 - Support capture mode
 - Support continuous mode or one-shot mode
 - Provides reference mode and output various duty-cycle waveform

- Watch Dog
 - 32 bits watchdog counter width
 - Counter clock is from apb bus clock
 - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
 - WDT can perform two types of operations when timeout occurs:
 - ◆ Generate a system reset
 - ◆ First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
 - Programmable reset pulse length
 - Totally 16 defined-ranges of main timeout period
- Interrupt Controller
 - Support 3 PPI interrupt source and 112 SPI interrupt sources input from different components inside RK3288
 - Support 16 software-triggered interrupts
 - Input interrupt level is fixed , only high-level sensitive
 - Two interrupt outputs (nFIQ and nIRQ) separately for eachCortex-A17, both are low-level sensitive
 - Support different interrupt priority for each interrupt source, and they are always software-programmable
- DMAC
 - Micro-code programming based DMA
 - The specific instruction set provides flexibility for programming DMA transfers
 - Linked list DMA function is supported to complete scatter-gather transfer
 - Support internal instruction cache
 - Embedded DMA manager thread
 - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
 - Signals the occurrence of various DMA events using the interrupt output signals
 - Mapping relationship between each channel and different interrupt outputs is software-programmable
 - Two embedded DMA controller, BUS_DMAC is for bus system, PERI_DMAC is for peripheral system
 - BUS_DMAC features:
 - ◆ 6 channels totally
 - ◆ 6 hardware request from peripherals
 - ◆ 2 interrupt output
 - ◆ Dual APB slave interface for register config, designated as secure and non-secure
 - ◆ Support trustzone technology and programmable secure state for each DMA channel
 - PERI_DMAC features:
 - ◆ 7 channels totally
 - ◆ 9 hardware request from peripherals
 - ◆ 2 interrupt output
 - ◆ Not support trustzone technology
- Security system
 - Support trustzone technology for the following components inside RK3288
 - ◆ Cortex-A17, support security and non-security mode, switch by software
 - ◆ BUS_DMAC, support some dedicated channels work only in security mode
 - ◆ eFuse, only accessed by Cortex-A17 in security mode
 - ◆ Internal memory , part of space is addressed only in security mode, detailed size

- is software-programmable together with TZMA(trustzone memory adapter) and TZPC(trustzone protection controller)
- Embedded encryption and decryption engine
 - ◆ Support AES 128/192/256 bits key mode, ECB/CBC/CTR chain mode, Slave/FIFO mode
 - ◆ Support DES/3DES (ECB and CBC chain mode) , 3DES (EDE/ EEE key mode), Slave/FIFO mode
 - ◆ Support SHA1/SHA256/MD5 (with hardware padding) HASH function, FIFO mode only
 - ◆ Support 160 bit Pseudo Random Number Generator (PRNG)
 - ◆ Support 256 bit True Random Number Generator (PRNG)
- Support PKA 512/1024/2048 bit Exp ModulatorSupport security boot
- Support security debug

1.2.6 Video CODEC

- Shared internal memory and bus interface for video decoder and encoder②
- Embedded memory management unit(MMU)
 - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4,H.263, H.264, AVS, VC-1, VP8, MVC
 - Error detection and concealment support for all video formats
 - Output data format is YUV420 semi-planar, and YUV400(monochrome) is also supported for H.264
 - H.264 up to HP level 5.1 : 2160p@24fps (3840x2160)③
 - MPEG-4 up to ASP level 5: 1080p@60fps (1920x1088)
 - MPEG-2 up to MP : 1080p@60fps (1920x1088)
 - MPEG-1 up to MP : 1080p@60fps (1920x1088)
 - H.263 : 576p@60fps(720x576)
 - VC-1 up to AP level 3 : 1080p@30fps (1920x1088)
 - VP8 : 1080p@60fps (1920x1088)
 - AVS : 1080p@60fps (1920x1088)
 - MVC : 1080p@60fps (1920x1088)
 - For AVS, 4:4:4 sampling not supported
 - For H.264, image cropping not supported
 - For MPEG-4,GMC(global motion compensation)not supported
 - For VC-1, upscaling and range mapping are supported in image post-processor
 - For MPEG-4 SP/H.263, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit

1.2.7 Video Encoder

- Support video encoder for H.264 (BP@level4.0, MP@level4.0, HP@level4.0), MVC and VP8
- Only support I and P slices, not B slices
- Support error resilience based on constrained intra prediction and slices
- Input data format:
 - ◆ YCbCr 4:2:0 planar
 - ◆ YCbCr 4:2:0 semi-planar
 - ◆ YCbYCr 4:2:2
 - ◆ CbYCrY 4:2:2 interleaved
 - ◆ RGB444 and BGR444
 - ◆ RGB555 and BGR555
 - ◆ RGB565 and BGR565
 - ◆ RGB888 and BRG888
 - ◆ RGB101010 and BRG101010
- Image size is from 96x96 to 1920x1088(Full HD)
- Maximum frame rate is up to 30fps@1920x1080③
- Bit rate supported is from 10Kbps to 20Mbps

1.2.8 HEVC Decoder

- Main/Main10 HEVC/H.265 decoder, 4k@60FPS
- Support up to 4096x2304 resolution
- Embedded memory management unit(MMU)
- Stream error detector (28 IDs)
- Internal 128k cache for bandwidth reduction
- Multi-clock domains and auto clock-gating design for power saving

1.2.9 JPEG CODEC

- JPEG decoder
 - Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
 - Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
 - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
 - Support JPEG ROI(region of image) decode
 - Maximum data rate④ is up to 76million pixels per second
 - Embedded memory management unit(MMU)
- JPEG encoder
 - Input raw image :
 - ◆ YCbCr 4:2:0 planar
 - ◆ YCbCr 4:2:0 semi-planar
 - ◆ YCbYCr 4:2:2
 - ◆ CbYCrY 4:2:2 interleaved
 - ◆ RGB444 and BGR444
 - ◆ RGB555 and BGR555
 - ◆ RGB565 and BGR565
 - ◆ RGB888 and BRG888
 - ◆ RGB101010 and BRG101010
 - Output JPEG file: JFIF file format 1.02 or Non-progressive JPEG
 - Encoder image size up to 8192x8192(64million pixels) from 96x32
 - Maximum data rate④ up to 90million pixels per second
 - Embedded memory management unit(MMU)

1.2.10 Image Enhancement

- Image pre-processor
 - Only used together with HD video encoder inside RK3288, not support stand-alone mode
 - Provides RGB to YCbCr 4:2:0 color space conversion, compatible with BT601, BT709 or user defined coefficients
 - Provides YCbCr4:2:2 to YCbCr4:2:0 color space conversion
 - Support cropping operation from 8192x8192 to any supported encoding size
 - Support rotation with 90 or 270 degrees
- Video stabilization
 - Work in combined mode with HD video encoder inside RK3288 and stand-alone mode
 - Adaptive motion compensation filter
 - Support scene detection from video sequence, encodes key frame when scene change noticed
- Image Post-Processor(embedded inside video decoder)
 - Combined with HD video decoder and JPEG decoder, post-processor can read input data directly from decoder output to reduce bus bandwidth

- Also work as a stand-alone mode, its input data is from image data stored in external memory
- Input data format:
 - ◆ Any format generated by video decoder in combined mode
 - ◆ YCbCr 4:2:0 semi-planar
 - ◆ YCbCr 4:2:0 planar
 - ◆ YCbYCr 4:2:2
 - ◆ YCrYCb 4:2:2
 - ◆ CbYCrY 4:2:2
 - ◆ CrYCbY 4:2:2
- Output data format:
 - ◆ YCbCr 4:2:0 semi-planar
 - ◆ YCbYCr 4:2:2
 - ◆ YCrYCb 4:2:2
 - ◆ CbYCrY 4:2:2
 - ◆ CrYCbY 4:2:2
 - ◆ Fully configurable ARGB channel lengths and locations inside 32bits, such as ARGB8888, RGB565, ARGB4444 etc.
- Input image size:
 - ◆ Combined mode: from 48x48 to 8176x8176 (66.8Mpixels)
 - ◆ Stand-alone mode: width from 48 to 8176, height from 48 to 8176, and maximum size limited to 16.7Mpixels
 - ◆ Step size is 16 pixels
- Output image size: from 16x16 to 1920x1088 (horizontal step size 8, vertical step size 2)
- Support image up-scaling:
 - ◆ Bicubic polynomial interpolation with a four-tap horizontal kernel and a two-tap vertical kernel
 - ◆ Arbitrary non-integer scaling ratio separately for both dimensions
 - ◆ Maximum output width is 3x input width
 - ◆ Maximum output height is 3x input height
- Support image down-scaling:
 - ◆ Arbitrary non-integer scaling ratio separately for both dimensions
 - ◆ Unlimited down-scaling ratio
- Support YUV to RGB color conversion, compatible with BT.601-5, BT.709 and user definable conversion coefficient
- Support dithering (2x2 ordered spatial dithering) for 4/5/6bit RGB channel precision
- Support programmable alpha channel and alpha blending operation with the following overlay input formats:
 - ◆ 8bit alpha +YUV444, big endian channel order with AYUV8888
 - ◆ 8bit alpha +24bit RGB, big endian channel order with ARGB8888
- Support deinterlacing with conditional spatial deinterlace filtering, only compatible with YUV420 input format
- Support RGB image contrast/brightness/color saturation adjustment
- Support image cropping & digital zoom only for JPEG or stand-alone mode
- Support picture in picture
- Support image rotation (horizontal flip, vertical flip, rotation 90,180 or 270 degrees)
- Image Enhancement-Processor (IEP)
 - Image format
 - ◆ Input data: XRGB/RGB565/YUV420/YUV422
 - ◆ Output data: ARGB/RGB565/YUV420/YUV422
 - ◆ The format ARGB/XRGB/RGB565/YUV support swap
 - ◆ Support YUV semi-planar/planar
 - ◆ Support BT601_l/BT601_f/BT709_l/BT709_f color space conversion
 - ◆ Support RGB dither up/down conversion
 - ◆ Support YUV up/down sampling conversion

- ◆ Max source image resolution: 8192x8192
- ◆ Max scaled image resolution: 4096x4096
- Enhancement
 - ◆ Gamma adjustment with programmable mapping table
 - ◆ Hue/Saturation/Brightness/Contrast enhancement
 - ◆ Color enhancement with programmable coefficient
 - ◆ Detail enhancement with filter matrix up to 9x9
 - ◆ Edge enhancement with filter matrix up to 9x9
 - ◆ Programmable difference table for detail enhancement
 - ◆ Programmable distance table for detail and edge enhancement
- Noise reduction
 - ◆ Compression noise reduction with filter matrix up to 9x9
 - ◆ Programmable difference table for compression noise reduction
 - ◆ Programmable distance table for compression noise reduction
 - ◆ Spatial sampling noise reduction
 - ◆ Temporal sampling noise reduction
 - ◆ Optional coefficient for sampling noise reduction
- Scaling
 - ◆ Horizontal down-scaling with vertical down-scaling
 - ◆ Horizontal down-scaling with vertical up-scaling
 - ◆ Horizontal up-scaling with vertical down-scaling
 - ◆ Horizontal up-scaling with vertical up-scaling
 - ◆ Arbitrary non-integer scaling ratio, from 1/16 to 16
- Deinterlace
 - ◆ Input 4 fields, output 2 frames mode
 - ◆ Input 4 fields, output 1 frames mode
 - ◆ Input 2 fields, output 1 frames mode
 - ◆ Programmable motion detection coefficient
 - ◆ Programmable high frequency factor
 - ◆ Programmable edge interpolation parameter
 - ◆ Source width up to 1920
- Interface
 - ◆ Programmable direct path to VOP
- Embedded memory management unit(MMU)

1.2.11 Graphics Engine

- 3D Graphics Engine :
 - ARM Mali-T764 GPU core
 - High performance OpenGL ES1.1/2.0/3.0, OpenCL 1.2, DirectX 11(W version only)
 - Embedded 4 shader cores with shared hierarchical tiler
 - Provide MMU and L2 Cache with 256KB size
 - Image quality using double-precision FP64, and anti-aliasing
- 2D Graphics Engine (RGA2):
 - BitBlit with Stretch Blit, Simple Blit and Filter Blit
 - Color fill with gradient fill, and pattern fill
 - Line drawing with anti-aliasing and specified width
 - High-performance stretch and shrink
 - Monochrome expansion for text rendering
 - ROP2,ROP3,ROP4
 - Alpha blending modes including global alpha, per pixel alpha, porter-duff and fading
 - 8K x 8K input and 2K x 2K output raster 2D coordinate system
 - Arbitrary degrees rotation with anti-aliasing on every 2D primitive
 - Blending, scaling and rotation are supported in one pass for Bitbilt
 - Source format:

- ◆ ABGR8888, XBGR888, ARGB8888, XRGB888
- ◆ RGB888, RGB565
- ◆ RGBA5551, RGBA4444
- ◆ YUV420 planar, YUV420 semi-planar
- ◆ YUV422 planar, YUV422 semi-planar
- ◆ BPP8, BPP4, BPP2, BPP1
- Destination formats:
 - ◆ ABGR8888, XBGR888, ARGB8888, XRGB888
 - ◆ RGB888, RGB565
 - ◆ RGBA5551, RGBA4444
 - ◆ YUV420 planar, YUV420 semi-planar only in filter and pre-scale mode
 - ◆ YUV422 planar, YUV422 semi-planar only in filter and pre-scale mode

1.2.12 Video IN/OUT

- Camera Interface(DVP interface only)
 - Support up to 5M pixels
 - 8bits BT656(PAL/NTSC) interface
 - 16bits BT601 DDR interface
 - 8bits/10bits/12bits raw data interface
 - YUV422 data input format with adjustable YUV sequence
 - YUV422,YUV420 output format with separately Y and UV space
 - Support picture in picture (PIP)
 - Support simple image effects such as arbitrary (sepia), Negative, Art freeze, Embossing etc.
 - Support static histogram statistics and white balance statistics
 - Support image crop with arbitrary windows
 - Support scale up/down from 1/8 to 8 with arbitrary non-integer ratio
- Camera Interface and Image Processor(Interface and Image Processing)
 - Maximum input resolution of 14M(4416x3312) pixels
 - Main scaler with pixel-accurate up- and down-scaling to any resolution between 4416x3312 and 32x16 pixel in processing mode
 - Self scaler with pixel-accurate up- and down-scaling to any resolution between 1920x1080 and 32x16 pixel in processing mode
 - support of semiplanar NV21 color storage format
 - support of independent image cropping on main and self path
 - ITU-R BT 601/656 compliant video interface supporting YCbCr or RGB Bayer data
 - 12 bit camera interface
 - 12 bit resolution per color component internally
 - YCbCr 4:2:2 processing
 - Hardware JPEG encoder incl. JFIF1.02 stream generator and programmable quantization and Huffman tables
 - Windowing and frame synchronization
 - Frame skip support for video (e.g. MPEG-4) encoding
 - Macro block line, frame end, capture error, data loss interrupts and sync. (h_start, v_start) interrupts
 - Luminance/chrominance and chrominance blue/red swapping for YUV input signals
 - Continuous resize support
 - Color processing (contrast, saturation, brightness, hue, offset, range)
 - Display-ready RGB output in self-picture path (RGB888, RGB666 and RGB565)
 - Rotation unit in self-picture path (90°, 180°, 270° and h/v flipping) for RGB output
 - Read port provided to read back a picture from system memory
 - Simultaneous picture read back, resizing and storing through self path while main path captures the camera picture
 - Black level compensation
 - Four channel Lens shade correction (Vignetting)

- Auto focus measurement
- White balancing and black level measurement
- Auto exposure support by brightness measurement in 5x5 sub windows
- Defect pixel cluster correction unit (DPCC) supports on the fly and table based pixel correction
- De-noising pre filter (DPF)
- Enhanced color interpolation (RGB Bayer demosaicing)
- Chromatic aberration correction
- Combined edge sensitive Sharpening / Blurring filter (Noise filter)
- Color correction matrix (cross talk matrix)
- Global Tone Mapping with wide dynamic range unit (WDR)
- Image Stabilization support and Video Stabilization Measurement
- Flexible Histogram calculation
- Digital image effects (Emboss, Sketch, Sepia, B/W (Grayscale), Color Selection, Negative image, sharpening)
- Solarize effect through gamma correction
- Display Interface
 - Embedded two channel display interfaces: VOP_BIG and VOP_LIT.
 - Parallel Display interface
 - ◆ Parallel RGB LCD Interface:
 - 30-bit(RGB101010),24-bit(RGB888),18-bit(RGB666), 15-bit(RGB565)
 - ◆ Serial RGB LCD Interface(optional):
 - 2x12-bit, 3x8-bit(RGB delta support), 3x8-bit+dummy
 - ◆ MCU LCD interface(optional):
 - i-8080(up to 24-bit RGB), Hold/Auto/Bypass modes
 - ◆ TV Interface: ITU-R BT.656(8-bit, 480i/576i/1080i)
 - ◆ DDR output interface:
 - parallel RGB and 2x12-bit serial RGB
 - Single or dual clock out
 - ◆ dither down:
 - allegro,FRC
 - gamma after dither
 - ◆ Max output resolution: 3840x2160 (for VOP_BIG), 2560x1600(for VOP_LIT)
 - ◆ Scanning timing 8192x4096
 - Display process
 - ◆ Background layer:
 - programmable 24-bit color
 - ◆ Win0 (Video0) layer:
 - RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
 - Support virtual display
 - 1/8 to 8 scaling-down and scaling-up engine:
 - ✧ Scale up using bicubic or bilinear;
 - ✧ Scale down using bilinear or average;
 - ✧ 4 Bicubic tables : precise,spline,catrom,mitchell;
 - ✧ coord 8bit, coe 8bit signed
 - x-mirror,y-mirror
 - ◆ Win1 (Video1) layer:
 - RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
 - Support virtual display
 - 1/8 to 8 scaling-down and scaling-up engine
 - ✧ Scale up using bicubic or bilinear;
 - ✧ Scale down using bilinear otraverage;
 - ✧ 4 Bicubic tables : precise,spline,catrom,mitchell;
 - ✧ coord 8bit, coe 8bit signed
 - x-mirror,y-mirror
 - ◆ Win2 (UI 0) layer:

- RGB888, ARGB888, RGB565, 1/2/4/8bpp
- Support virtual display
- 4 display regions
- x-mirror,y-mirror
- ◆ Win3 (UI 1) layer:
 - RGB888, ARGB888, RGB565, 1/2/4/8bpp
 - Support virtual display
 - 4 display regions
 - x-mirror,y-mirror
- ◆ Hardware cursor:
 - RGB888, ARGB888, RGB565, 1/2/4/8bpp
 - Support two size: 32x32,64x64,or 128x128
- ◆ Overlay:
 - Win0/Win1/Win2/Win3 256 level alpha blending(support pre-multiplied alpha)
 - Win0/Win1/Win2/Win3 overlay position exchangeable
 - Win0/Win1/Win2/Win3 Transparency color key
 - Win0/Win1/Win2/Win3 global/per-pixel alpha
 - HWC 256 level alpha blending
 - HWC global/per-pixel alpha
- Others
 - ◆ 3 x 256 x 8 bits display LUTs
 - ◆ YcbCr2RGB(rec601-mpeg/rec601-jpeg/rec709/BT2020)and RGB2YcbCr
 - ◆ Support BCSH function
 - ◆ Support CABG function
 - ◆ QoS request signals
 - ◆ Gather transfer (Max 8)
 - ◆ Y/UV scheduler
 - ◆ Addr alignment
 - ◆ Support IEP direct path(win0/1/2/3)
 - ◆ Embedded memory management unit(MMU)
 - ◆ Support MIPI flow control

1.2.13 HDMI

- Single Physical Layer PHY with support for HDMI 1.4 and 2.0 operation
- For HDMI operation, support for the following:
 - Up to 1080p at 120 Hz and 4k x 2k at 60 Hz HDTV display resolutions and up to QXGA graphic display resolutions
 - 3-D video formats
 - Up to 10-bit Deep Color modes
 - Up to 18 Gbps aggregate bandwidth
 - 13.5–600 MHz input reference clock
 - HPD input analog comparator
- Link controller flexible interface with 30-, 60- or 120-bit SDR data access
- RK3288 Supports HDCP 1.4
- RK3288 W version support 4K YUV 4:2:0 output and HDCP 2.2

1.2.14 LVDS (RK3288-C has not this function)

- Comply with the TIA/EIA-644-A LVDS standard
- Combine LVTTTL IO, support LVDS/LVTTTL data output
- Support reference clock frequency range from 10Mhz to 148.5Mhz
- Support LVDS RGB 30/24/18bits color data transfer
- Support VESA/JEIDA LVDS data format transfer
- Support LVDS single channel and double channel data transfer, every channel include 5 data lanes and 1 clock lane

1.2.15 MIPI PHY

- Embedded 3 MIPI PHY, MIPI 0 only for TX, MIPI 1 for TX and RX, MIPI 2 only for RX
- Support 4 data lane, providing up to 4Gbps data rate
- Support 1080p @ 60fps output
- Lane operation ranging from 80 Mbps to 1 Gbps in forward direction

1.2.16 eDP PHY

- Support 4Kx2K @ 30fps
- Compliant with eDP TM Specification, version 1.1
- Up to 4 physical lanes of 2.7/1.62 Gbps/lane(HBR2/HBR/RBR)
- RGB, YCbCr 4:4:4, YCbCr 4:2:2 and 8/10/12 bit per component video format
- Support VESA DMT and CVT timing standards
- Fully support EIA/CEA-861D video timing and Info Frame structure
- Hot plug and unplug detection and link status monitor
- Support DDC/CI and MCCS command transmission when the monitor includes a display controller.
- Supports Panel Self Refresh(PSR)

1.2.17 Audio Interface

- I2S/PCM with 8ch
 - Support 8-channels audio transmitting in I2S mode and 2-channels in PCM mode.
 - Support 2-channels audio receiving in I2S and PCM mode
 - Audio resolution from 16bits to 32bits
 - Sample rate up to 192KHz
 - Provides master and slave work mode, software configurable
 - Support 3 I2S formats (normal, left-justified, right-justified)
 - Support 4 PCM formats(early, late1, late2, late3)
 - I2S and PCM mode cannot be used at the same time
- SPDIF
 - Support two 16-bit audio data store together in one 32-bit wide location
 - Support biphase format stereo audio data output
 - Support 16 to 31 bit audio data left or right justified in 32-bit wide sample data buffer
 - Support 16, 20, 24 bits audio data transfer in linear PCM mode
 - Support non-linear PCM transfer

1.2.18 Connectivity

- SDIO interface
 - Embedded 2 SDIO interface
 - Compatible with SDIO 3.0 protocol
 - 4bits data bus width
- High-speed ADC stream interface
 - Support single-channel 8bits/10bits interface
 - DMA-based and interrupt-based operation
 - Support 8bits TS stream interface
- TS interface
 - Supports two TS input channels and one TS output channel.
 - Supports 4 TS Input Mode: sync/valid mode in the case of serial TS input; nosync/valid mode, sync/valid, sync/burst mode in the case of parallel TS input.
 - Supports serial and parallel output mode with PCR adjustment, and lsb-msb or msb-lsb bit ordering can be chosen in the serial output mode.

- Supports 2 TS sources: demodulators and local memory.
 - Supports 2 Built-in PTIs(Programmable Transport Interface) to process TS simultaneously, and Each PTI supports:
 - ◆ 64 PID filters.
 - ◆ TS descrambling with 16 sets of Control Word under CSA v2.0 standard, up to 104Mbps
 - ◆ 16 PES/ES filters with PTS/DTS extraction and ES start code detection.
 - ◆ 4/8 PCR extraction channels
 - ◆ 64 Section filters with CRC check, and three interrupt mode: stop per unit, full-stop, recycle mode with version number check
 - ◆ PID done and error interrupts for each channel
 - ◆ PCR/DTS/PTS extraction interrupt for each channel
 - Supports 1 PVR (Personal Video Recording) output channel.
 - 1 built-in multi-channel DMA Controller.
- PS2 interface
 - Support PS/2 data communication protocol
 - Support PS/2 master mode
 - Software programmable timing requirement to support max PS/2 clockfrequency to 33KHZ
 - Support status to be queried for data communication error
 - Support interrupt mode for data communication finish
 - Support timeout mechanism for data communication
 - Support interrupt mode for data communication timeout
- Smart Card
 - support card activation and deactivation
 - support cold/warm reset
 - support Answer to Reset (ATR) response reception
 - support T0 for asynchronous half-duplex character transmission
 - support T1 for asynchronous half-duplex block transmission
 - support automatic operating voltage class selection
 - support adjustable clock rate and bit (baud) rate
 - support configurable automatic byte repetition
- Host interface
 - Low Pin Count interface(8 inputs/16 outputs or 16 inputs/8 outputs)
 - No mandatory Tri-State signals
 - All signals driven using source synchronous clock.(2 DDR clock signals per direction for TX and RX paths)
 - Low latency through serialization/deserialization
 - Transport clocks and bus clock are independent
 - Support Asymmetric(Host/Peripheral) communication operations
 - Support multiple outstanding transactions reads, writes and interrupts
 - Support Mirror Mode to enable self test with identical device
- GPS Interface
 - Single chip, integrate GPS bb with cpu
 - 32 DMA channels for AHB master access
 - Complete 1-band, C/A, and NMEA-0183 compatibility
 - Support reference frequencies 16.368MHz
 - High sensitivity for indoor fixes
 - Low power consumption
 - Low cost with smaller size
 - Multi modes support both standalone GPS and A_GPS

- GMAC 10/100/1000M Ethernet Controller
 - Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces
 - Supports 10/100-Mbps data transfer rates with the RMII interfaces
 - Supports both full-duplex and half-duplex operation
 - ◆ Supports CSMA/CD Protocol for half-duplex operation
 - ◆ Supports packet bursting and frame extension in 1000 Mbps half-duplex operation
 - ◆ Supports IEEE 802.3x flow control for full-duplex operation
 - ◆ Optional forwarding of received pause control frames to the user application in full-duplex operation
 - ◆ Back-pressure support for half-duplex operation
 - ◆ Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation
 - Preamble and start-of-frame data (SFD) insertion in Transmit, and deletion in Receive paths
 - Automatic CRC and pad generation controllable on a per-frame basis
 - Options for Automatic Pad/CRC Stripping on receive frames
 - Programmable InterFrameGap (40-96 bit times in steps of 8)
 - Supports a variety of flexible address filtering modes
 - Separate 32-bit status returned for transmission and reception packets
 - Supports IEEE 802.1Q VLAN tag detection for reception frames
 - Support detection of LAN wake-up frames and AMD Magic Packet frames
 - Support checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame
 - Support checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagrams
 - Comprehensive status reporting for normal operation and transfers with errors
 - Automatic generation of PAUSE frame control or backpressure signal to the GMAC core based on Receive FIFO-fill (threshold configurable) level
 - Handles automatic retransmission of Collision frames for transmission
 - Discards frames on late collision, excessive collisions, excessive deferral and underrun conditions
- SPI Controller
 - 3 on-chip SPI controller inside RK3288
 - Support serial-master and serial-slave mode, software-configurable
 - DMA-based or interrupt-based operation
 - Embedded two 32x16bits FIFO for TX and RX operation respectively
 - Support 2 chip-selects output in serial-master mode
- Uart Controller
 - 5 on-chip uart controller inside RK3288
 - DMA-based or interrupt-based operation
 - For all UART, two 64Bytes FIFOs are embedded for TX/RX operation respectively
 - Support 5bit,6bit,7bit,8bit serial data transmit or receive
 - Standard asynchronous communication bits such as start, stop and parity
 - Support different input clock for uart operation to get up to 4Mbps or other special baud rate
 - Support non-integer clock divides for baud clock generation
 - Auto flow control mode is for all UART, except UART_DBG
- I2C controller
 - 6 on-chip I2C controller in RK3288
 - Multi-master I2C operation
 - Support 7bits and 10bits address mode
 - Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast

- mode
 - Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode
- GPIO
 - Totally 160 GPIOs
 - All of GPIOs can be used to generate interrupt to Cortex-A17
 - GPIO0 can be used to wakeup system from low-power mode
 - The pull direction(pullup or pulldown) for all of GPIOs are software-programmable
 - All of GPIOs are always in input direction in default after power-on-reset
 - The drive strength for all of GPIOs is software-programmable
- USB Host2.0
 - Embedded 2 USB Host2.0 interfaces
 - USB host (ECHI controller) only supports USB2.0, and USB1.1 (W version).
USB host (DW controller) support USB2.0/USB1.1.
 - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
 - Provides 16 host mode channels
 - Support periodic out channel in host mode
- USB OTG2.0
 - Compatible with USB OTG2.0 specification
 - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
 - Support up to 9 device mode endpoints in addition to control endpoint 0
 - Support up to 6 device mode IN endpoints including control endpoint 0
 - Endpoints 1/3/5/7 can be used only as data IN endpoint
 - Endpoints 2/4/6 can be used only as data OUT endpoint
 - Endpoints 8/9 can be used as data OUT and IN endpoint
 - Provides 9 host mode channels
- USIC Interface
 - Compliant with the USB2.0 Specification and Enhanced Host Controller Interface Specification 2.0
 - 1 Port USIC PHY Interface Operates in host mode
 - Built-in one 512x64 bits FIFO
 - Internal DMA with scatter/gather function

1.2.19 Others

- Temperature Sensor(TS-ADC)
 - 3 bipolar-based temperature-sensing cell embedded
 - 3-channel 12-bits SAR ADC
- SAR-ADC(Successive Approximation Register)
 - 3-channel single-ended 10-bit SAR analog-to-digital converter
- eFuse
 - Two high-density electrical Fuse is integrated: 256bits (32x8) / 1024bits (32x32)
 - Support standby mode

Notes :^① DDR3/LPDDR2/LPDDR3 are not used simultaneously as well as async and sync ddr nand flash

^② In RK3288, Video decoder (except H.265) and encoder are not used simultaneously because of shared internal buffer

^③ Actual maximum frame rate will depend on the clock frequency and system bus performance

^④ Actual maximum data rate will depend on the clock frequency and JPEG compression rate

1.2.20 Software difference for W version and others

| Item | Updated | Note |
|-------------|--|---------------------------------------|
| USB HOST | Add OHCI feature | need SW patch to support new feature |
| | Fixed EHCI bug | |
| GPU | Support DirectX | need SW update to support new feature |
| VOP | Support YUV 4:2:0 output for 4K 60fps | need SW patch to support new feature |
| | CABC update | |
| PAD | Modified jtag_rstn IO default to pull-down | HW and SW compatible |
| VIDEO CODEC | improve VLC performance | need SW patch to support new feature |
| UART_DEBUG | update uart_debug default setting | SW compatible |
| ISP/VIP | update ISP and DVP interface | need SW patch to support new feature |
| RGA2 | Fixed bug of RGA2 scale | SW compatible |
| IEP | Support 4K | need SW update to support new feature |
| HDMI | Add HDCP2.2 feature | need SW update to support new feature |
| I2C | Modified I2C IO timing | SW compatible |
| HDMI | Update HDMI_cecin_msk control | need SW update to support new feature |
| SGRF | Update SGRF reset value | SW compatible |

1.3 Block Diagram

The following diagram shows the basic block diagram for RK3288.

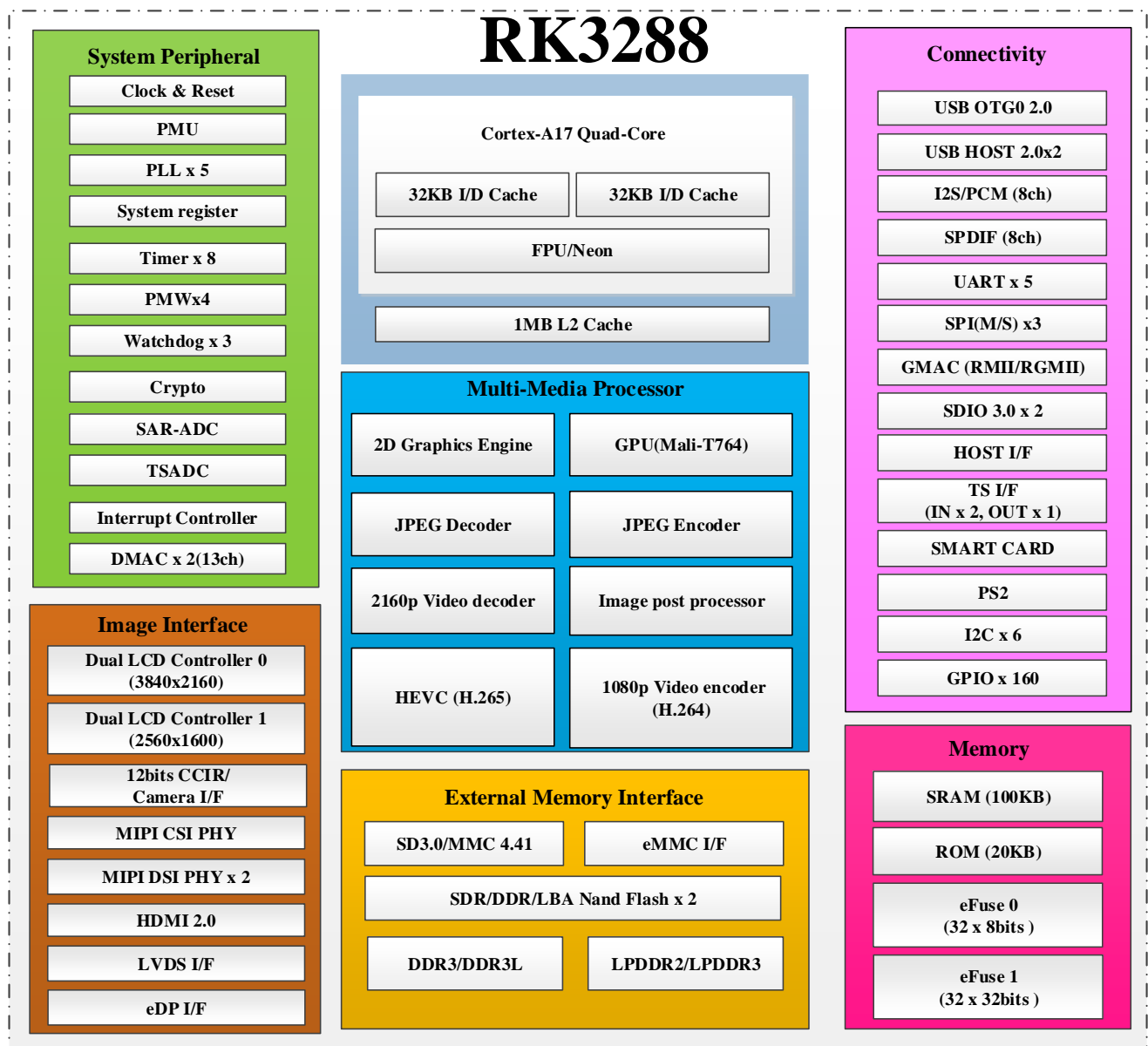


Fig. 1-1 RK3288 Block Diagram

Chapter 2 Package information

2.1 Ordering information

| Orderable Device | Device Version | RoHS status | Package | Package Qty | Device Feature | Available |
|------------------|----------------|-------------|------------|-------------|---|-----------|
| RK3288 | | RoHS | FCBGA636LD | 700 | 1.6GHz Quad core A17 AP | EOL |
| RK3288 | W Version | RoHS | FCBGA636LD | 700 | 1.6GHz Quad core A17 AP | MP |
| RK3288-C | | RoHS | FCBGA636LD | 700 | 1.8GHz Quad core A17 AP For ChromeOS application | MP |
| RK3288K | W Version | RoHS | FCBGA636LD | 700 | 1.8GHz Quad core A17 AP for commercial application | MP |
| RK3288-D | | RoHS | FCBGA636LD | 700 | 1.6GHz Quad core A17 AP with Dolby function | MP |
| RK3288-CG | | RoHS | FCBGA636LD | 700 | 1.8GHz Quad core A17 AP | EOL |
| RK3288-CG | W Version | RoHS | FCBGA636LD | 700 | 1.8GHz Quad core A17 AP | MP |

2.2 Top Marking:

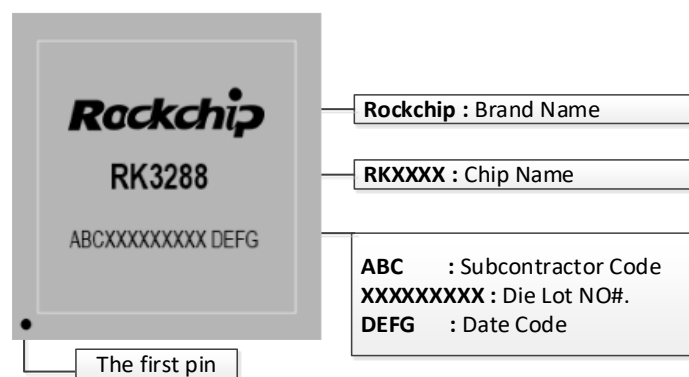


Fig. 2-1 RK3288 Silk Marking

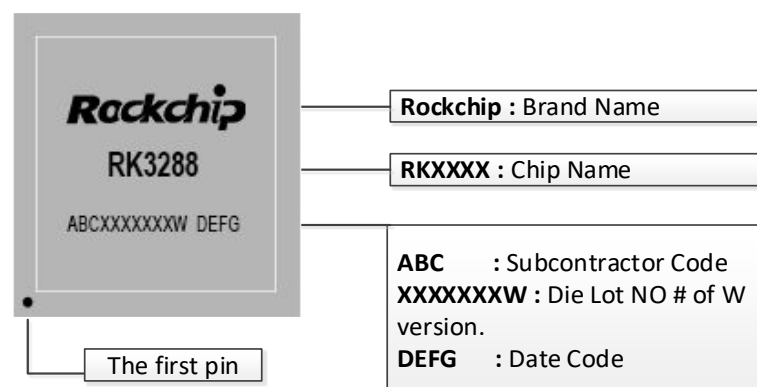


Fig. 2-2 RK3288 W Version Silk Marking

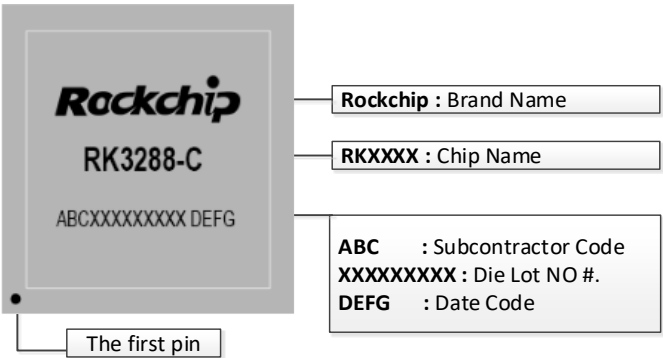


Fig. 2-3 RK3288-C Silk Marking

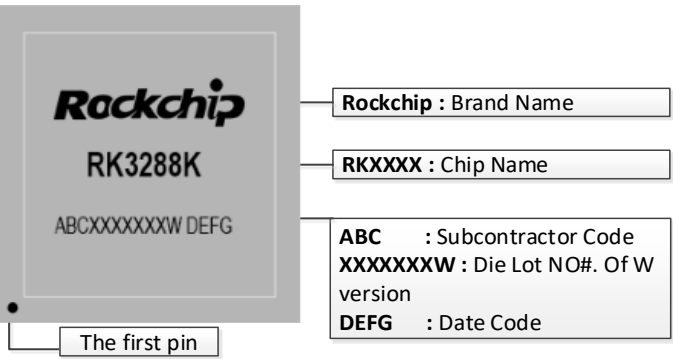


Fig. 2-4 RK3288K Silk Marking

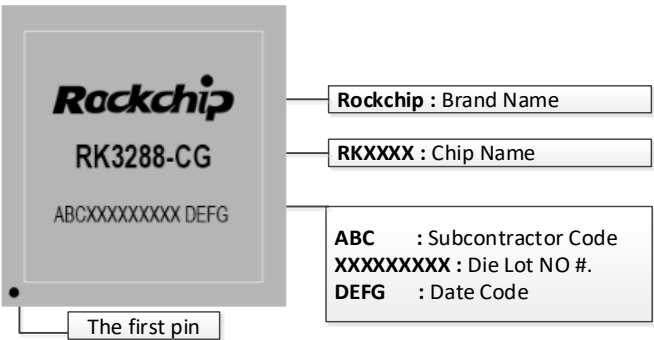


Fig. 2-5 RK3288-CG Silk Marking

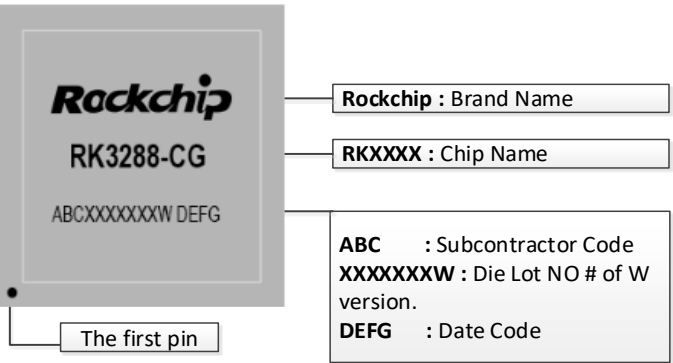


Fig. 2-6 RK3288-CG W Version Silk Marking

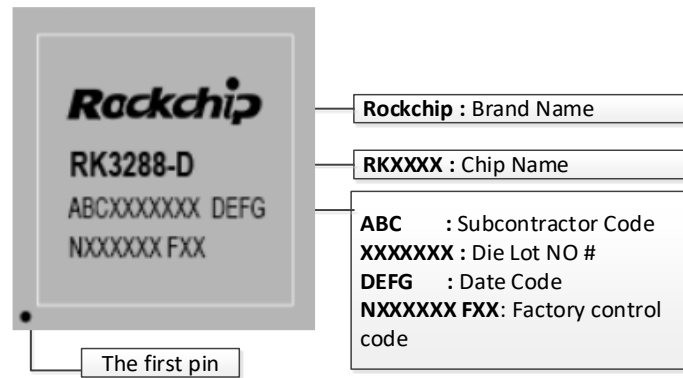


Fig. 2-7 RK3288-D Version Silk Marking

2.3 Dimension

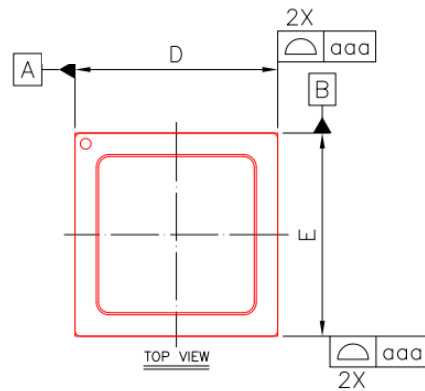


Fig. 2-8 FCBGA636LD Package Top View

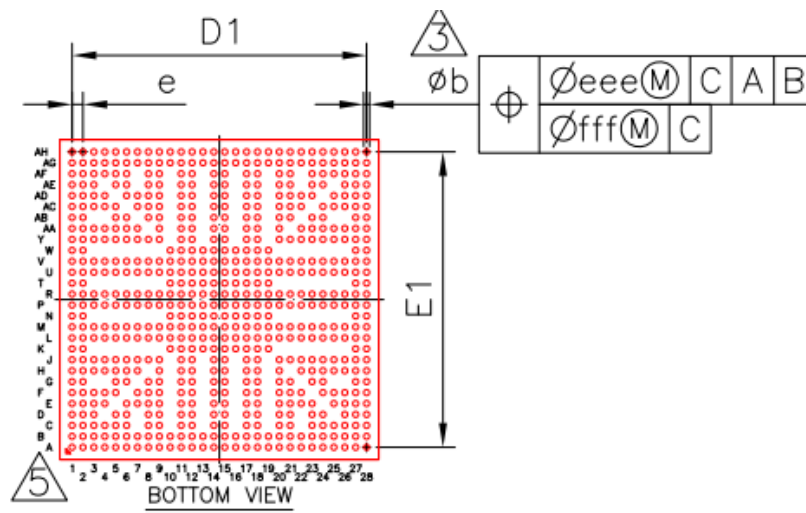
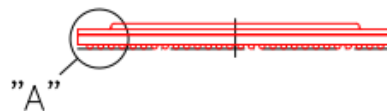


Fig. 2-9 FCBGA636LD Package Bottom View



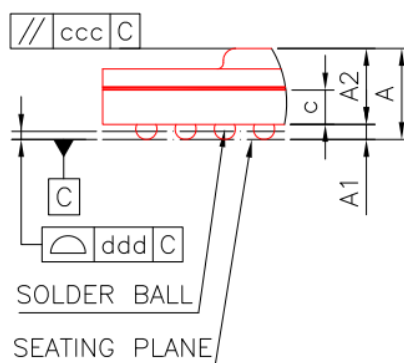


Fig. 2-10 FCBGA636LD Package Side View

| Symbol | Dimension in mm | | | Dimension in inch | | |
|--------|-----------------|-------|-------|-------------------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.41 | 1.51 | 1.61 | 0.056 | 0.059 | 0.063 |
| A1 | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| A2 | 1.21 | 1.26 | 1.31 | 0.048 | 0.050 | 0.052 |
| c | 0.47 | 0.57 | 0.67 | 0.019 | 0.022 | 0.026 |
| D/E | 18.90 | 19.00 | 19.15 | 0.744 | 0.748 | 0.754 |
| D1/E1 | --- | 17.55 | --- | --- | 0.691 | --- |
| e | --- | 0.65 | --- | --- | 0.026 | --- |
| b | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| aaa | 0.20 | | | 0.008 | | |
| ccc | 0.25 | | | 0.010 | | |
| ddd | 0.20 | | | 0.008 | | |
| eee | 0.25 | | | 0.010 | | |
| fff | 0.10 | | | 0.004 | | |

Fig. 2-11 FCBGA636LD Package Dimension

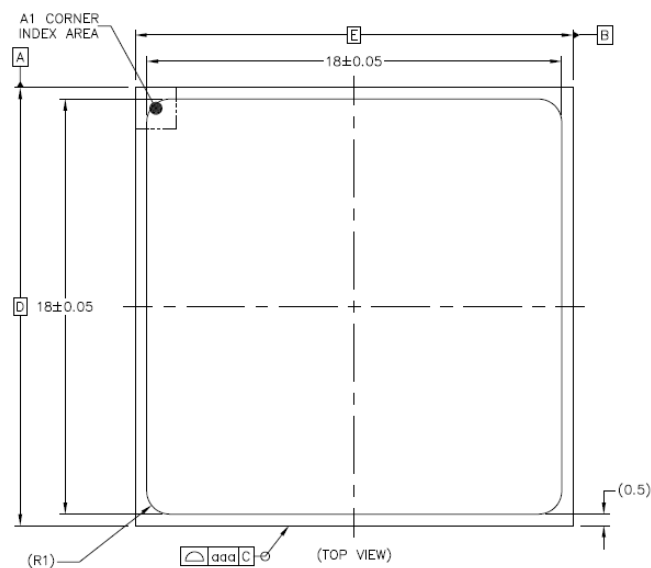


Fig. 2-12 RK3288 FCCSP636LD Package Top View--EOL

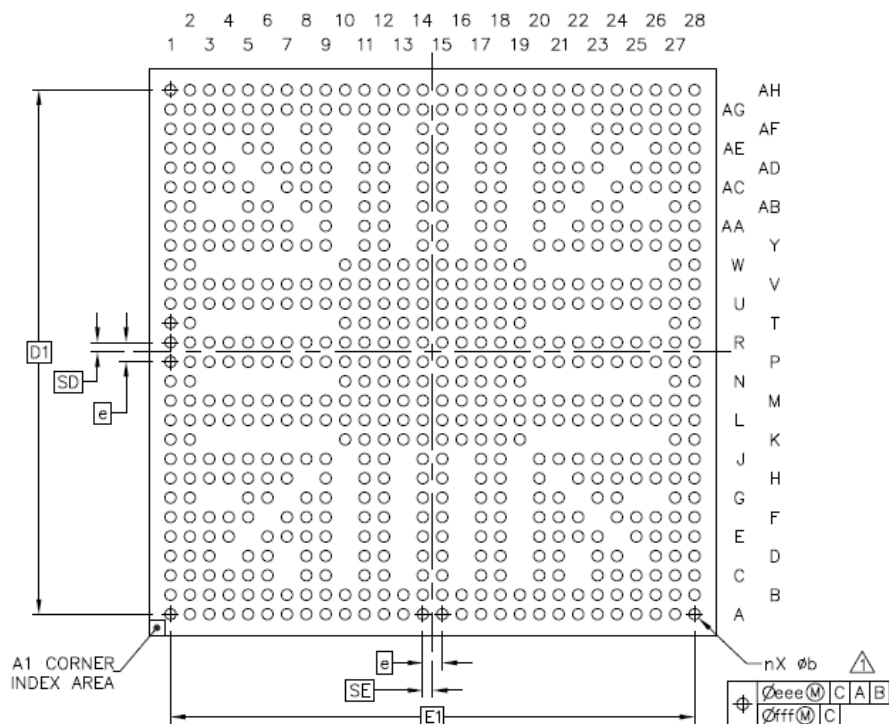


Fig. 2-13 RK3288 FCCSP636LD Package Bottom View-EOL

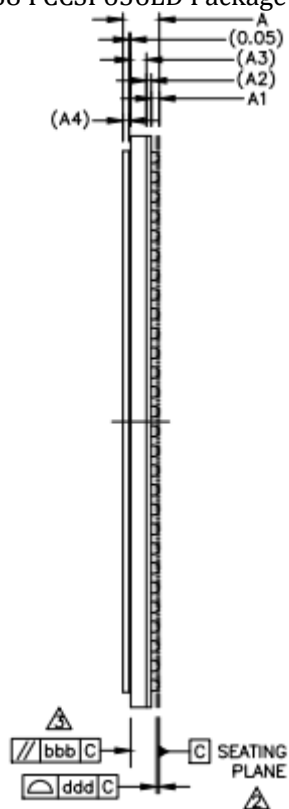


Fig. 2-14 RK3288 FCCSP636LD Package Side View-EOL

| | SYMBOL | COMMON DIMENSIONS | | |
|-----------------------------|--------|-------------------|------|------|
| | | MIN. | NOR. | MAX. |
| TOTAL THICKNESS | A | 1.1 | --- | 1.3 |
| STAND OFF | A1 | 0.22 | --- | 0.32 |
| SUBSTRATE THICKNESS | A2 | 0.15 | | REF |
| MOLD THICKNESS | A3 | 0.53 | | REF |
| HEAT SINK THICKNESS | A4 | 0.2 | | REF |
| BODY SIZE | D | 19 | | BSC |
| | E | 19 | | BSC |
| BALL DIAMETER | | 0.35 | | |
| BALL OPENING | | 0.3 | | |
| BALL WIDTH | b | 0.32 | --- | 0.42 |
| BALL PITCH | e | 0.65 | | BSC |
| BALL COUNT | n | 636 | | |
| EDGE BALL CENTER TO CENTER | D1 | 17.55 | | BSC |
| | E1 | 17.55 | | BSC |
| BODY CENTER TO CONTACT BALL | SD | 0.325 | | BSC |
| | SE | 0.325 | | BSC |
| PACKAGE EDGE TOLERANCE | aaa | 0.15 | | |
| FLATNESS | bbb | 0.2 | | |
| COPLANARITY | ddd | 0.1 | | |
| BALL OFFSET (PACKAGE) | eee | 0.15 | | |
| BALL OFFSET (BALL) | fff | 0.08 | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

Fig. 2-15 RK3288 FCCSP636LD Package Dimension-EOL

2.4 Ball Map

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | |
|----|--|--|---|--|---|--|---|---------------------------------|---------------------------------|----|
| A | DDR0_DQ25 | DDR0_DQ24 | DDR0_DQ10 | DDR0_DQS3N | DDR0_DQ9 | DDR0_DQ13 | DDR0_DQS1N | DDR0_CASN | DDR0_BA1 | A |
| B | DDR1_DQ24 | DDR1_DQ25 | DDR0_DM3 | DDR0_DQS3 | DDR0_DQ8 | DDR0_DQ14 | DDR0_DQS1 | DDR0_CS0N | DDR0_WEN | B |
| C | DDR1_DQ10 | DDR1_DQ30 | VSS1 | DDR0_DQ30 | DDR0_DQ28 | DDR0_DQ11 | NP | DDR0_CKE1 | DDR0_CKE0 | C |
| D | DDR1_DQS3N | DDR1_DQS3 | DDR1_DM3 | | DDR0_DQ26 | VSS2 | NP | DDR0_BA0 | VSS3 | D |
| E | DDR1_DQ9 | DDR1_DQ8 | DDR1_DQ28 | DDR1_DQ26 | NP | DDR0_DQ27 | DDR0_DQ31 | DDR0_DQ12 | DDR0_RESET | E |
| F | DDR1_CKE0 | DDR1_RESET | DDR1_DQ11 | VSS12 | DDR1_DQ29 | NP | DDR0_DQ29 | DDR0_DQ15 | DDR0_DM1 | F |
| G | DDR1_DQS1N | DDR1_DQS1 | NP | NP | DDR1_DM1 | DDR1_DQ27 | NP | DDR0_RETLE | NC/Reserve0 | G |
| H | DDR1_CASN | DDR1_CS0N | DDR1_CKE1 | DDR1_DQ13 | DDR1_DQ12 | DDR1_DQ31 | DDR1_RETLE | NP | DDR0_VDD1 | H |
| J | DDR1_BA1 | DDR1_WEN | DDR1_CS1N | VSS13 | DDR1_DQ14 | DDR1_DQ15 | NC/Reserve1 | DDR1_VDD1 | VSS14 | J |
| K | DDR1_A2 | DDR1_A1 | NP | NP | NP | NP | NP | NP | NP | K |
| L | DDR1_KV | DDR1_CK | DDR1_A0 | DDR1_BA0 | DDR1_BA2 | DDR1_RASN | NC/DDR1_ACTN | DDR1_VREFAO | DDR1_VDD2 | L |
| M | DDR1_A6 | DDR1_A5 | DDR1_A7 | VSS34 | DDR1_A3 | DDR1_A4 | DDR1_ATO | DDR1_VREF | DDR1_VDD3 | M |
| N | DDR1_A8 | DDR1_A10 | NP | NP | NP | NP | NP | NP | NP | N |
| P | DDR1_A9 | DDR1_A14 | DDR1_A13 | DDR1_A11 | DDR1_ODT0 | DDR1_A12 | NC/DDR1_BG0 | DDR1_VDDAO | DDR1_VDD4 | P |
| R | DDR1_A15 | DDR1_ODT1 | DDR1_DM2 | VSS53 | DDR1_DQ19 | DDR1_DQ17 | NC/DDR1_BG1 | DDR1_DTO1 | DDR1_VDD5 | R |
| T | DDR1_DQ18 | DDR1_DQ16 | NP | NP | NP | NP | NP | NP | NP | T |
| U | DDR1_DQS2N | DDR1_DQS2 | DDR1_DQ22 | DDR1_DQ20 | DDR1_DM0 | DDR1_DQ3 | DDR1_PZQ | DDR1_DTO0 | VSS15 | U |
| V | DDR1_DQ21 | DDR1_DQ23 | DDR1_DQ1 | VSS73 | DDR1_DQ6 | FLASH1_D1/HOST_D1/ MAC_TXD3/SDIO1_D1/ GPIO3_D1 | FLASH1_CS2N/HOST_D 15/MAC_TXCLK/SDIO1_ PWREN/GPIO4_B1 | FLASH1_VDD | VSS69 | V |
| W | DDR1_DQ4 | DDR1_DQ0 | NP | NP | NP | NP | NP | NP | NP | W |
| Y | DDR1_DQ2 | DDR1_DQ5 | DDR1_DQ7 | FLASH1_D0/HOST_D0/ MAC_TXD2/SDIO1_D0/ GPIO3_D0 | FLASH1_WRN/HOST_D 11/MAC_MDIO/GPIO4_ A5 | FLASH0_RDN/GPIO3_B 2 | FLASH0_CS3/EMMC_ RSTNOUT/GPIO3_C1 | GPIO3_C3/FLASH0_VOL TAGE_SEL | FLASH0_VDD | Y |
| AA | DDR1_DQS0N | DDR1_DQS0 | FLASH1_D6/HOST_D6/ MAC_RXD0/SDIO1_BKP WR/GPIO3_D6 | FLASH1_D7/HOST_D7/ MAC_RXD1/SDIO1_INT N/GPIO3_D7 | FLASH1_DQS/HOST_D1 4/MAC_COL/FLASH1_ CSN3/GPIO4_B0 | FLASH1_CS1N/HOST_D 13/MAC_CR5/SDIO1_CL KOUT/GPIO4_A7 | UART1_TX/TS0_D1/GPI O5_B1 | NP | TS0_VALID/GPIO5_C1 | AA |
| AB | FLASH1_D2/HOST_D2/ MAC_RXD2/SDIO1_D2/ GPIO3_D2 | FLASH1_D5/HOST_D5/ MAC_TXD1/SDIO1_WR PRT/GPIO3_D5 | NP | NP | FLASH1_CS0N/HOST_ D12/MAC_RXCLK/SDI O1_CMD/GPIO4_A6 | FLASH0_DQS/EMMC_C LKOUT/GPIO3_C2 | NP | TS0_ERR/GPIO5_C3 | SDMMC0_D3/JTAG_TC K/GPIO6_C3 | AB |
| AC | FLASH1_D3/HOST_D3/ MAC_RXD3/SDIO1_D3/ GPIO3_D3 | FLASH1_WP/HOST_CK OUTN/MAC_RXDV/FLA SH0_CS4/GPIO4_A1 | FLASH1_RDY/HOST_CK OUTP/MAC_MDC/GPIO 4_A0 | FLASH0_CS2N/EMMC_ CMD/GPIO3_C0 | FLASH0_CS0N/GPIO3_B 6 | NP | SPIO_CS0N/TS0_D5/UA RT4_RTSN/GPIO5_B5 | SDMMC0_CMD/GPIO6_ C5 | SDMMC0_VDD | AC |
| AD | FLASH1_D4/HOST_D4/ MAC_TXD0/SDIO1_DET /GPIO3_D4 | FLASH1_CLE/HOST_D10 /MAC_TXEN/FLASH0_C SN7/GPIO4_A4 | FLASH0_D1/EMMC_D1/ GPIO3_A1 | FLASH0_CS1N/GPIO3_B 7 | NP | UART1_RTSN/TS0_D3/ GPIO5_B3 | SPIO_CLK/TS0_D4/UAR T4_CTSN/GPIO5_B4 | SDMMC0_D2/JTAG_TDI /GPIO6_C2 | GPIO4_D7 | AD |
| AE | FLASH1_RDN/HOST_D8 /MAC_RXER/FLASH0_C SN5/GPIO4_A2 | FLASH1_ALE/HOST_D9/ MAC_CLK/FLASH0_CS N6/GPIO4_A3 | FLASH0_D0/EMMC_D0/ GPIO3_A0 | NP | SPIO_TXD/TS0_D6/UAR T4_TX/GPIO5_B6 | TS0_CLK/GPIO5_C2 | NP | SDIO0_INTN/GPIO4_D6 | SDIO0_WRPRT/GPIO4_ D3 | AE |
| AF | FLASH0_D3/EMMC_D3 /GPIO3_A3 | FLASH0_D4/EMMC_D4 /GPIO3_A4 | FLASH0_D2/EMMC_D2/ GPIO3_A2 | FLASH0_ALE/GPIO3_B3 | UART1_RX/TS0_D0/GPI O5_B0 | SPIO_RXD/TS0_D7/UAR T4_RX/GPIO5_B7 | NP | SDIO0_BKPWR/GPIO4_ D5 | SDIO0_DET/GPIO4_D2 | AF |
| AG | FLASH0_D6/EMMC_D6 /GPIO3_A6 | FLASH0_D7/EMMC_D7 /GPIO3_A7 | FLASH0_D5/EMMC_D5/ GPIO3_A5 | FLASH0_WRN/GPIO3_B 5 | SPIO_CS1N/TS0_SYNC/ GPIO5_C0 | SDMMC0_CLKOUT/JTA G_TDO/GPIO6_C4 | SDMMC0_D0/JTAG_TM S/GPIO6_C0 | SDIO0_CLKOUT/GPIO4_ D1 | SDIO0_D2/GPIO4_C6 | AG |
| AH | FLASH0_WP/EMMC_P WREN/GPIO3_B1 | FLASH0_RDY/GPIO3_B0 | FLASH0_CLE/GPIO3_B4 | UART1_CTSN/TS0_D2/ GPIO5_B2 | SDMMC0_DECTN/GPIO 6_C6 | SDMMC0_D1/JTAG_TR STN/GPIO6_C1 | SDIO0_D3/GPIO4_C7 | SDIO0_CMD/GPIO4_D0 | SDIO0_D0/GPIO4_C4 | AH |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | |

| | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | |
|----|-------------------|----------------------|--------------------------|-------------------|----------------------|--------------------|-----------|-----------------------------|--------------------|------------|----|
| A | DDR0_A2 | DDR0_CKN | DDR0_A7 | DDR0_A10 | DDR0_A9 | DDR0_DM2 | DDR0_DQ17 | DDR0_DQS2N | DDR0_DQ23 | DDR0_DQ4 | A |
| B | DDR0_A0 | DDR0_CK | DDR0_A5 | DDR0_A8 | DDR0_A14 | DDR0_DQ16 | DDR0_DQ19 | DDR0_DQS2 | DDR0_DQ21 | DDR0_DQ0 | B |
| C | NP | DDR0_A1 | DDR0_A6 | NP | DDR0_A13 | DDR0_A15 | NP | DDR0_DQ22 | DDR0_DQ1 | NP | C |
| D | NP | DDR0_RASN | VSS4 | NP | DDR0_A11 | VSS5 | NP | DDR0_DQ20 | VSS6 | NP | D |
| E | NP | DDR0_BA2 | DDR0_A3 | NP | DDR0_ODT0 | DDR0_ODT1 | NP | DDR0_DM0 | DDR0_DQ5 | NP | E |
| F | NP | DDR0_CS1N | DDR0_A4 | NP | DDR0_A12 | DDR0_DQ18 | NP | DDR0_DQ2 | DDR0_DQ3 | NP | F |
| G | NP | NC/DDR0_ACTN | DDR0_ATO | NP | NC/DDR0_BG0 | NC/DDR0_BG1 | NP | DDR0_PZQ | USB_AVDD_1V0 | NP | G |
| H | NP | DDR0_VREFAO | DDR0_VREF | NP | DDR0_VDDAO | DDR0_DTO1 | NP | DDR0_DTO0 | USB_AVSS1 | NP | H |
| J | NP | DDR0_VDD2 | DDR0_VDD3 | NP | DDR0_VDD4 | DDR0_VDD5 | NP | VSS16 | VSS28 | NP | J |
| K | VSS18 | VSS19 | VSS20 | VSS21 | VSS22 | VSS23 | VSS24 | VSS25 | VSS26 | VSS27 | K |
| L | VSS29 | VSS30 | LOGIC_VDD1 | VSS31 | VSS32 | VSS33 | GPU_VDD1 | GPU_VDD2 | GPU_VDD3 | GPU_VDD4 | L |
| M | VSS35 | VSS36 | LOGIC_VDD2 | VSS37 | VSS38 | GPU_VDD_COM | GPU_VDD7 | GPU_VDD8 | GPU_VDD9 | GPU_VDD10 | M |
| N | VSS40 | VSS41 | LOGIC_VDD3 | VSS42 | VSS43 | VSS44 | GPU_VDD5 | GPU_VDD6 | GPU_VDD11 | GPU_VDD12 | N |
| P | VSS45 | VSS46 | LOGIC_VDD4 | VSS47 | VSS48 | VSS49 | VSS50 | VSS51 | VSS52 | EFUSE_VQPS | P |
| R | VSS54 | LOGIC_VDD8 | LOGIC_VDD5 | VSS55 | VSS61 | VSS71 | VSS56 | VSS57 | VSS58 | VSS59 | R |
| T | VSS60 | LOGIC_VDD9 | LOGIC_VDD6 | VSS62 | CPU_VDD_COM | VSS64 | VSS65 | VSS66 | VSS67 | VSS68 | T |
| U | VSS70 | LOGIC_VDD10 | LOGIC_VDD7 | VSS72 | CPU_VDD1 | CPU_VDD2 | CPU_VDD3 | CPU_VDD4 | CPU_VDD5 | CPU_VDD6 | U |
| V | VSS74 | VSS75 | VSS76 | VSS77 | CPU_VDD7 | CPU_VDD8 | CPU_VDD9 | CPU_VDD10 | CPU_VDD11 | CPU_VDD12 | V |
| W | VSS17 | VSS78 | VSS79 | VSS80 | VSS81 | VSS82 | VSS83 | VSS84 | VSS85 | VSS86 | W |
| Y | NP | APIOS_VDD | APIO4_VDD | NP | NC/MIPI_LLI_AVDD_1V0 | NC/SATA_AVDD_1V0 | NP | EDP_AVDD_1V0 | VSS39 | NP | Y |
| AA | NP | APIO3_VDD | EDP_TP_OUT/SATA_R EXT | NP | NC/MIPI_LLI_AVDD_1V8 | NC/SATA_AVDD_1V8 | NP | EDP_AVDD_1V8 | HDMI_AVDD_1V0 | NP | AA |
| AB | NP | UART0_RTSN/GPIO4_C3 | UART0_CTSN/GPIO4_C2 | NP | NC/SATA_TXP | NC/SATA_TXN | NP | HDMI_REXT | HDMI_HPD | NP | AB |
| AC | NP | SDIO0_PWREN/GPIO4_D4 | I2S_CLK/GPIO6_B0 | NP | NC/SATA_RXP | NC/SATA_RXN | NP | EDP_CLK24M_IN/MIPI_LLI_REXT | EDP_REXT | NP | AC |
| AD | NP | I2S_SCLK/GPIO6_A0 | I2C2_SCL/GPIO6_B2 | NP | NC/MIPI_LLI_RX_D0P | NC/MIPI_LLI_TX_D0P | NP | NC/MIPI_LLI_RX_D1P | NC/MIPI_LLI_TX_D1P | NP | AD |
| AE | NP | I2S_SDI/GPIO6_A3 | SPDIF_TX/GPIO6_B3 | NP | NC/MIPI_LLI_RX_D0N | NC/MIPI_LLI_TX_D0N | NP | NC/MIPI_LLI_RX_D1N | NC/MIPI_LLI_TX_D1N | NP | AE |
| AF | NP | I2S_LRCK_TX/GPIO6_A2 | I2C2_SDA/GPIO6_B1 | NP | AVSS1 | AVSS2 | NP | AVSS3 | AVSS4 | NP | AF |
| AG | UART0_TX/GPIO4_C1 | I2S_LRCK_RX/GPIO6_A1 | I2S_SDO0/GPIO6_A4 | I2S_SDO2/GPIO6_A6 | EDP_TX0P | EDP_TX1P | EDP_TX2P | EDP_TX3P | EDP_AUXP | HDMI_TCP | AG |
| AH | SDIO0_D1/GPIO4_C5 | UART0_RX/GPIO4_C0 | I2S_SDO3/GPIO6_A7 | I2S_SDO1/GPIO6_A5 | EDP_TX0N | EDP_TX1N | EDP_TX2N | EDP_TX3N | EDP_AUXN | HDMI_TCN | AH |
| | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | |

| | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | |
|----|------------------|---|---|--|---|--|---------------------------------------|---|--|----|
| A | DDR0_DQ50 | VSS9 | HOST2_DM | HOST1_DM | NC/OTG_SUPER_RXM | NC/OTG_SUPER_TXM | OTG_DM | USIC_DATA | I2C1_SDA/SC_RST/GPI O8_A4 | A |
| B | DDR0_DQ50N | USB_AVSS4 | HOST2_DP | HOST1_DP | NC/OTG_SUPER_RXP | NC/OTG_SUPER_TXP | OTG_DP | USIC_STROBE | SPI2_CSN1/SC_IO/GPIO 8_A3 | B |
| C | DDR0_DQ6 | HOST2_TXRTUNE | NP | HOST1_TXRTUNE | USB_AVSS2 | OTG_ID | USB_AVSS3 | PS2_DATA/GPIO8_A1 | SPI2_TXD/SC_CLK_T1/ GPIO8_B1 | C |
| D | DDR0_DQ7 | OTG_TXRTUNE | NP | OTG_VBUS | PS2_CLK/GPIO8_A0 | NP | SPI2_CLK/SC_IO_T1/GP IO8_A6 | SPI2_CSN0/SC_DET_T1 /GPIO8_A7 | GPIO7_A2 | D |
| E | VSS7 | USB_AVDD_1V8 | BS_JTAG_TRSTN | BS_JTAG_TCK | NP | I2C1_SCL/SC_CLK/GPIO 8_A5 | GPIO7_A4 | UART3_RX/GPS_MAG/ HSADC_D0_T1/GPIO7_ A7 | EDP_HOTPLUG/GPIO7_ B3 | E |
| F | USB_AVDD_3V3 | BS_JTAG_TDI | BS_JTAG_TDO | NP | SPI2_RXD/SC_RST_T1/ GPIO8_B0 | GPIO7_A3 | GPIO7_A6 | UART3_RTSN/GPIO7_B 2 | ISP_PRELIGHTTRIG/SPI 1_RXD/GPIO7_B6 | F |
| G | BS_JTAG_TMS | GPIO8_A2/SC_DET | NP | PWM1/GPIO7_A1 | GPIO7_A5 | NP | NP | ISP_SHUTTERTRIG/SPI1 _TXD/GPIO7_B7 | ISP_FLASHTRIGIN/EDP HDMI_CEC_T1/GPIO7_ C0 | G |
| H | USIC_AVDD_1V2 | NP | PWM0/GPIO7_A0 | UART3_CTSN/GPS_RFC LK/GPS_CLK_T1/GPIO7 _B1 | ISP_FLASHTRIGOUT/SPI 1_CSN0/GPIO7_B5 | I2C4_SDA/GPIO7_C1 | I2C5_SDA/EDPHDMI_I2 C_SDA/GPIO7_C3 | GPIO7_C5 | UART2_TX/IR_TX/PWM 3/EDPHDMI_CEC/GPIO 7_C7 | H |
| J | APIO2_VDD | UART3_TX/GPS_SIG/HS ADC_D1_T1/GPIO7_B0 | ISP_SHUTTEREN/SPI1_ CLK/GPIO7_B4 | I2C4_SCL/GPIO7_C2 | I2C5_SCL/EDPHDMI_I2 C_SCL/GPIO7_C4 | UART2_RX/IR_RX/PW M2/GPIO7_C6 | PMUGPIO0_A2/DDRIO 0_RETEN | PMUGPIO0_A1/DDRIO _PWROFF | PMUGPIO0_A0/GLOBA L_PWROFF | J |
| K | NP | NP | NP | NP | NP | NP | NP | PMUGPIO0_A3/DDRIO 1_RETEN | PMUGPIO0_A4 | K |
| L | APIO1_VDD | PMUGPIO0_A5 | PMUGPIO0_A6 | PMUGPIO0_A7 | PMUGPIO0_B0 | PMUGPIO0_B1 | PMUGPIO0_B2/OTP_O UT | PMUGPIO0_B3 | PMUGPIO0_B5/CLK27 M_IN | L |
| M | PMU_VDD_1V0 | PMUGPIO0_C0/I2CO_S CL | PMUGPIO0_B6 | PMUGPIO0_C1/TEST_C LKOUT/CLK_27M_T1 | PMUGPIO0_C2 | PMUGPIO0_B7/I2CO_S DA | TEST | NPOR | PMUGPIO0_B4 | M |
| N | NP | NP | NP | NP | NP | NP | NP | OSC_XI | OSC_XO | N |
| P | PUMIO_VDD | ADC_IN1 | I2C3_SCL/GPIO2_C0 | ADC_IN2 | ADC_IN0 | CLK32K | XVSS | PLL_AVSS | PLL_AVDD_1V0 | P |
| R | ADC_AVDD_1V8 | CIF_D11/GPIO2_B7 | CIF_CLKOUT/HOST_WK REQ/TS_FAIL/GPIO2_B 3 | I2C3_SDA/GPIO2_C1 | CIF_D10/GPIO2_B6 | CIF_VSYNC/HOST_D6/T S_SYNC/GPIO2_B0 | CIF_D1/GPIO2_B5 | CIF_D0/GPIO2_B4 | CIF_HREF/HOST_D7/TS _VALID/GPIO2_B1 | R |
| T | NP | NP | NP | NP | NP | NP | NP | LCDC0_D0/LVDS_D0P/ TRACE_D0 | LCDC0_D1/LVDS_D0N/ TRACE_D1 | T |
| U | DVPIO_VDD | CIF_D7/HOST_CKINN/T S_D5/GPIO2_A5 | CIF_D6/HOST_CKINP/T S_D4/GPIO2_A4 | CIF_D8/HOST_D4/TS_D 6/GPIO2_A6 | VSS8 | LCDC0_D12/LVDS_D5P /TRACE_D12 | LCDC0_D13/LVDS_D5N /TRACE_D13 | LCDC0_D2/LVDS_D1P/ TRACE_D2 | LCDC0_D3/LVDS_D1N/ TRACE_D3 | U |
| V | LCDC_VDD | CIF_D5/HOST_D3/TS_D 3/GPIO2_A3 | CIF_CLKIN/HOST_WKA CK/GPS_CLK/TS_CLKOU T/GPIO2_B2 | CIF_D9/HOST_D5/TS_D 7/GPIO2_A7 | LVDS_RBIA5 | LCDC0_D14/LVDS_D6P /TRACE_D14 | LCDC0_D15/LVDS_D6N /TRACE_D15 | LCDC0_D10/LVDS_CLK OP/TRACE_D10 | LCDC0_D11/LVDS_CLK ON/TRACE_D11 | V |
| W | NP | NP | NP | NP | NP | NP | NP | LCDC0_D4/LVDS_D2P/ TRACE_D4 | LCDC0_D5/LVDS_D2N/ TRACE_D5 | W |
| Y | VSS63 | CIF_D3/HOST_D1/TS_D 1/GPIO2_A1 | CIF_D4/HOST_D2/TS_D 2/GPIO2_A2 | CIF_D2/HOST_D0/TS_D 0/GPIO2_A0 | VSS10 | LCDC0_D22/LVDS_CLK 1P | LCDC0_D23/LVDS_CLK 1N | LCDC0_D6/LVDS_D3P/ TRACE_D6 | LCDC0_D7/LVDS_D3N/ TRACE_D7 | Y |
| AA | LVDS_AVDD_1V0 | NP | LCDC0_DEN/GPIO1_D2 | LCDC0_HSYNC/GPIO1_ D0 | LCDC0_DCLK/GPIO1_D 3 | LCDC0_D16/LVDS_D7P /TRACE_CLK | LCDC0_D17/LVDS_D7N /TRACE_CTL | LCDC0_D8/LVDS_D4P/ TRACE_D8 | LCDC0_D9/LVDS_D4N/ TRACE_D9 | AA |
| AB | HDMI_AVDD_1V8 | LVDS_AVDD_1V8 | NP | LVDS_AVDD_3V3 | LCDC0_VSYNC/GPIO1_ D1 | NP | NP | LCDC0_D18/LVDS_D8P | LCDC0_D19/LVDS_D8N | AB |
| AC | MIPI_RX_AVDD_1V8 | MIPI_TX/RX_AVDD_1V 8 | MIPI_TX_AVDD_1V8 | NP | VSS11 | LCDC0_D20/LVDS_D9P | LCDC0_D21/LVDS_D9N | MIPI_TX_D3P | MIPI_TX_D3N | AC |
| AD | AVSS5 | MIPI_RX_REXT | MIPI_TX/RX_REXT | AVSS6 | NP | MIPI_TX/RX_D3N | AVSS7 | MIPI_TX_D2P | MIPI_TX_D2N | AD |
| AE | MIPI_TX/RX_D0P | MIPI_TX/RX_D1P | NP | MIPI_TX/RX_CLKP | MIPI_TX/RX_D2P | NP | MIPI_TX_REXT | MIPI_TX_CLKP | MIPI_TX_CLKN | AE |
| AF | MIPI_TX/RX_D0N | MIPI_TX/RX_D1N | NP | MIPI_TX/RX_CLKN | MIPI_TX/RX_D2N | MIPI_TX/RX_D3P | AVSS8 | MIPI_TX_D1P | MIPI_TX_D1N | AF |
| AG | HDMI_TX0P | HDMI_TX1P | HDMI_TX2P | MIPI_RX_D0P | MIPI_RX_D1P | MIPI_RX_CLKP | MIPI_RX_D2P | MIPI_TX_D0P | MIPI_TX_D0N | AG |
| AH | HDMI_TX0N | HDMI_TX1N | HDMI_TX2N | MIPI_RX_D0N | MIPI_RX_D1N | MIPI_RX_CLKN | MIPI_RX_D2N | MIPI_RX_D3N | MIPI_RX_D3P | AH |
| | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | |

Fig. 2-16 RK3288 Ball Mapping Diagram

2.5 Ball Pin Number Order

Table 2-1 RK3288 Ball Pin Number Order Information

| | | | |
|-----|--------------------------|-----|--------------------------|
| A1 | DDR0_DQ25 | B1 | DDR1_DQ24 |
| A2 | DDR0_DQ24 | B2 | DDR1_DQ25 |
| A3 | DDR0_DQ10 | B3 | DDR0_DM3 |
| A4 | DDR0_DQS3N | B4 | DDR0_DQS3 |
| A5 | DDR0_DQ9 | B5 | DDR0_DQ8 |
| A6 | DDR0_DQ13 | B6 | DDR0_DQ14 |
| A7 | DDR0_DQS1N | B7 | DDR0_DQS1 |
| A8 | DDR0_CASN | B8 | DDR0_CS0N |
| A9 | DDR0_BA1 | B9 | DDR0_WEN |
| A10 | DDR0_A2 | B10 | DDR0_A0 |
| A11 | DDR0_CKN | B11 | DDR0_CK |
| A12 | DDR0_A7 | B12 | DDR0_A5 |
| A13 | DDR0_A10 | B13 | DDR0_A8 |
| A14 | DDR0_A9 | B14 | DDR0_A14 |
| A15 | DDR0_DM2 | B15 | DDR0_DQ16 |
| A16 | DDR0_DQ17 | B16 | DDR0_DQ19 |
| A17 | DDR0_DQS2N | B17 | DDR0_DQS2 |
| A18 | DDR0_DQ23 | B18 | DDR0_DQ21 |
| A19 | DDR0_DQ4 | B19 | DDR0_DQ0 |
| A20 | DDR0_DQS0 | B20 | DDR0_DQS0N |
| A21 | VSS | B21 | USB_AVSS |
| A22 | HOST2_DM | B22 | HOST2_DP |
| A23 | HOST1_DM | B23 | HOST1_DP |
| A24 | NC | B24 | NC |
| A25 | NC | B25 | NC |
| A26 | OTG_DM | B26 | OTG_DP |
| A27 | USIC_DATA | B27 | USIC_STROBE |
| A28 | I2C1_SDA/SC_RST/GPIO8_A4 | B28 | SPI2_CSN1/SC_IO/GPIO8_A3 |
| C1 | DDR1_DQ10 | D1 | DDR1_DQS3N |
| C2 | DDR1_DQ30 | D2 | DDR1_DQS3 |
| C3 | VSS | D3 | DDR1_DM3 |
| C4 | DDR0_DQ30 | D4 | NC |
| C5 | DDR0_DQ28 | D5 | DDR0_DQ26 |
| C6 | DDR0_DQ11 | D6 | VSS |
| C7 | NC | D7 | NC |
| C8 | DDR0_CKE1 | D8 | DDR0_BA0 |
| C9 | DDR0_CKE0 | D9 | VSS |
| C10 | NC | D10 | NC |
| C11 | DDR0_A1 | D11 | DDR0_RASN |
| C12 | DDR0_A6 | D12 | VSS |
| C13 | NC | D13 | NC |

| | | | |
|-----|---|-----|--|
| C14 | DDR0_A13 | D14 | DDR0_A11 |
| C15 | DDR0_A15 | D15 | VSS |
| C16 | NC | D16 | NC |
| C17 | DDR0_DQ22 | D17 | DDR0_DQ20 |
| C18 | DDR0_DQ1 | D18 | VSS |
| C19 | NC | D19 | NC |
| C20 | DDR0_DQ6 | D20 | DDR0_DQ7 |
| C21 | HOST2_TXRTUNE | D21 | OTG_TXRTUNE |
| C22 | NC | D22 | NC |
| C23 | HOST1_TXRTUNE | D23 | OTG_VBUS |
| C24 | USB_AVSS | D24 | PS2_CLK/GPIO8_A0 |
| C25 | OTG_ID | D25 | NC |
| C26 | USB_AVSS | D26 | SPI2_CLK/SC_IO_T1/GPIO8_A6 |
| C27 | PS2_DATA/GPIO8_A1 | D27 | SPI2_CSN0/SC_DET_T1/GPIO8_A7 |
| C28 | SPI2_TXD/SC_CLK_T1/GPIO8_B1 | D28 | GPIO7_A2 |
| E1 | DDR1_DQ9 | F1 | DDR1_CKE0 |
| E2 | DDR1_DQ8 | F2 | DDR1_RESET |
| E3 | DDR1_DQ28 | F3 | DDR1_DQ11 |
| E4 | DDR1_DQ26 | F4 | VSS |
| E5 | NC | F5 | DDR1_DQ29 |
| E6 | DDR0_DQ27 | F6 | NC |
| E7 | DDR0_DQ31 | F7 | DDR0_DQ29 |
| E8 | DDR0_DQ12 | F8 | DDR0_DQ15 |
| E9 | DDR0_RESET | F9 | DDR0_DM1 |
| E10 | NC | F10 | NC |
| E11 | DDR0_BA2 | F11 | DDR0_CS1N |
| E12 | DDR0_A3 | F12 | DDR0_A4 |
| E13 | NC | F13 | NC |
| E14 | DDR0_ODT0 | F14 | DDR0_A12 |
| E15 | DDR0_ODT1 | F15 | DDR0_DQ18 |
| E16 | NC | F16 | NC |
| E17 | DDR0_DM0 | F17 | DDR0_DQ2 |
| E18 | DDR0_DQ5 | F18 | DDR0_DQ3 |
| E19 | NC | F19 | NC |
| E20 | VSS | F20 | USB_AVDD_3V3 |
| E21 | USB_AVDD_1V8 | F21 | BS_JTAG_TDI |
| E22 | BS_JTAG_TRSTN | F22 | BS_JTAG_TDO |
| E23 | BS_JTAG_TCK | F23 | NC |
| E24 | NC | F24 | SPI2_RXD/SC_RST_T1/GPIO8_B0 |
| E25 | I2C1_SCL/SC_CLK/GPIO8_A5 | F25 | GPIO7_A3 |
| E26 | GPIO7_A4 | F26 | GPIO7_A6 |
| E27 | UART3_RX/GPS_MAG/HSADC_D0_T1/ GPIO7_A7 | F27 | UART3_RTSN/GPIO7_B2 |
| E28 | EDP_HOTPLUG/GPIO7_B3 | F28 | ISP_PRELIGHTTRIG/SPI1_RXD/GPIO 7_B6 |

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|-----|---|-----|--|
| G1 | DDR1_DQS1N | H1 | DDR1_CASN |
| G2 | DDR1_DQS1 | H2 | DDR1_CS0N |
| G3 | NC | H3 | DDR1_CKE1 |
| G4 | NC | H4 | DDR1_DQ13 |
| G5 | DDR1_DM1 | H5 | DDR1_DQ12 |
| G6 | DDR1_DQ27 | H6 | DDR1_DQ31 |
| G7 | NC | H7 | DDR1_RETLE |
| G8 | DDR0_RETLE | H8 | NC |
| G9 | NC | H9 | DDR0_VDD |
| G10 | NC | H10 | NC |
| G11 | NC | H11 | DDR0_VREFAO |
| G12 | DDR0_ATO | H12 | DDR0_VREF |
| G13 | NC | H13 | NC |
| G14 | NC | H14 | DDR0_VDDAO |
| G15 | NC | H15 | DDR0_DTO1 |
| G16 | NC | H16 | NC |
| G17 | DDR0_PZQ | H17 | DDR0_DTO0 |
| G18 | USB_AVDD_1V0 | H18 | USB_AVSS |
| G19 | NC | H19 | NC |
| G20 | BS_JTAG_TMS | H20 | USIC_AVDD_1V2 |
| G21 | GPIO8_A2/SC_DET | H21 | NC |
| G22 | NC | H22 | PWM0/GPIO7_A0 |
| G23 | PWM1/GPIO7_A1 | H23 | UART3_CTSN/GPS_RFCLK/GPS_CLK_T1/GPIO7_B1 |
| G24 | GPIO7_A5 | H24 | ISP_FLASHTRIGOUT/SPI1_CSN0/GPIO7_B5 |
| G25 | NC | H25 | I2C4_SDA/GPIO7_C1 |
| G26 | NC | H26 | I2C5_SDA/EDPHDMI_I2C_SDA/GPIO7_C3 |
| G27 | ISP_SHUTTERTRIG/SPI1_TXD/GPIO7_B7 | H27 | GPIO7_C5 |
| G28 | ISP_FLASHTRIGIN/EDPHDMI_CEC_T1/GPIO7_C0 | H28 | UART2_TX/IR_TX/PWM3/EDPHDMI_CEC/GPIO7_C7 |
| J1 | DDR1_BA1 | K1 | DDR1_A2 |
| J2 | DDR1_WEN | K2 | DDR1_A1 |
| J3 | DDR1_CS1N | K3 | NC |
| J4 | VSS | K4 | NC |
| J5 | DDR1_DQ14 | K5 | NC |
| J6 | DDR1_DQ15 | K6 | NC |
| J7 | NC | K7 | NC |
| J8 | DDR1_VDD | K8 | NC |
| J9 | VSS | K9 | NC |
| J10 | NC | K10 | VSS |
| J11 | DDR0_VDD | K11 | VSS |
| J12 | DDR0_VDD | K12 | VSS |

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|-----|---------------------------------------|-----|------------------------------------|
| J13 | NC | K13 | VSS |
| J14 | DDR0_VDD | K14 | VSS |
| J15 | DDR0_VDD | K15 | VSS |
| J16 | NC | K16 | VSS |
| J17 | VSS | K17 | VSS |
| J18 | VSS | K18 | VSS |
| J19 | NC | K19 | VSS |
| J20 | APIO2_VDD | K20 | NC |
| J21 | UART3_TX/GPS_SIG/HSADC_D1_T1/GPIO7_B0 | K21 | NC |
| J22 | ISP_SHUTTEREN/SPI1_CLK/GPIO7_B4 | K22 | NC |
| J23 | I2C4_SCL/GPIO7_C2 | K23 | NC |
| J24 | I2C5_SCL/EDPHDMI_I2C_SCL/GPIO7_C4 | K24 | NC |
| J25 | UART2_RX/IR_RX/PWM2/GPIO7_C6 | K25 | NC |
| J26 | PMUGPIO0_A2/DDRIO0_RETEN | K26 | NC |
| J27 | PMUGPIO0_A1/DDRIO_PWROFF | K27 | PMUGPIO0_A3/DDRIO1_RETEN |
| J28 | PMUGPIO0_A0/GLOBAL_PWROFF | K28 | PMUGPIO0_A4 |
| L1 | DDR1_CKN | M1 | DDR1_A6 |
| L2 | DDR1_CK | M2 | DDR1_A5 |
| L3 | DDR1_A0 | M3 | DDR1_A7 |
| L4 | DDR1_BA0 | M4 | VSS |
| L5 | DDR1_BA2 | M5 | DDR1_A3 |
| L6 | DDR1_RASN | M6 | DDR1_A4 |
| L7 | NC | M7 | DDR1_ATO |
| L8 | DDR1_VREFAO | M8 | DDR1_VREF |
| L9 | DDR1_VDD | M9 | DDR1_VDD |
| L10 | VSS | M10 | VSS |
| L11 | VSS | M11 | VSS |
| L12 | LOGIC_VDD | M12 | LOGIC_VDD |
| L13 | VSS | M13 | VSS |
| L14 | VSS | M14 | VSS |
| L15 | VSS | M15 | GPU_VDD |
| L16 | GPU_VDD | M16 | GPU_VDD |
| L17 | GPU_VDD | M17 | GPU_VDD |
| L18 | GPU_VDD | M18 | GPU_VDD |
| L19 | GPU_VDD | M19 | GPU_VDD |
| L20 | APIO1_VDD | M20 | PMU_VDD_1V0 |
| L21 | PMUGPIO0_A5 | M21 | PMUGPIO0_C0/I2C0_SCL |
| L22 | PMUGPIO0_A6 | M22 | PMUGPIO0_B6 |
| L23 | PMUGPIO0_A7 | M23 | PMUGPIO0_C1/TEST_CLKOUT/CLK_27M_T1 |
| L24 | PMUGPIO0_B0 | M24 | PMUGPIO0_C2 |
| L25 | PMUGPIO0_B1 | M25 | PMUGPIO0_B7/I2C0_SDA |
| L26 | PMUGPIO0_B2/OTP_OUT | M26 | TEST |

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|-----|-----------------------|-----|-------------------|
| L27 | PMUGPIO0_B3 | M27 | NPOR |
| L28 | PMUGPIO0_B5/CLK27M_IN | M28 | PMUGPIO0_B4 |
| N1 | DDR1_A8 | P1 | DDR1_A9 |
| N2 | DDR1_A10 | P2 | DDR1_A14 |
| N3 | NC | P3 | DDR1_A13 |
| N4 | NC | P4 | DDR1_A11 |
| N5 | NC | P5 | DDR1_ODT0 |
| N6 | NC | P6 | DDR1_A12 |
| N7 | NC | P7 | NC |
| N8 | NC | P8 | DDR1_VDDAO |
| N9 | NC | P9 | DDR1_VDD |
| N10 | VSS | P10 | VSS |
| N11 | VSS | P11 | VSS |
| N12 | LOGIC_VDD | P12 | LOGIC_VDD |
| N13 | VSS | P13 | VSS |
| N14 | VSS | P14 | VSS |
| N15 | VSS | P15 | VSS |
| N16 | GPU_VDD | P16 | VSS |
| N17 | GPU_VDD | P17 | VSS |
| N18 | GPU_VDD | P18 | VSS |
| N19 | GPU_VDD | P19 | EFUSE_VQPS |
| N20 | NC | P20 | PUMIO_VDD |
| N21 | NC | P21 | ADC_IN1 |
| N22 | NC | P22 | I2C3_SCL/GPIO2_C0 |
| N23 | NC | P23 | ADC_IN2 |
| N24 | NC | P24 | ADC_IN0 |
| N25 | NC | P25 | CLK32K |
| N26 | NC | P26 | VSS |
| N27 | OSC_XI | P27 | PLL_AVSS |
| N28 | OSC_XO | P28 | PLL_AVDD_1V0 |
| R1 | DDR1_A15 | T1 | DDR1_DQ18 |
| R2 | DDR1_ODT1 | T2 | DDR1_DQ16 |
| R3 | DDR1_DM2 | T3 | NC |
| R4 | VSS | T4 | NC |
| R5 | DDR1_DQ19 | T5 | NC |
| R6 | DDR1_DQ17 | T6 | NC |
| R7 | NC | T7 | NC |
| R8 | DDR1_DTO1 | T8 | NC |
| R9 | DDR1_VDD | T9 | NC |
| R10 | VSS | T10 | VSS |
| R11 | LOGIC_VDD | T11 | LOGIC_VDD |
| R12 | LOGIC_VDD | T12 | LOGIC_VDD |
| R13 | VSS | T13 | VSS |
| R14 | VSS | T14 | CPU_VDD |
| R15 | VSS | T15 | VSS |

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|-----|--|-----|---|
| R16 | VSS | T16 | VSS |
| R17 | VSS | T17 | VSS |
| R18 | VSS | T18 | VSS |
| R19 | VSS | T19 | VSS |
| R20 | ADC_AVDD_1V8 | T20 | NC |
| R21 | CIF_D11/GPIO2_B7 | T21 | NC |
| R22 | CIF_CLKOUT/HOST_WKREQ/TS_FAIL/ GPIO2_B3 | T22 | NC |
| R23 | I2C3_SDA/GPIO2_C1 | T23 | NC |
| R24 | CIF_D10/GPIO2_B6 | T24 | NC |
| R25 | CIF_VSYNC/HOST_D6/TS_SYNC/GPIO 2_B0 | T25 | NC |
| R26 | CIF_D1/GPIO2_B5 | T26 | NC |
| R27 | CIF_D0/GPIO2_B4 | T27 | LCDC0_D0/LVDS_D0P/TRACE_D0 |
| R28 | CIF_HREF/HOST_D7/TS_VALID/GPIO2 _B1 | T28 | LCDC0_D1/LVDS_D0N/TRACE_D1 |
| U1 | DDR1_DQS2N | V1 | DDR1_DQ21 |
| U2 | DDR1_DQS2 | V2 | DDR1_DQ23 |
| U3 | DDR1_DQ22 | V3 | DDR1_DQ1 |
| U4 | DDR1_DQ20 | V4 | VSS |
| U5 | DDR1_DM0 | V5 | DDR1_DQ6 |
| U6 | DDR1_DQ3 | V6 | FLASH1_D1/HOST_D1/MAC_TXD3/S DIO1_D1/GPIO3_D1 |
| U7 | DDR1_PZQ | V7 | FLASH1_CSN2/HOST_D15/MAC_TXCL K/SDIO1_PWREN/GPIO4_B1 |
| U8 | DDR1_DT00 | V8 | FLASH1_VDD |
| U9 | VSS | V9 | VSS |
| U10 | VSS | V10 | VSS |
| U11 | LOGIC_VDD | V11 | VSS |
| U12 | LOGIC_VDD | V12 | VSS |
| U13 | VSS | V13 | VSS |
| U14 | CPU_VDD | V14 | CPU_VDD |
| U15 | CPU_VDD | V15 | CPU_VDD |
| U16 | CPU_VDD | V16 | CPU_VDD |
| U17 | CPU_VDD | V17 | CPU_VDD |
| U18 | CPU_VDD | V18 | CPU_VDD |
| U19 | CPU_VDD | V19 | CPU_VDD |
| U20 | DVPIO_VDD | V20 | LCDC_VDD |
| U21 | CIF_D7/HOST_CKINN/TS_D5/GPIO2_A 5 | V21 | CIF_D5/HOST_D3/TS_D3/GPIO2_A3 |
| U22 | CIF_D6/HOST_CKINP/TS_D4/GPIO2_A 4 | V22 | CIF_CLKIN/HOST_WKACK/GPS_CLK/ TS_CLKOUT/GPIO2_B2 |
| U23 | CIF_D8/HOST_D4/TS_D6/GPIO2_A6 | V23 | CIF_D9/HOST_D5/TS_D7/GPIO2_A7 |
| U24 | VSS | V24 | LVDS_RBIAS |
| U25 | LCDC0_D12/LVDS_D5P/TRACE_D12 | V25 | LCDC0_D14/LVDS_D6P/TRACE_D14 |

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|-----|---|-----|---|
| U26 | LCDC0_D13/LVDS_D5N/TRACE_D13 | V26 | LCDC0_D15/LVDS_D6N/TRACE_D15 |
| U27 | LCDC0_D2/LVDS_D1P/TRACE_D2 | V27 | LCDC0_D10/LVDS_CLK0P/TRACE_D10 |
| U28 | LCDC0_D3/LVDS_D1N/TRACE_D3 | V28 | LCDC0_D11/LVDS_CLK0N/TRACE_D11 |
| W1 | DDR1_DQ4 | Y1 | DDR1_DQ2 |
| W2 | DDR1_DQ0 | Y2 | DDR1_DQ5 |
| W3 | NC | Y3 | DDR1_DQ7 |
| W4 | NC | Y4 | FLASH1_D0/HOST_D0/MAC_TXD2/S DIO1_D0/GPIO3_D0 |
| W5 | NC | Y5 | FLASH1_WRN/HOST_D11/MAC_CMD/ GPIO4_A5 |
| W6 | NC | Y6 | FLASH0_RDN/GPIO3_B2 |
| W7 | NC | Y7 | FLASH0_CSN3/EMMC_RSTNOUT/GPI O3_C1 |
| W8 | NC | Y8 | GPIO3_C3/FLASH0_VOLTAGE_SEL |
| W9 | NC | Y9 | FLASH0_VDD |
| W10 | VSS | Y10 | NC |
| W11 | VSS | Y11 | APIO5_VDD |
| W12 | VSS | Y12 | APIO4_VDD |
| W13 | VSS | Y13 | NC |
| W14 | VSS | Y14 | NC |
| W15 | VSS | Y15 | NC |
| W16 | VSS | Y16 | NC |
| W17 | VSS | Y17 | EDP_AVDD_1V0 |
| W18 | VSS | Y18 | VSS |
| W19 | VSS | Y19 | NC |
| W20 | NC | Y20 | VSS |
| W21 | NC | Y21 | CIF_D3/HOST_D1/TS_D1/GPIO2_A1 |
| W22 | NC | Y22 | CIF_D4/HOST_D2/TS_D2/GPIO2_A2 |
| W23 | NC | Y23 | CIF_D2/HOST_D0/TS_D0/GPIO2_A0 |
| W24 | NC | Y24 | VSS |
| W25 | NC | Y25 | LCDC0_D22/LVDS_CLK1P |
| W26 | NC | Y26 | LCDC0_D23/LVDS_CLK1N |
| W27 | LCDC0_D4/LVDS_D2P/TRACE_D4 | Y27 | LCDC0_D6/LVDS_D3P/TRACE_D6 |
| W28 | LCDC0_D5/LVDS_D2N/TRACE_D5 | Y28 | LCDC0_D7/LVDS_D3N/TRACE_D7 |
| AA1 | DDR1_DQS0N | AB1 | FLASH1_D2/HOST_D2/MAC_RXD2/S DIO1_D2/GPIO3_D2 |
| AA2 | DDR1_DQS0 | AB2 | FLASH1_D5/HOST_D5/MAC_TXD1/S DIO1_WRPRT/GPIO3_D5 |
| AA3 | FLASH1_D6/HOST_D6/MAC_RXD0/SDI O1_BKPWR/GPIO3_D6 | AB3 | NC |
| AA4 | FLASH1_D7/HOST_D7/MAC_RXD1/SDI O1_INTN/GPIO3_D7 | AB4 | NC |

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|------|---|------|---|
| AA5 | FLASH1_DQS/HOST_D14/MAC_COL/FLASH1__CSN3/GPIO4_B0 | AB5 | FLASH1_CSN0/HOST_D12/MAC_RXCLK/SDIO1_CMD/GPIO4_A6 |
| AA6 | FLASH1_CSN1/HOST_D13/MAC_CRSDIO1_CLKOUT/GPIO4_A7 | AB6 | FLASH0_DQS/EMMC_CLKOUT/GPIO3_C2 |
| AA7 | UART1_TX/TS0_D1/GPIO5_B1 | AB7 | NC |
| AA8 | NC | AB8 | TS0_ERR/GPIO5_C3 |
| AA9 | TS0_VALID/GPIO5_C1 | AB9 | SDMMC0_D3/JTAG_TCK/GPIO6_C3 |
| AA10 | NC | AB10 | NC |
| AA11 | APIO3_VDD | AB11 | UART0_RTSN/GPIO4_C3 |
| AA12 | EDP_TP_OUT/SATA_REXT | AB12 | UART0_CTSN/GPIO4_C2 |
| AA13 | NC | AB13 | NC |
| AA14 | NC | AB14 | NC |
| AA15 | NC | AB15 | NC |
| AA16 | NC | AB16 | NC |
| AA17 | EDP_AVDD_1V8 | AB17 | HDMI_REXT |
| AA18 | HDMI_AVDD_1V0 | AB18 | HDMI_HPD |
| AA19 | NC | AB19 | NC |
| AA20 | LVDS_AVDD_1V0 | AB20 | HDMI_AVDD_1V8 |
| AA21 | NC | AB21 | LVDS_AVDD_1V8 |
| AA22 | LCDC0_DEN/GPIO1_D2 | AB22 | NC |
| AA23 | LCDC0_HSYNC/GPIO1_D0 | AB23 | LVDS_AVDD_3V3 |
| AA24 | LCDC0_DCLK/GPIO1_D3 | AB24 | LCDC0_VSYNC/GPIO1_D1 |
| AA25 | LCDC0_D16/LVDS_D7P/TRACE_CLK | AB25 | NC |
| AA26 | LCDC0_D17/LVDS_D7N/TRACE_CTL | AB26 | NC |
| AA27 | LCDC0_D8/LVDS_D4P/TRACE_D8 | AB27 | LCDC0_D18/LVDS_D8P |
| AA28 | LCDC0_D9/LVDS_D4N/TRACE_D9 | AB28 | LCDC0_D19/LVDS_D8N |
| AC1 | FLASH1_D3/HOST_D3/MAC_RXD3/SDIO1_D3/GPIO3_D3 | AD1 | FLASH1_D4/HOST_D4/MAC_TXD0/SDIO1_DET/GPIO3_D4 |
| AC2 | FLASH1_WP/HOST_CKOUTN/MAC_RXDV/FLASH0_CSN4/GPIO4_A1 | AD2 | FLASH1_CLE/HOST_D10/MAC_TXEN/FLASH0_CSN7/GPIO4_A4 |
| AC3 | FLASH1_RDY/HOST_CKOUTP/MAC_MD C/GPIO4_A0 | AD3 | FLASH0_D1/EMMC_D1/GPIO3_A1 |
| AC4 | FLASH0_CSN2/EMMC_CMD/GPIO3_C0 | AD4 | FLASH0_CSN1/GPIO3_B7 |
| AC5 | FLASH0_CSN0/GPIO3_B6 | AD5 | NC |
| AC6 | NC | AD6 | UART1_RTSN/TS0_D3/GPIO5_B3 |
| AC7 | SPI0_CSN0/TS0_D5/UART4_RTSN/GPIO5_B5 | AD7 | SPI0_CLK/TS0_D4/UART4_CTSN/GPIO5_B4 |
| AC8 | SDMMC0_CMD/GPIO6_C5 | AD8 | SDMMC0_D2/JTAG_TDI/GPIO6_C2 |
| AC9 | SDMMC0_VDD | AD9 | GPIO4_D7 |
| AC10 | NC | AD10 | NC |
| AC11 | SDIO0_PWREN/GPIO4_D4 | AD11 | I2S_SCLK/GPIO6_A0 |
| AC12 | I2S_CLK/GPIO6_B0 | AD12 | I2C2_SCL/GPIO6_B2 |
| AC13 | NC | AD13 | NC |
| AC14 | NC | AD14 | NC |
| AC15 | NC | AD15 | NC |

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|------|--|------|-----------------------------------|
| AC16 | NC | AD16 | NC |
| AC17 | EDP_CLK24M_IN/MIPI_LLI_REXT | AD17 | NC |
| AC18 | EDP_REXT | AD18 | NC |
| AC19 | NC | AD19 | NC |
| AC20 | MIPI_RX_AVDD_1V8 | AD20 | AVSS |
| AC21 | MIPI_TX/RX_AVDD_1V8 | AD21 | MIPI_RX_REXT |
| AC22 | MIPI_TX_AVDD_1V8 | AD22 | MIPI_TX/RX_REXT |
| AC23 | NC | AD23 | AVSS |
| AC24 | VSS | AD24 | NC |
| AC25 | LCDC0_D20/LVDS_D9P | AD25 | MIPI_TX/RX_D3N |
| AC26 | LCDC0_D21/LVDS_D9N | AD26 | AVSS |
| AC27 | MIPI_TX_D3P | AD27 | MIPI_TX_D2P |
| AC28 | MIPI_TX_D3N | AD28 | MIPI_TX_D2N |
| AE1 | FLASH1_RDN/HOST_D8/MAC_RXER/FLASH0_CSN5/GPIO4_A2 | AF1 | FLASH0_D3/EMMC_D3/GPIO3_A3 |
| AE2 | FLASH1_ALE/HOST_D9/MAC_CLK/FLASH0_CSN6/GPIO4_A3 | AF2 | FLASH0_D4/EMMC_D4/GPIO3_A4 |
| AE3 | FLASH0_D0/EMMC_D0/GPIO3_A0 | AF3 | FLASH0_D2/EMMC_D2/GPIO3_A2 |
| AE4 | NC | AF4 | FLASH0_ALE/GPIO3_B3 |
| AE5 | SPI0_TXD/TS0_D6/UART4_TX/GPIO5_B6 | AF5 | UART1_RX/TS0_D0/GPIO5_B0 |
| AE6 | TS0_CLK/GPIO5_C2 | AF6 | SPI0_RXD/TS0_D7/UART4_RX/GPIO5_B7 |
| AE7 | NC | AF7 | NC |
| AE8 | SDIO0_INTN/GPIO4_D6 | AF8 | SDIO0_BKPWR/GPIO4_D5 |
| AE9 | SDIO0_WRPRT/GPIO4_D3 | AF9 | SDIO0_DET/GPIO4_D2 |
| AE10 | NC | AF10 | NC |
| AE11 | I2S_SDI/GPIO6_A3 | AF11 | I2S_LRCK_TX/GPIO6_A2 |
| AE12 | SPDIF_TX/GPIO6_B3 | AF12 | I2C2_SDA/GPIO6_B1 |
| AE13 | NC | AF13 | NC |
| AE14 | NC | AF14 | AVSS |
| AE15 | NC | AF15 | AVSS |
| AE16 | NC | AF16 | NC |
| AE17 | NC | AF17 | AVSS |
| AE18 | NC | AF18 | AVSS |
| AE19 | NC | AF19 | NC |
| AE20 | MIPI_TX/RX_D0P | AF20 | MIPI_TX/RX_D0N |
| AE21 | MIPI_TX/RX_D1P | AF21 | MIPI_TX/RX_D1N |
| AE22 | NC | AF22 | NC |
| AE23 | MIPI_TX/RX_CLKP | AF23 | MIPI_TX/RX_CLKN |
| AE24 | MIPI_TX/RX_D2P | AF24 | MIPI_TX/RX_D2N |
| AE25 | NC | AF25 | MIPI_TX/RX_D3P |
| AE26 | MIPI_TX_REXT | AF26 | AVSS |
| AE27 | MIPI_TX_CLKP | AF27 | MIPI_TX_D1P |
| AE28 | MIPI_TX_CLKN | AF28 | MIPI_TX_D1N |

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|------|---------------------------------|------|-------------------------------|
| AG1 | FLASH0_D6/EMMC_D6/GPIO3_A6 | AH1 | FLASH0_WP/EMMC_PWREN/GPIO3_B1 |
| AG2 | FLASH0_D7/EMMC_D7/GPIO3_A7 | AH2 | FLASH0_RDY/GPIO3_B0 |
| AG3 | FLASH0_D5/EMMC_D5/GPIO3_A5 | AH3 | FLASH0_CLE/GPIO3_B4 |
| AG4 | FLASH0_WRN/GPIO3_B5 | AH4 | UART1_CTSN/TS0_D2/GPIO5_B2 |
| AG5 | SPI0_CSN1/TS0_SYNC/GPIO5_C0 | AH5 | SDMMC0_DECTN/GPIO6_C6 |
| AG6 | SDMMC0_CLKOUT/JTAG_TDO/GPIO6_C4 | AH6 | SDMMC0_D1/JTAG_TRSTN/GPIO6_C1 |
| AG7 | SDMMC0_D0/JTAG_TMS/GPIO6_C0 | AH7 | SDIO0_D3/GPIO4_C7 |
| AG8 | SDIO0_CLKOUT/GPIO4_D1 | AH8 | SDIO0_CMD/GPIO4_D0 |
| AG9 | SDIO0_D2/GPIO4_C6 | AH9 | SDIO0_D0/GPIO4_C4 |
| AG10 | UART0_TX/GPIO4_C1 | AH10 | SDIO0_D1/GPIO4_C5 |
| AG11 | I2S_LRCK_RX/GPIO6_A1 | AH11 | UART0_RX/GPIO4_C0 |
| AG12 | I2S_SDO0/GPIO6_A4 | AH12 | I2S_SDO3/GPIO6_A7 |
| AG13 | I2S_SDO2/GPIO6_A6 | AH13 | I2S_SDO1/GPIO6_A5 |
| AG14 | EDP_TX0P | AH14 | EDP_TX0N |
| AG15 | EDP_TX1P | AH15 | EDP_TX1N |
| AG16 | EDP_TX2P | AH16 | EDP_TX2N |
| AG17 | EDP_TX3P | AH17 | EDP_TX3N |
| AG18 | EDP_AUXP | AH18 | EDP_AUXN |
| AG19 | HDMI_TCP | AH19 | HDMI_TCN |
| AG20 | HDMI_TX0P | AH20 | HDMI_TX0N |
| AG21 | HDMI_TX1P | AH21 | HDMI_TX1N |
| AG22 | HDMI_TX2P | AH22 | HDMI_TX2N |
| AG23 | MIPI_RX_D0P | AH23 | MIPI_RX_D0N |
| AG24 | MIPI_RX_D1P | AH24 | MIPI_RX_D1N |
| AG25 | MIPI_RX_CLKP | AH25 | MIPI_RX_CLKN |
| AG26 | MIPI_RX_D2P | AH26 | MIPI_RX_D2N |
| AG27 | MIPI_TX_D0P | AH27 | MIPI_RX_D3N |
| AG28 | MIPI_TX_D0N | AH28 | MIPI_RX_D3P |

2.6 Power/ground IO descriptions

Table 2-2 RK3288 Power/Ground IO information

| Group | Ball # | Descriptions |
|-----------|---|---|
| VSS | C3,D6,D9,D12,D15,D18,E20,U24,A21,Y24,AC24,F4,J4,J9,U9,J17,W10,K10,K11,K12,K13,K14,K15,K16,K17,K18,K19,J18,L10,L11,L13,L14,L15,M4,M10,M11,M13,M14,Y18,N10,N11,N13,N14,N15,P10,P11,P13,P14,P15,P16,P17,P18,R4,R10,R13,R16,R17,R18,R19,T10,R14,T13,Y20,T15,T16,T17,T18,T19,V9,U10,R15,U13,V4,V10,V11,V12,V13,W11,W12,W13,W14,W15,W16,W17,W18,W19,P26 | Internal Logic Ground and Digital IO Ground |
| CPU_VDD | U14,U15,U16,U17,U18,U19,V14,V15,V16,V17,V18,V19,T14 | Internal CPU core Power |
| LOGIC_VDD | L12,M12,N12,P12,R12,T12,U12,R11,T11,U11 | Internal Logic core Power Supply |

| Group | Ball # | Descriptions |
|---------------|---|--|
| GPU_VDD | M15,L16,L17,L18,L19,N16,N17,M16,M17,M18,M19,N18,N19 | Internal GPU core Power Supply |
| DDR0_VDDAO | H14 | DDR3 Digital IO Power Supply LPDDR2/3 Digital IO Power Supply |
| DDR1_VDDAO | P8 | DDR3 Digital IO Power Supply LPDDR2/3 Digital IO Power Supply |
| DDR0_VDD | H9,J11,J12,J14,J15 | DDR3 Digital IO Power Supply LPDDR2/3 Digital IO Power Supply |
| DDR1_VDD | J8,L9,M9,P9,R9 | DDR3 Digital IO Power Supply LPDDR2/3 Digital IO Power Supply |
| PMU_VDD_1V0 | M20 | Internal PMU Domain Logic Power Supply |
| PMUIO_VDD | P20 | PMU Domain Digital IO Power Supply |
| APIO1_VDD | L20 | GPIO30 Digital IO Power Supply |
| APIO2_VDD | J20 | GPIO1830 Digital IO Power Supply |
| LCDC_VDD | V20 | LCDC Digital IO Power Supply |
| DVPIO_VDD | U20 | DVP Digital IO Power Supply |
| FLASH0_VDD | Y9 | Nand Flash0 Digital IO Power Supply |
| FLASH1_VDD | V8 | Nand Flash1 Digital IO Power Supply |
| SDMMC0_VDD | AC9 | SDMMC0 Digital IO Power Supply |
| APIO3_VDD | AA11 | WIFI Digital IO Power Supply |
| APIO4_VDD | Y12 | AUDIO Digital IO Power Supply |
| APIO5_VDD | Y11 | BB Digital IO Power Supply |
| PLL_AVSS | P27 | PLL Analog Ground |
| PLL_AVDD_1V0 | P28 | PLL Analog Power Supply |
| ADC_AVDD_1V8 | R20 | SAR-ADC/TSADC Analog Power Supply |
| USB_AVDD_1V0 | G18 | USB OTG2.0/Host2.0 Digital Power Supply |
| USB_AVDD_1V8 | E21 | USB OTG2.0/Host2.0 Analog Power Supply |
| USB_AVDD_3V3 | F20 | USB OTG2.0/Host2.0 Analog Power Supply |
| USB_AVSS | H18,C24,C26,B21 | USB Analog Ground |
| EFUSE_VDDQ | P19 | eFuse IO Digital Power Supply |
| USIC_VDD_1V2 | H20 | USIC 1.2V Transmitter Power Supply |
| EDP_AVDD_1V0 | Y17 | eDP 1.0V Power Supply |
| EDP_AVDD_1V8 | AA17 | eDP 1.8V Power Supply |
| HDMI_AVDD_1V0 | AA18 | HDMI 1.0V Power Supply |

| Group | Ball # | Descriptions |
|--------------------|--------|----------------------------------|
| HDMI_AVDD_1V8 | AB20 | HDMI 1.8V Power Supply |
| LVDS_AVDD_1V0 | AA20 | LVDS 1.0V Power Supply |
| LVDS_AVDD_1V8 | AB21 | LVDS 1.8V Power Supply |
| LVDS_AVDD_3V3 | AB23 | LVDS 3.3V Power Supply |
| MIPI_TXRX_AVDD_1V8 | AC21 | MIPI TX/RX PHY 1.8V Power Supply |
| MIPI_TX_AVDD_1V8 | AC22 | MIPI TX PHY 1.8V Power Supply |
| MIPI_RX_AVDD_1V8 | AC20 | MIPI RX PHY 1.8V Power Supply |

2.7 Function IO description

| Pad# | Ball# | func0 | func1 | func2 | func3 | func4 | Pad type | Current | Pull | Reset State | Power Supply |
|------------------------------------|-------|---------|---------------|------------|-------------|-------|----------|---------|------|-------------|--------------|
| NPOR | M27 | npor | | | | | I | 2 | up | I | PMU |
| XIN24M | N27 | xin24m | | | | | I | 2 | NA | I | |
| XOUT24M | N28 | xout24m | | | | | O | 2 | NA | O | |
| TEST | M26 | test | | | | | I | 8 | down | I | |
| CLK32K | P25 | clk32k | | | | | I/O | 8 | down | I | |
| PMUGPIO0_A0/GLOBAL_PWROFF | J28 | gpio0a0 | global_pwroff | | | | I/O | 8 | down | I | |
| PMUGPIO0_A1/DDRIO_PWROFF | J27 | gpio0a1 | ddrio_pwroff | | | | I/O | 8 | down | I | |
| PMUGPIO0_A2/DDRIO0_RETEN | J26 | gpio0a2 | ddrio0_reten | | | | I/O | 4 | up | I | |
| PMUGPIO0_A3/DDRIO1_RETEN | K27 | gpio0a3 | ddrio1_reten | | | | I/O | 4 | up | I | |
| PMUGPIO0_A4 | K28 | gpio0a4 | | | | | I/O | 2 | up | I | |
| PMUGPIO0_A5 | L21 | gpio0a5 | | | | | I/O | 2 | up | I | |
| PMUGPIO0_A6 | L22 | gpio0a6 | | | | | I/O | 2 | up | I | |
| PMUGPIO0_A7 | L23 | gpio0a7 | | | | | I/O | 2 | up | I | |
| PMUGPIO0_B0 | L24 | gpio0b0 | | | | | I/O | 2 | up | I | |
| PMUGPIO0_B1 | L25 | gpio0b1 | | | | | I/O | 2 | up | I | |
| PMUGPIO0_B2/OTP_OUT | L26 | gpio0b2 | tsadc_int | | | | I/O | 2 | down | I | |
| PMUGPIO0_B3 | L27 | gpio0b3 | | | | | I/O | 2 | down | I | |
| PMUGPIO0_B4 | M28 | gpio0b4 | | | | | I/O | 2 | down | I | |
| PMUGPIO0_B5/CLK27M_IN | L28 | gpio0b5 | clk_27m | | | | I/O | 2 | down | I | |
| PMUGPIO0_B6 | M22 | gpio0b6 | | | | | I/O | 2 | down | I | |
| PMUGPIO0_B7/I2C0_SDA | M25 | gpio0b7 | i2c0pmu_sda | | | | I/O | 2 | up | I | |
| PMUGPIO0_C0/I2C0_SCL | M21 | gpio0c0 | i2c0pmu_scl | | | | I/O | 2 | up | I | |
| PMUGPIO0_C1/TEST_CLKOUT/CLK_27M_T1 | M23 | gpio0c1 | test_clkout | clkt1_27m | | | I/O | 4 | down | I | LCDC |
| PMUGPIO0_C2 | M24 | gpio0c2 | | | | | I/O | 2 | up | I | |
| LCDC0_HSYNC/GPIO1_D0 | AA23 | gpio1d0 | lcdc0_hsync | | | | I/O | 8 | down | I | |
| LCDC0_VSYNC/GPIO1_D1 | AB24 | gpio1d1 | lcdc0_vsync | | | | I/O | 8 | down | I | |
| LCDC0_DEN/GPIO1_D2 | AA22 | gpio1d2 | lcdc0_den | | | | I/O | 8 | down | I | DVP |
| LCDC0_DCLK/GPIO1_D3 | AA24 | gpio1d3 | lcdc0_dclk | | | | I/O | 8 | down | I | |
| CIF_D2/HOST_D0/TS_D0/GPIO2_A0 | Y23 | gpio2a0 | cif_data2 | host_din0 | hsadc_data0 | | I/O | 8 | down | I | |
| CIF_D3/HOST_D1/TS_D1/GPIO2_A1 | Y21 | gpio2a1 | cif_data3 | host_din1 | hsadc_data1 | | I/O | 8 | down | I | |
| CIF_D4/HOST_D2/TS_D2/GPIO2_A2 | Y22 | gpio2a2 | cif_data4 | host_din2 | hsadc_data2 | | I/O | 8 | down | I | |
| CIF_D5/HOST_D3/TS_D3/GPIO2_A3 | V21 | gpio2a3 | cif_data5 | host_din3 | hsadc_data3 | | I/O | 8 | down | I | DVP |
| CIF_D6/HOST_CKINP/TS_D4/GPIO2_A4 | U22 | gpio2a4 | cif_data6 | host_ckinp | hsadc_data4 | | I/O | 8 | down | I | |

| Pad# | Ball# | func0 | func1 | func2 | func3 | func4 | Pad type | Curr ent | Pull | Reset State | Power Supply |
|---|-------|---------|--------------|--------------|---------------|--------------|----------|----------|------|-------------|--------------|
| CIF_D7/HOST_CKINN/TS_D5/GPIO2_A5 | U21 | gpio2a5 | cif_data7 | host_ckinn | hsadc_data5 | | I/O | 8 | down | I | |
| CIF_D8/HOST_D4/TS_D6/GPIO2_A6 | U23 | gpio2a6 | cif_data8 | host_din4 | hsadc_data6 | | I/O | 8 | down | I | |
| CIF_D9/HOST_D5/TS_D7/GPIO2_A7 | V23 | gpio2a7 | cif_data9 | host_din5 | hsadc_data7 | | I/O | 8 | down | I | |
| CIF_VSYNC/HOST_D6/TS_SYNC/GPIO2_B0 | R25 | gpio2b0 | cif_vsync | host_din6 | hsadcts_sync | | I/O | 8 | down | I | |
| CIF_HREF/HOST_D7/TS_VALID/GPIO2_B1 | R28 | gpio2b1 | cif_href | host_din7 | hsadcts_valid | | I/O | 8 | down | I | |
| CIF_CLKIN/HOST_WKACK/GPS_CLK/TS_CLKOUT/GPIO2_B2 | V22 | gpio2b2 | cif_clk | host_wkack | gps_clk | hsadc_clkout | I/O | 8 | down | I | |
| CIF_CLKOUT/HOST_WKREQ/TS_FAIL/GPIO2_B3 | R22 | gpio2b3 | cif_clkout | host_wkreq | hsadcts_fail | | I/O | 8 | down | I | |
| CIF_D0/GPIO2_B4 | R27 | gpio2b4 | cif_data0 | | | | I/O | 8 | down | I | |
| CIF_D1/GPIO2_B5 | R26 | gpio2b5 | cif_data1 | | | | I/O | 8 | down | I | |
| CIF_D10/GPIO2_B6 | R24 | gpio2b6 | cif_data10 | | | | I/O | 8 | down | I | |
| CIF_D11/GPIO2_B7 | R21 | gpio2b7 | cif_data11 | | | | I/O | 8 | down | I | |
| I2C3_SCL/GPIO2_C0 | P22 | gpio2c0 | i2c3cam_scl | | | | I/O | 2 | up | I | |
| I2C3_SDA/GPIO2_C1 | R23 | gpio2c1 | i2c3cam_sda | | | | I/O | 2 | up | I | |
| FLASH0_D0/EMMC_D0/GPIO3_A0 | AE3 | gpio3a0 | flash0_data0 | emmc_data0 | | | I/O | 8 | up | I | FLASH 0 |
| FLASH0_D1/EMMC_D1/GPIO3_A1 | AD3 | gpio3a1 | flash0_data1 | emmc_data1 | | | I/O | 8 | up | I | |
| FLASH0_D2/EMMC_D2/GPIO3_A2 | AF3 | gpio3a2 | flash0_data2 | emmc_data2 | | | I/O | 8 | up | I | |
| FLASH0_D3/EMMC_D3/GPIO3_A3 | AF1 | gpio3a3 | flash0_data3 | emmc_data3 | | | I/O | 8 | up | I | |
| FLASH0_D4/EMMC_D4/GPIO3_A4 | AF2 | gpio3a4 | flash0_data4 | emmc_data4 | | | I/O | 8 | up | I | |
| FLASH0_D5/EMMC_D5/GPIO3_A5 | AG3 | gpio3a5 | flash0_data5 | emmc_data5 | | | I/O | 8 | up | I | |
| FLASH0_D6/EMMC_D6/GPIO3_A6 | AG1 | gpio3a6 | flash0_data6 | emmc_data6 | | | I/O | 8 | up | I | |
| FLASH0_D7/EMMC_D7/GPIO3_A7 | AG2 | gpio3a7 | flash0_data7 | emmc_data7 | | | I/O | 8 | up | I | |
| FLASH0_RDY/GPIO3_B0 | AH2 | gpio3b0 | flash0_rdy | | | | I/O | 4 | up | I | |
| FLASH0_WP/EMMC_PWREN/GPIO3_B1 | AH1 | gpio3b1 | flash0_wp | emmc_pwren | | | I/O | 4 | down | I | |
| FLASH0_RDN/GPIO3_B2 | Y6 | gpio3b2 | flash0_rdn | | | | I/O | 4 | up | I | |
| FLASH0_ALE/GPIO3_B3 | AF4 | gpio3b3 | flash0_ale | | | | I/O | 4 | down | I | |
| FLASH0_CLE/GPIO3_B4 | AH3 | gpio3b4 | flash0_cle | | | | I/O | 4 | down | I | |
| FLASH0_WRN/GPIO3_B5 | AG4 | gpio3b5 | flash0_wrn | | | | I/O | 8 | up | I | |
| FLASH0_CSN0/GPIO3_B6 | AC5 | gpio3b6 | flash0_csn0 | | | | I/O | 4 | up | I | |
| FLASH0_CSN1/GPIO3_B7 | AD4 | gpio3b7 | flash0_csn1 | | | | I/O | 4 | up | I | |
| FLASH0_CSN2/EMMC_CMD/GPIO3_C0 | AC4 | gpio3c0 | flash0_csn2 | emmc_cmd | | | I/O | 4 | up | I | |
| FLASH0_CSN3/EMMC_RSTNOUT/GPIO3_C1 | Y7 | gpio3c1 | flash0_csn3 | emmc_rstnout | | | I/O | 4 | up | I | |
| FLASH0_DQS/EMMC_CLKOUT/GPIO3_C2 | AB6 | gpio3c2 | flash0_dqs | emmc_clkout | | | I/O | 8 | down | I | |
| GPIO3_C3/FLASH0_VOLTAGE_SEL | Y8 | gpio3c3 | | | | | I/O | 4 | down | I | |
| FLASH1_D0/HOST_D0/MAC_TXD2/SDIO1_D0/GPIO3_D0 | Y4 | gpio3d0 | flash1_data0 | host_dout0 | mac_txd2 | sdio1_data0 | I/O | 8 | up | I | |

| Pad# | Ball# | func0 | func1 | func2 | func3 | func4 | Pad type | Current | Pull | Reset State | Power Supply |
|---|-------|---------|---------------|-------------|-----------|---------------|----------|---------|------|-------------|---------------|
| FLASH1_D1/HOST_D1/MAC_TXD3/SDIO1_D1/GPIO3_D1 | V6 | gpio3d1 | flash1_data1 | host_dout1 | mac_txd3 | sdio1_data1 | I/O | 8 | up | I | FLASH 1 |
| FLASH1_D2/HOST_D2/MAC_RXD2/SDIO1_D2/GPIO3_D2 | AB1 | gpio3d2 | flash1_data2 | host_dout2 | mac_rxd2 | sdio1_data2 | I/O | 8 | up | I | |
| FLASH1_D3/HOST_D3/MAC_RXD3/SDIO1_D3/GPIO3_D3 | AC1 | gpio3d3 | flash1_data3 | host_dout3 | mac_rxd3 | sdio1_data3 | I/O | 8 | up | I | |
| FLASH1_D4/HOST_D4/MAC_TXD0/SDIO1_DET/GPIO3_D4 | AD1 | gpio3d4 | flash1_data4 | host_dout4 | mac_txd0 | sdio1_detectn | I/O | 8 | up | I | |
| FLASH1_D5/HOST_D5/MAC_TXD1/SDIO1_WRPRT/GPIO3_D5 | AB2 | gpio3d5 | flash1_data5 | host_dout5 | mac_txd1 | sdio1_wrprt | I/O | 8 | up | I | |
| FLASH1_D6/HOST_D6/MAC_RXD0/SDIO1_BKPWR/GPIO3_D6 | AA3 | gpio3d6 | flash1_data6 | host_dout6 | mac_rxd0 | sdio1_bkpwr | I/O | 8 | up | I | |
| FLASH1_D7/HOST_D7/MAC_RXD1/SDIO1_INTN/GPIO3_D7 | AA4 | gpio3d7 | flash1_data7 | host_dout7 | mac_rxd1 | sdio1_intn | I/O | 8 | up | I | |
| FLASH1_RDY/HOST_CKOUTP/MAC_MDC/GPIO4_A0 | AC3 | gpio4a0 | flash1_rdy | host_ckoutp | mac_mdc | | I/O | 4 | up | I | |
| FLASH1_WP/HOST_CKOUTN/MAC_RXDV/FLASH0_CSN4/GPIO4_A1 | AC2 | gpio4a1 | flash1_wp | host_ckoutn | mac_rxdv | flash0_csn4 | I/O | 4 | up | I | |
| FLASH1_RDN/HOST_D8/MAC_RXER/FLASH0_CSN5/GPIO4_A2 | AE1 | gpio4a2 | flash1_rdn | host_dout8 | mac_rxer | flash0_csn5 | I/O | 4 | up | I | |
| FLASH1_ALE/HOST_D9/MAC_CLK/FLASH0_CSN6/GPIO4_A3 | AE2 | gpio4a3 | flash1_ale | host_dout9 | mac_clk | flash0_csn6 | I/O | 4 | up | I | |
| FLASH1_CLE/HOST_D10/MAC_TXEN/FLASH0_CSN7/GPIO4_A4 | AD2 | gpio4a4 | flash1_cle | host_dout10 | mac_txen | flash0_csn7 | I/O | 4 | up | I | |
| FLASH1_WRN/HOST_D11/MAC_CMD/GPIO4_A5 | Y5 | gpio4a5 | flash1_wrn | host_dout11 | mac_mdio | | I/O | 8 | up | I | |
| FLASH1_CSN0/HOST_D12/MAC_RXCLK/SDIO1_CMD/GPIO4_A6 | AB5 | gpio4a6 | flash1_csn0 | host_dout12 | mac_rxclk | sdio1_cmd | I/O | 4 | up | I | |
| FLASH1_CSN1/HOST_D13/MAC_CRS/SDIO1_CLKOUT/GPIO4_A7 | AA6 | gpio4a7 | flash1_csn1 | host_dout13 | mac_crs | sdio1_clkout | I/O | 4 | up | I | |
| FLASH1_DQS/HOST_D14/MAC_COL/FLASH1_CSN3/GPIO4_B0 | AA5 | gpio4b0 | flash1_dqs | host_dout14 | mac_col | flash1_csn3 | I/O | 8 | up | I | WIFI (APIO 3) |
| FLASH1_CSN2/HOST_D15/MAC_TXCLK/SDIO1_PWREN/GPIO4_B1 | V7 | gpio4b1 | flash1_csn2 | host_dout15 | mac_txclk | sdio1_pwren | I/O | 2 | up | I | |
| UART0_RX/GPIO4_C0 | AH11 | gpio4c0 | uart0bt_sin | | | | I/O | 2 | up | I | |
| UART0_TX/GPIO4_C1 | AG10 | gpio4c1 | uart0bt_sout | | | | I/O | 2 | down | I | |
| UART0_CTSN/GPIO4_C2 | AB12 | gpio4c2 | uart0bt_ctsn | | | | I/O | 2 | up | I | |
| UART0_RTSN/GPIO4_C3 | AB11 | gpio4c3 | uart0bt_rtsn | | | | I/O | 2 | up | I | |
| SDIO0_D0/GPIO4_C4 | AH9 | gpio4c4 | sdio0_data0 | | | | I/O | 4 | up | I | |
| SDIO0_D1/GPIO4_C5 | AH10 | gpio4c5 | sdio0_data1 | | | | I/O | 4 | up | I | |
| SDIO0_D2/GPIO4_C6 | AG9 | gpio4c6 | sdio0_data2 | | | | I/O | 4 | up | I | |
| SDIO0_D3/GPIO4_C7 | AH7 | gpio4c7 | sdio0_data3 | | | | I/O | 4 | up | I | |
| SDIO0_CMD/GPIO4_D0 | AH8 | gpio4d0 | sdio0_cmd | | | | I/O | 4 | up | I | |
| SDIO0_CLKOUT/GPIO4_D1 | AG8 | gpio4d1 | sdio0_clkout | | | | I/O | 4 | down | I | |
| SDIO0_DET/GPIO4_D2 | AF9 | gpio4d2 | sdio0_detectn | | | | I/O | 2 | up | I | |
| SDIO0_WRPRT/GPIO4_D3 | AE9 | gpio4d3 | sdio0_wrprt | | | | I/O | 2 | down | I | |
| SDIO0_PWREN/GPIO4_D4 | AC11 | gpio4d4 | sdio0_pwren | | | | I/O | 2 | down | I | |
| SDIO0_BKPWR/GPIO4_D5 | AF8 | gpio4d5 | sdio0_bkpwr | | | | I/O | 2 | down | I | |
| SDIO0_INTN/GPIO4_D6 | AE8 | gpio4d6 | sdio0_intn | | | | I/O | 2 | up | I | |

| Pad# | Ball# | func0 | func1 | func2 | func3 | func4 | Pad type | Current | Pull | Reset State | Power Supply |
|--------------------------------------|-------|---------|---------------|------------|---------------|-------|----------|---------|--------------------|-------------|----------------|
| GPIO4_D7 | AD9 | gpio4d7 | | | | | I/O | 2 | up | I | BB (APIO 5) |
| UART1_RX/TS0_D0/GPIO5_B0 | AF5 | gpio5b0 | uart1bb_sin | ts0_data0 | | | I/O | 2 | up | I | |
| UART1_TX/TS0_D1/GPIO5_B1 | AA7 | gpio5b1 | uart1bb_sout | ts0_data1 | | | I/O | 2 | down | I | |
| UART1_CTSN/TS0_D2/GPIO5_B2 | AH4 | gpio5b2 | uart1bb_ctsn | ts0_data2 | | | I/O | 2 | up | I | |
| UART1_RTSN/TS0_D3/GPIO5_B3 | AD6 | gpio5b3 | uart1bb_rtsn | ts0_data3 | | | I/O | 2 | up | I | |
| SPI0_CLK/TS0_D4/UART4_CTSN/GPIO5_B4 | AD7 | gpio5b4 | spi0_clk | ts0_data4 | uart4exp_ctsn | | I/O | 2 | up | I | |
| SPI0_CSN0/TS0_D5/UART4_RTSN/GPIO5_B5 | AC7 | gpio5b5 | spi0_csn0 | ts0_data5 | uart4exp_rtsn | | I/O | 2 | up | I | |
| SPI0_TXD/TS0_D6/UART4_TX/GPIO5_B6 | AE5 | gpio5b6 | spi0_txd | ts0_data6 | uart4exp_sout | | I/O | 2 | down | I | |
| SPI0_RXD/TS0_D7/UART4_RX/GPIO5_B7 | AF6 | gpio5b7 | spi0_rxd | ts0_data7 | uart4exp_sin | | I/O | 2 | up | I | |
| SPI0_CSN1/TS0_SYNC/GPIO5_C0 | AG5 | gpio5c0 | spi0_csn1 | ts0_sync | | | I/O | 2 | up | I | |
| TS0_VALID/GPIO5_C1 | AA9 | gpio5c1 | ts0_valid | | | | I/O | 2 | down | I | |
| TS0_CLK/GPIO5_C2 | AE6 | gpio5c2 | ts0_clk | | | | I/O | 2 | down | I | |
| TS0_ERR/GPIO5_C3 | AB8 | gpio5c3 | ts0_err | | | | I/O | 2 | down | I | |
| I2S_SCLK/GPIO6_A0 | AD11 | gpio6a0 | i2s_sclk | | | | I/O | 2 | down | I | AUDIO (APIO 4) |
| I2S_LRCK_RX/GPIO6_A1 | AG11 | gpio6a1 | i2s_lrckrx | | | | I/O | 2 | down | I | |
| I2S_LRCK_TX/GPIO6_A2 | AF11 | gpio6a2 | i2s_lrcktx | | | | I/O | 2 | down | I | |
| I2S_SDI/GPIO6_A3 | AE11 | gpio6a3 | i2s_sdi | | | | I/O | 2 | down | I | |
| I2S_SDO0/GPIO6_A4 | AG12 | gpio6a4 | i2s_sdo0 | | | | I/O | 2 | down | I | |
| I2S_SDO1/GPIO6_A5 | AH13 | gpio6a5 | i2s_sdo1 | | | | I/O | 2 | down | I | |
| I2S_SDO2/GPIO6_A6 | AG13 | gpio6a6 | i2s_sdo2 | | | | I/O | 2 | down | I | |
| I2S_SDO3/GPIO6_A7 | AH12 | gpio6a7 | i2s_sdo3 | | | | I/O | 2 | down | I | |
| I2S_CLK/GPIO6_B0 | AC12 | gpio6b0 | i2s_clk | | | | I/O | 4 | down | I | |
| I2C2_SDA/GPIO6_B1 | AF12 | gpio6b1 | i2c2audio_sda | | | | I/O | 2 | up | I | |
| I2C2_SCL/GPIO6_B2 | AD12 | gpio6b2 | i2c2audio_scl | | | | I/O | 2 | up | I | |
| SPDIF_TX/GPIO6_B3 | AE12 | gpio6b3 | spdif_tx | | | | I/O | 2 | down | I | |
| SDMMC0_D0/JTAG_TMS/GPIO6_C0 | AG7 | gpio6c0 | sdmmc0_dat a0 | jtag_tms | | | I/O | 4 | up | I | SDMMC0 |
| SDMMC0_D1/JTAG_TRSTN/GPIO6_C1 | AH6 | gpio6c1 | sdmmc0_dat a1 | jtag_trstn | | | I/O | 4 | Up Down(W version) | I | |
| SDMMC0_D2/JTAG_TDI/GPIO6_C2 | AD8 | gpio6c2 | sdmmc0_dat a2 | jtag_tdi | | | I/O | 4 | up | I | |
| SDMMC0_D3/JTAG_TCK/GPIO6_C3 | AB9 | gpio6c3 | sdmmc0_dat a3 | jtag_tck | | | I/O | 4 | up | I | |
| SDMMC0_CLKOUT/JTAG_TDO/GPIO6_C4 | AG6 | gpio6c4 | sdmmc0_clkout | jtag_tdo | | | O | 4 | down | O | |
| SDMMC0_CMD/GPIO6_C5 | AC8 | gpio6c5 | sdmmc0_cmd | | | | I/O | 4 | up | I | |
| SDMMC0_DECTN/GPIO6_C6 | AH5 | gpio6c6 | sdmmc0_dectn | | | | I/O | 2 | up | I | |

| Pad# | Ball# | func0 | func1 | func2 | func3 | func4 | Pad type | Current | Pull | Reset State | Power Supply |
|--|-------|---------|------------------|------------------|-------------|------------------|----------|---------|------|-------------|------------------|
| PWM0/GPIO7_A0 | H22 | gpio7a0 | pwm_0 | vop0_pwm | vop1_pwm | | I/O | 2 | down | I | GPIO30 (APIO1) |
| PWM1/GPIO7_A1 | G23 | gpio7a1 | pwm_1 | | | | I/O | 2 | down | I | |
| GPIO7_A2 | D28 | gpio7a2 | | | | | I/O | 2 | down | I | |
| GPIO7_A3 | F25 | gpio7a3 | | | | | I/O | 2 | down | I | |
| GPIO7_A4 | E26 | gpio7a4 | | | | | I/O | 2 | up | I | |
| GPIO7_A5 | G24 | gpio7a5 | | | | | I/O | 2 | down | I | |
| GPIO7_A6 | F26 | gpio7a6 | | | | | I/O | 2 | up | I | |
| UART3_RX/GPS_MAG/HSADC_D0_T1/GPIO7_A7 | E27 | gpio7a7 | uart3gps_sin | gps_mag | hsadc_data0 | | I/O | 2 | up | I | |
| UART3_TX/GPS_SIG/HSADC_D1_T1/GPIO7_B0 | J21 | gpio7b0 | uart3gps_sout | gps_sig | hsadc_data1 | | I/O | 2 | down | I | |
| UART3_CTSN/GPS_RFCLK/GPS_CLK_T1/GPIO7_B1 | H23 | gpio7b1 | uart3gps_ctsn | gps_rfclk | gps_clk | | I/O | 2 | up | I | |
| UART3_RTSN/GPIO7_B2 | F27 | gpio7b2 | uart3gps_rtsn | usb_drvvbus0 | | | I/O | 2 | up | I | |
| EDP_HOTPLUG/GPIO7_B3 | E28 | gpio7b3 | usb_drvvbus1 | edp_hotplug | | | I/O | 2 | down | I | |
| ISP_SHUTTEREN/SPI1_CLK/GPIO7_B4 | J22 | gpio7b4 | isp_shutteren | spi1_clk | | | I/O | 2 | down | I | |
| ISP_FLASHTRIGOUT/SPI1_CSN0/GPIO7_B5 | H24 | gpio7b5 | isp_flashtrigout | spi1_csn0 | | | I/O | 2 | up | I | |
| ISP_PRELIGHTTRIG/SPI1_RXD/GPIO7_B6 | F28 | gpio7b6 | isp_prelighttrig | spi1_rxd | | | I/O | 2 | down | I | |
| ISP_SHUTTERTRIG/SPI1_TXD/GPIO7_B7 | G27 | gpio7b7 | isp_shuttertrig | spi1_txd | | | I/O | 2 | down | I | |
| ISP_FLASHTRIGIN/EDPHDMI_CEC_T1/GPIO7_C0 | G28 | gpio7c0 | isp_flashtrigin | edphdmi_cecinout | | | I/O | 2 | up | I | |
| I2C4_SDA/GPIO7_C1 | H25 | gpio7c1 | i2c4tp_sda | | | | I/O | 2 | up | I | |
| I2C4_SCL/GPIO7_C2 | J23 | gpio7c2 | i2c4tp_scl | | | | I/O | 2 | up | I | |
| I2C5_SDA/EDPHDMI_I2C_SDA/GPIO7_C3 | H26 | gpio7c3 | i2c5hdmi_sda | edphdmii2c_sda | | | I/O | 2 | up | I | |
| I2C5_SCL/EDPHDMI_I2C_SCL/GPIO7_C4 | J24 | gpio7c4 | i2c5hdmi_scl | edphdmii2c_scl | | | I/O | 2 | up | I | |
| GPIO7_C5 | H27 | gpio7c5 | | | | | I/O | 2 | down | I | GPIO1830 (APIO2) |
| UART2_RX/IR_RX/PWM2/GPIO7_C6 | J25 | gpio7c6 | uart2dbg_sin | uart2dbg_sirin | pwm_2 | | I/O | 2 | up | I | |
| UART2_TX/IR_TX/PWM3/EDPHDMI_CEC/GPIO7_C7 | H28 | gpio7c7 | uart2dbg_sout | uart2dbg_sirout | pwm_3 | edphdmi_cecinout | I/O | 2 | up | I | |
| PS2_CLK/GPIO8_A0 | D24 | gpio8a0 | ps2_clk | sc_vcc18v | | | I/O | 2 | up | I | |
| PS2_DATA/GPIO8_A1 | C27 | gpio8a1 | ps2_data | sc_vcc33v | | | I/O | 2 | up | I | |
| GPIO8_A2/SC_DET | G21 | gpio8a2 | sc_detect | | | | I/O | 2 | up | I | |
| SPI2_CSN1/SC_IO/GPIO8_A3 | B28 | gpio8a3 | spi2_csn1 | sc_io | | | I/O | 2 | up | I | |
| I2C1_SDA/SC_RST/GPIO8_A4 | A28 | gpio8a4 | i2c1sensor_sda | sc_rst | | | I/O | 2 | up | I | |
| I2C1_SCL/SC_CLK/GPIO8_A5 | E25 | gpio8a5 | i2c1sensor_scl | sc_clk | | | I/O | 2 | up | I | GPIO1830 (APIO2) |
| SPI2_CLK/SC_IO_T1/GPIO8_A6 | D26 | gpio8a6 | spi2_clk | sc_io | | | I/O | 2 | down | I | |
| SPI2_CSN0/SC_DET_T1/GPIO8_A7 | D27 | gpio8a7 | spi2_csn0 | sc_detect | | | I/O | 2 | up | I | |

| Pad# | Ball# | func0 | func1 | func2 | func3 | func4 | Pad type | Curr ent | Pull | Reset State | Power Supply |
|-----------------------------|-------|--------------|--------------|--------------|-------|-------|----------|----------|------|-------------|--------------|
| SPI2_RXD/SC_RST_T1/GPIO8_B0 | F24 | gpio8b0 | spi2_rxd | sc_rst | | | I/O | 2 | down | I | |
| SPI2_TXD/SC_CLK_T1/GPIO8_B1 | C28 | gpio8b1 | spi2_txd | sc_clk | | | I/O | 2 | down | I | |
| BSJTAGTMS | G20 | bsjtagtms | | | | | I | 2 | up | I | |
| BSJTAGRSTN | E22 | bsjtagtrstn | | | | | I | 2 | up | I | |
| BSJTAGTDI | F21 | bsjtagtdi | | | | | I | 2 | up | I | |
| BSJTAGTCK | E23 | bsjtagtck | | | | | I | 2 | up | I | |
| BSJTAGTDO | F22 | bsjtagtdo | | | | | O | 2 | N/A | O | |
| LVDS_DATAP0 | T27 | lvds_padp0 | lcdc0_data0 | trace_data0 | | | A | | | NA | LVDS |
| LVDS_DATAN0 | T28 | lvds_padn0 | lcdc0_data1 | trace_data1 | | | A | | | NA | |
| LVDS_DATAP1 | U27 | lvds_padp1 | lcdc0_data2 | trace_data2 | | | A | | | NA | |
| LVDS_DATAN1 | U28 | lvds_padn1 | lcdc0_data3 | trace_data3 | | | A | | | NA | |
| LVDS_DATAP2 | W27 | lvds_padp2 | lcdc0_data4 | trace_data4 | | | A | | | NA | |
| LVDS_DATAN2 | W28 | lvds_padn2 | lcdc0_data5 | trace_data5 | | | A | | | NA | |
| LVDS_DATAP3 | Y27 | lvds_padp3 | lcdc0_data6 | trace_data6 | | | A | | | NA | |
| LVDS_DATAN3 | Y28 | lvds_padn3 | lcdc0_data7 | trace_data7 | | | A | | | NA | |
| LVDS_DATAP4 | AA27 | lvds_padp4 | lcdc0_data8 | trace_data8 | | | A | | | NA | |
| LVDS_DATAN4 | AA28 | lvds_padn4 | lcdc0_data9 | trace_data9 | | | A | | | NA | |
| LVDS_CLKP0 | V27 | lvds_clkp0 | lcdc0_data10 | trace_data10 | | | A | | | NA | |
| LVDS_CLKN0 | V28 | lvds_clkn0 | lcdc0_data11 | trace_data11 | | | A | | | NA | |
| LVDS_DATAP5 | U25 | lvds_padp5 | lcdc0_data12 | trace_data12 | | | A | | | NA | |
| LVDS_DATAN5 | U26 | lvds_padn5 | lcdc0_data13 | trace_data13 | | | A | | | NA | |
| LVDS_DATAP6 | V25 | lvds_padp6 | lcdc0_data14 | trace_data14 | | | A | | | NA | |
| LVDS_DATAN6 | V26 | lvds_padn6 | lcdc0_data15 | trace_data15 | | | A | | | NA | |
| LVDS_DATAP7 | AA25 | lvds_padp7 | lcdc0_data16 | trace_clk | | | A | | | NA | |
| LVDS_DATAN7 | AA26 | lvds_padn7 | lcdc0_data17 | trace_ctl | | | A | | | NA | |
| LVDS_DATAP8 | AB27 | lvds_padp8 | lcdc0_data18 | | | | A | | | NA | |
| LVDS_DATAN8 | AB28 | lvds_padn8 | lcdc0_data19 | | | | A | | | NA | |
| LVDS_DATAP9 | AC25 | lvds_padp9 | lcdc0_data20 | | | | A | | | NA | |
| LVDS_DATAN9 | AC26 | lvds_padn9 | lcdc0_data21 | | | | A | | | NA | |
| LVDS_CLKP1 | Y25 | lvds_clkp1 | lcdc0_data22 | | | | A | | | NA | |
| LVDS_CLKN1 | Y26 | lvds_clkn1 | lcdc0_data23 | | | | A | | | NA | |
| ADC_IN2 | P23 | saradc_ain2 | | | | | A | | | NA | SARAD C |
| ADC_IN1 | P21 | saradc_ain1 | | | | | A | | | NA | |
| ADC_IN0 | P24 | saradc_ain0 | | | | | A | | | NA | |
| MIPI_TXRX_D0N | AF20 | mip_itrx_d0n | | | | | A | | | NA | MIPI |

| Pad# | Ball# | func0 | func1 | func2 | func3 | func4 | Pad type | Current | Pull | Reset State | Power Supply |
|----------------|-------|---------------|-------|-------|-------|-------|----------|---------|------|-------------|--------------|
| MIPI_TXRX_D0P | AE20 | mip_itrx_d0p | | | | | A | | | NA | |
| MIPI_TXRX_D1P | AE21 | mip_itrx_d1p | | | | | A | | | NA | |
| MIPI_TXRX_D1N | AF21 | mip_itrx_d1n | | | | | A | | | NA | |
| MIPI_TXRX_CLKN | AF23 | mip_itrx_clkn | | | | | A | | | NA | |
| MIPI_TXRX_CLKP | AE23 | mip_itrx_clkp | | | | | A | | | NA | |
| MIPI_TXRX_D2N | AF24 | mip_itrx_d2n | | | | | A | | | NA | |
| MIPI_TXRX_D2P | AE24 | mip_itrx_d2p | | | | | A | | | NA | |
| MIPI_TXRX_D3N | AD25 | mip_itrx_d3n | | | | | A | | | NA | |
| MIPI_TXRX_D3P | AF25 | mip_itrx_d3p | | | | | A | | | NA | |
| MIPI_TXRX_REXT | AD22 | mip_itrx_rext | | | | | A | | | NA | |
| MIPI_TX_REXT | AE26 | mipi_tx_rext | | | | | A | | | NA | |
| MIPI_TX_D3P | AC27 | mipi_tx_d3p | | | | | A | | | NA | |
| MIPI_TX_D3N | AC28 | mipi_tx_d3n | | | | | A | | | NA | |
| MIPI_TX_D2N | AD28 | mipi_tx_d2n | | | | | A | | | NA | |
| MIPI_TX_D2P | AD27 | mipi_tx_d2p | | | | | A | | | NA | |
| MIPI_TX_CLKP | AE27 | mipi_tx_clkp | | | | | A | | | NA | |
| MIPI_TX_CLKN | AE28 | mipi_tx_clkn | | | | | A | | | NA | |
| MIPI_TX_D1P | AF27 | mipi_tx_d1p | | | | | A | | | NA | |
| MIPI_TX_D1N | AF28 | mipi_tx_d1n | | | | | A | | | NA | |
| MIPI_TX_D0N | AG28 | mipi_tx_d0n | | | | | A | | | NA | |
| MIPI_TX_D0P | AG27 | mipi_tx_d0p | | | | | A | | | NA | |
| MIPI_RX_REXT | AD21 | mipi_rx_rext | | | | | A | | | NA | |
| MIPI_RX_D3N | AH27 | mipi_rx_d3n | | | | | A | | | NA | |
| MIPI_RX_D3P | AH28 | mipi_rx_d3p | | | | | A | | | NA | |
| MIPI_RX_D2N | AH26 | mipi_rx_d2n | | | | | A | | | NA | |
| MIPI_RX_D2P | AG26 | mipi_rx_d2p | | | | | A | | | NA | |
| MIPI_RX_CLKP | AG25 | mipi_rx_clkp | | | | | A | | | NA | |
| MIPI_RX_CLKN | AH25 | mipi_rx_clkn | | | | | A | | | NA | |
| MIPI_RX_D1P | AG24 | mipi_rx_d1p | | | | | A | | | NA | |
| MIPI_RX_D1N | AH24 | mipi_rx_d1n | | | | | A | | | NA | |
| MIPI_RX_D0P | AG23 | mipi_rx_d0p | | | | | A | | | NA | |
| MIPI_RX_D0N | AH23 | mipi_rx_d0n | | | | | A | | | NA | |
| HDMI_TX2P | AG22 | hdmi_tx2p | | | | | A | | | NA | HDMI |

| Pad# | Ball# | func0 | func1 | func2 | func3 | func4 | Pad type | Current | Pull | Reset State | Power Supply |
|---------------|-------|---------------|-------|-------|-------|-------|----------|---------|------|-------------|--------------|
| HDMI_TX2N | AH22 | hdmi_tx2n | | | | | A | | | NA | |
| HDMI_TX1P | AG21 | hdmi_tx1p | | | | | A | | | NA | |
| HDMI_TX1N | AH21 | hdmi_tx1n | | | | | A | | | NA | |
| HDMI_TX0P | AG20 | hdmi_tx0p | | | | | A | | | NA | |
| HDMI_TX0N | AH20 | hdmi_tx0n | | | | | A | | | NA | |
| HDMI_TCN | AH19 | hdmi_tcn | | | | | A | | | NA | |
| HDMI_TCP | AG19 | hdmi_tcp | | | | | A | | | NA | |
| HDMI_REXT | AB17 | hdmi_rext | | | | | A | | | NA | |
| HDMI_HPD | AB18 | hdmi_hpd | | | | | A | | | NA | |
| EDP_TP_OUT | AA12 | edp_tp_out | | | | | A | | | NA | eDP |
| EDP_REXT | AC18 | edp_rext | | | | | A | | | NA | |
| EDP_CLK24M_IN | AC17 | edp_clk24m_in | | | | | A | | | NA | |
| EDP_AUXN | AH18 | edp_auxn | | | | | A | | | NA | |
| EDP_AUXP | AG18 | edp_auxp | | | | | A | | | NA | |
| EDP_TX3P | AG17 | edp_tx3p | | | | | A | | | NA | |
| EDP_TX3N | AH17 | edp_tx3n | | | | | A | | | NA | |
| EDP_TX2N | AH16 | edp_tx2n | | | | | A | | | NA | |
| EDP_TX2P | AG16 | edp_tx2p | | | | | A | | | NA | |
| EDP_TX1N | AH15 | edp_tx1n | | | | | A | | | NA | |
| EDP_TX1P | AG15 | edp_tx1p | | | | | A | | | NA | |
| EDP_TX0P | AG14 | edp_tx0p | | | | | A | | | NA | |
| EDP_TX0N | AH14 | edp_tx0n | | | | | A | | | NA | |
| DDR1_DQ7 | Y3 | ddr1_dq7 | | | | | A | | | NA | DDR1 |
| DDR1_DQ6 | V5 | ddr1_dq6 | | | | | A | | | NA | |
| DDR1_DQ5 | Y2 | ddr1_dq5 | | | | | A | | | NA | |
| DDR1_DQS0 | AA2 | ddr1_dqs0 | | | | | A | | | NA | |
| DDR1_DQS0N | AA1 | ddr1_dqs0n | | | | | A | | | NA | |
| DDR1_DQ4 | W1 | ddr1_dq4 | | | | | A | | | NA | |
| DDR1_DQ3 | U6 | ddr1_dq3 | | | | | A | | | NA | |
| DDR1_DQ2 | Y1 | ddr1_dq2 | | | | | A | | | NA | |
| DDR1_DQ1 | V3 | ddr1_dq1 | | | | | A | | | NA | |
| DDR1_DQ0 | W2 | ddr1_dq0 | | | | | A | | | NA | |
| DDR1_DM0 | U5 | ddr1_dm0 | | | | | A | | | NA | |
| DDR1_VREF | M8 | ddr1_vref0 | | | | | P | | | NA | |
| DDR1_DQ23 | V2 | ddr1_dq23 | | | | | A | | | NA | |

| Pad# | Ball# | func0 | func1 | func2 | func3 | func4 | Pad type | Curr ent | Pull | Reset State | Power Supply |
|------------|-------|------------|-------|-------|-------|-------|----------|----------|------|-------------|--------------|
| DDR1_DQ22 | U3 | ddr1_dq22 | | | | | A | | | NA | |
| DDR1_DQ21 | V1 | ddr1_dq21 | | | | | A | | | NA | |
| DDR1_DQ20 | U4 | ddr1_dq20 | | | | | A | | | NA | |
| DDR1_DQS2 | U2 | ddr1_dqs2 | | | | | A | | | NA | |
| DDR1_DQS2N | U1 | ddr1_dqn2 | | | | | A | | | NA | |
| DDR1_DQ19 | R5 | ddr1_dq19 | | | | | A | | | NA | |
| DDR1_DQ18 | T1 | ddr1_dq18 | | | | | A | | | NA | |
| DDR1_DQ17 | R6 | ddr1_dq17 | | | | | A | | | NA | |
| DDR1_DQ16 | T2 | ddr1_dq16 | | | | | A | | | NA | |
| DDR1_DM2 | R3 | ddr1_dm2 | | | | | A | | | NA | |
| DDR1_PZQ | U7 | ddr1_pzq | | | | | A | | | NA | |
| DDR1_ATO | M7 | ddr1_ato | | | | | A | | | NA | |
| DDR1_DTO1 | R8 | ddr1_dto1 | | | | | A | | | NA | |
| DDR1_DTO0 | U8 | ddr1_dto0 | | | | | A | | | NA | |
| DDR1_ODT1 | R2 | ddr1_odt1 | | | | | A | | | NA | |
| DDR1_ODT0 | P5 | ddr1_odt0 | | | | | A | | | NA | |
| DDR1_A15 | R1 | ddr1_a15 | | | | | A | | | NA | |
| DDR1_VREF | M8 | ddr1_vref1 | | | | | P | | | NA | |
| DDR1_A14 | P2 | ddr1_a14 | | | | | A | | | NA | |
| DDR1_A13 | P3 | ddr1_a13 | | | | | A | | | NA | |
| DDR1_A12 | P6 | ddr1_a12 | | | | | A | | | NA | |
| DDR1_A11 | P4 | ddr1_a11 | | | | | A | | | NA | |
| DDR1_A10 | N2 | ddr1_a10 | | | | | A | | | NA | |
| DDR1_A9 | P1 | ddr1_a9 | | | | | A | | | NA | |
| DDR1_A8 | N1 | ddr1_a8 | | | | | A | | | NA | |
| DDR1_A7 | M3 | ddr1_a7 | | | | | A | | | NA | |
| DDR1_A6 | M1 | ddr1_a6 | | | | | A | | | NA | |
| DDR1_A5 | M2 | ddr1_a5 | | | | | A | | | NA | |
| DDR1_CK | L2 | ddr1_ck | | | | | A | | | NA | |
| DDR1_CKN | L1 | ddr1_ckn | | | | | A | | | NA | |
| DDR1_A4 | M6 | ddr1_a4 | | | | | A | | | NA | |
| DDR1_A3 | M5 | ddr1_a3 | | | | | A | | | NA | |
| DDR1_A2 | K1 | ddr1_a2 | | | | | A | | | NA | |
| DDR1_A1 | K2 | ddr1_a1 | | | | | A | | | NA | |
| DDR1_A0 | L3 | ddr1_a0 | | | | | A | | | NA | |

| Pad# | Ball# | func0 | func1 | func2 | func3 | func4 | Pad type | Curr ent | Pull | Reset State | Power Supply |
|-------------|-------|------------|-------|-------|-------|-------|----------|----------|------|-------------|--------------|
| DDR1_BA2 | L5 | ddr1_ba2 | | | | | A | | | NA | |
| DDR1_BA1 | J1 | ddr1_ba1 | | | | | A | | | NA | |
| DDR1_BA0 | L4 | ddr1_ba0 | | | | | A | | | NA | |
| DDR1_RASN | L6 | ddr1_rasn | | | | | A | | | NA | |
| DDR1_CASN | H1 | ddr1_casn | | | | | A | | | NA | |
| DDR1_WEN | J2 | ddr1_wen | | | | | A | | | NA | |
| DDR1_CS1N | J3 | ddr1_csn1 | | | | | A | | | NA | |
| DDR1_CS0N | H2 | ddr1_csn0 | | | | | A | | | NA | |
| DDR1_CKE1 | H3 | ddr1_cke1 | | | | | A | | | NA | |
| DDR1_CKE0 | F1 | ddr1_cke0 | | | | | A | | | NA | |
| DDR1_RESET | F2 | ddr1_reset | | | | | A | | | NA | |
| DDR1_VREFAO | L8 | ddr1_vref2 | | | | | P | | | NA | |
| DDR1_RETLE | H7 | ddr1_retie | | | | | A | | | NA | |
| DDR1_DQ15 | J6 | ddr1_dq15 | | | | | A | | | NA | |
| DDR1_DQ14 | J5 | ddr1_dq14 | | | | | A | | | NA | |
| DDR1_DQ13 | H4 | ddr1_dq13 | | | | | A | | | NA | |
| DDR1_DQ12 | H5 | ddr1_dq12 | | | | | A | | | NA | |
| DDR1_DQS1 | G2 | ddr1_dqs1 | | | | | A | | | NA | |
| DDR1_DQS1N | G1 | ddr1_dqs1n | | | | | A | | | NA | |
| DDR1_DQ11 | F3 | ddr1_dq11 | | | | | A | | | NA | |
| DDR1_DQ10 | C1 | ddr1_dq10 | | | | | A | | | NA | |
| DDR1_DQ9 | E1 | ddr1_dq9 | | | | | A | | | NA | |
| DDR1_DQ8 | E2 | ddr1_dq8 | | | | | A | | | NA | |
| DDR1_DM1 | G5 | ddr1_dm1 | | | | | A | | | NA | |
| DDR1_VREF | M8 | ddr1_vref3 | | | | | P | | | NA | |
| DDR1_DQ31 | H6 | ddr1_dq31 | | | | | A | | | NA | |
| DDR1_DQ30 | C2 | ddr1_dq30 | | | | | A | | | NA | |
| DDR1_DQ29 | F5 | ddr1_dq29 | | | | | A | | | NA | |
| DDR1_DQ28 | E3 | ddr1_dq28 | | | | | A | | | NA | |
| DDR1_DQS3 | D2 | ddr1_dqs3 | | | | | A | | | NA | |
| DDR1_DQS3N | D1 | ddr1_dqs3n | | | | | A | | | NA | |
| DDR1_DQ27 | G6 | ddr1_dq27 | | | | | A | | | NA | |
| DDR1_DQ26 | E4 | ddr1_dq26 | | | | | A | | | NA | |
| DDR1_DQ25 | B2 | ddr1_dq25 | | | | | A | | | NA | |
| DDR1_DQ24 | B1 | ddr1_dq24 | | | | | A | | | NA | |

| Pad# | Ball# | func0 | func1 | func2 | func3 | func4 | Pad type | Curr ent | Pull | Reset State | Power Suppl y |
|-------------|-------|------------|-------|-------|-------|-------|----------|----------|------|-------------|---------------|
| DDR1_DM3 | D3 | ddr1_dm3 | | | | | A | | | NA | DDR0 |
| DDR0_DM3 | B3 | ddr0_dm3 | | | | | A | | | NA | |
| DDR0_DQ24 | A2 | ddr0_dq24 | | | | | A | | | NA | |
| DDR0_DQ25 | A1 | ddr0_dq25 | | | | | A | | | NA | |
| DDR0_DQ26 | D5 | ddr0_dq26 | | | | | A | | | NA | |
| DDR0_DQ27 | E6 | ddr0_dq27 | | | | | A | | | NA | |
| DDR0_DQS3N | A4 | ddr0_dqsn3 | | | | | A | | | NA | |
| DDR0_DQS3 | B4 | ddr0_dqs3 | | | | | A | | | NA | |
| DDR0_DQ28 | C5 | ddr0_dq28 | | | | | A | | | NA | |
| DDR0_DQ29 | F7 | ddr0_dq29 | | | | | A | | | NA | |
| DDR0_DQ30 | C4 | ddr0_dq30 | | | | | A | | | NA | |
| DDR0_DQ31 | E7 | ddr0_dq31 | | | | | A | | | NA | |
| DDR0_VREF | H12 | ddr0_vref3 | | | | | P | | | NA | |
| DDR0_DM1 | F9 | ddr0_dm1 | | | | | A | | | NA | |
| DDR0_DQ8 | B5 | ddr0_dq8 | | | | | A | | | NA | |
| DDR0_DQ9 | A5 | ddr0_dq9 | | | | | A | | | NA | |
| DDR0_DQ10 | A3 | ddr0_dq10 | | | | | A | | | NA | |
| DDR0_DQ11 | C6 | ddr0_dq11 | | | | | A | | | NA | |
| DDR0_DQS1N | A7 | ddr0_dqsn1 | | | | | A | | | NA | |
| DDR0_DQS1 | B7 | ddr0_dqs1 | | | | | A | | | NA | |
| DDR0_DQ12 | E8 | ddr0_dq12 | | | | | A | | | NA | |
| DDR0_DQ13 | A6 | ddr0_dq13 | | | | | A | | | NA | |
| DDR0_DQ14 | B6 | ddr0_dq14 | | | | | A | | | NA | |
| DDR0_DQ15 | F8 | ddr0_dq15 | | | | | A | | | NA | |
| DDR0_RETLE | G8 | ddr0_retie | | | | | A | | | NA | |
| DDR0_VREFAO | H11 | ddr0_verf2 | | | | | P | | | NA | |
| DDR0_RESET | E9 | ddr0_reset | | | | | A | | | NA | |
| DDR0_CKE0 | C9 | ddr0_cke0 | | | | | A | | | NA | |
| DDR0_CKE1 | C8 | ddr0_cke1 | | | | | A | | | NA | |
| DDR0_CS0N | B8 | ddr0_csn0 | | | | | A | | | NA | |
| DDR0_CS1N | F11 | ddr0_csn1 | | | | | A | | | NA | |
| DDR0_WEN | B9 | ddr0_wen | | | | | A | | | NA | |
| DDR0_CASN | A8 | ddr0_casn | | | | | A | | | NA | |
| DDR0_RASN | D11 | ddr0_rasn | | | | | A | | | NA | |
| DDR0_BA0 | D8 | ddr0_ba0 | | | | | A | | | NA | |

| Pad# | Ball# | func0 | func1 | func2 | func3 | func4 | Pad type | Curr ent | Pull | Reset State | Power Supply |
|------------|-------|------------|-------|-------|-------|-------|----------|----------|------|-------------|--------------|
| DDR0_BA1 | A9 | ddr0_ba1 | | | | | A | | | NA | |
| DDR0_BA2 | E11 | ddr0_ba2 | | | | | A | | | NA | |
| DDR0_A0 | B10 | ddr0_a0 | | | | | A | | | NA | |
| DDR0_A1 | C11 | ddr0_a1 | | | | | A | | | NA | |
| DDR0_A2 | A10 | ddr0_a2 | | | | | A | | | NA | |
| DDR0_A3 | E12 | ddr0_a3 | | | | | A | | | NA | |
| DDR0_A4 | F12 | ddr0_a4 | | | | | A | | | NA | |
| DDR0_CKN | A11 | ddr0_ckn | | | | | A | | | NA | |
| DDR0_CK | B11 | ddr0_ck | | | | | A | | | NA | |
| DDR0_A5 | B12 | ddr0_a5 | | | | | A | | | NA | |
| DDR0_A6 | C12 | ddr0_a6 | | | | | A | | | NA | |
| DDR0_A7 | A12 | ddr0_a7 | | | | | A | | | NA | |
| DDR0_A8 | B13 | ddr0_a8 | | | | | A | | | NA | |
| DDR0_A9 | A14 | ddr0_a9 | | | | | A | | | NA | |
| DDR0_A10 | A13 | ddr0_a10 | | | | | A | | | NA | |
| DDR0_A11 | D14 | ddr0_a11 | | | | | A | | | NA | |
| DDR0_A12 | F14 | ddr0_a12 | | | | | A | | | NA | |
| DDR0_A13 | C14 | ddr0_a13 | | | | | A | | | NA | |
| DDR0_A14 | B14 | ddr0_a14 | | | | | A | | | NA | |
| DDR0_VREF | H12 | ddr0_vref1 | | | | | P | | | NA | |
| DDR0_A15 | C15 | ddr0_a15 | | | | | A | | | NA | |
| DDR0_ODT0 | E14 | ddr0_odt0 | | | | | A | | | NA | |
| DDR0_ODT1 | E15 | ddr0_odt1 | | | | | A | | | NA | |
| DDR0_DTO0 | H17 | ddr0_dto0 | | | | | A | | | NA | |
| DDR0_DTO1 | H15 | ddr0_dto1 | | | | | A | | | NA | |
| DDR0_ATO | G12 | ddr0_ato | | | | | A | | | NA | |
| DDR0_PZQ | G17 | ddr0_pzq | | | | | A | | | NA | |
| DDR0_DM2 | A15 | ddr0_dm2 | | | | | A | | | NA | |
| DDR0_DQ16 | B15 | ddr0_dq16 | | | | | A | | | NA | |
| DDR0_DQ17 | A16 | ddr0_dq17 | | | | | A | | | NA | |
| DDR0_DQ18 | F15 | ddr0_dq18 | | | | | A | | | NA | |
| DDR0_DQ19 | B16 | ddr0_dq19 | | | | | A | | | NA | |
| DDR0_DQS2N | A17 | ddr0_dqsn2 | | | | | A | | | NA | |
| DDR0_DQS2 | B17 | ddr0_dqs2 | | | | | A | | | NA | |
| DDR0_DQ20 | D17 | ddr0_dq20 | | | | | A | | | NA | |

| Pad# | Ball# | func0 | func1 | func2 | func3 | func4 | Pad type | Curr ent | Pull | Reset State | Power Supply |
|------------------|-------|------------------|-------|-------|-------|-------|----------|----------|------|-------------|--------------|
| DDR0_DQ21 | B18 | ddr0_dq21 | | | | | A | | | NA | |
| DDR0_DQ22 | C17 | ddr0_dq22 | | | | | A | | | NA | |
| DDR0_DQ23 | A18 | ddr0_dq23 | | | | | A | | | NA | |
| DDR0_VREF | H12 | ddr0_vref0 | | | | | P | | | NA | |
| DDR0_DM0 | E17 | ddr0_dm0 | | | | | A | | | NA | |
| DDR0_DQ0 | B19 | ddr0_dq0 | | | | | A | | | NA | |
| DDR0_DQ1 | C18 | ddr0_dq1 | | | | | A | | | NA | |
| DDR0_DQ2 | F17 | ddr0_dq2 | | | | | A | | | NA | |
| DDR0_DQ3 | F18 | ddr0_dq3 | | | | | A | | | NA | |
| DDR0_DQ4 | A19 | ddr0_dq4 | | | | | A | | | NA | |
| DDR0_DQS0N | B20 | ddr0_dqs0 | | | | | A | | | NA | |
| DDR0_DQS0 | A20 | ddr0_dqs0 | | | | | A | | | NA | |
| DDR0_DQ5 | E18 | ddr0_dq5 | | | | | A | | | NA | |
| DDR0_DQ6 | C20 | ddr0_dq6 | | | | | A | | | NA | |
| DDR0_DQ7 | D20 | ddr0_dq7 | | | | | A | | | NA | |
| USBHOST2_DP | B22 | usbhost1_dp | | | | | A | | | NA | USBH OST1 |
| USBHOST2_DM | A22 | usbhost1_dm | | | | | A | | | NA | |
| USBHOST2_TXRTUNE | C21 | usbhost1_txrtune | | | | | A | | | NA | |
| USBHOST1_DP | B23 | usbhost1_dp | | | | | A | | | NA | USBH OST0 |
| USBHOST1_DM | A23 | usbhost1_dm | | | | | A | | | NA | |
| USBHOST1_TXRTUNE | C23 | usbhost1_txrtune | | | | | A | | | NA | |
| USBOTG_ID | C25 | usbotg_id | | | | | A | | | NA | USBOT G |
| USBOTG_VBUS | D23 | usbotg_vbus | | | | | A | | | NA | |
| USBOTG_DP | B26 | usbotg_dp | | | | | A | | | NA | |
| USBOTG_DM | A26 | usbotg_dm | | | | | A | | | NA | |
| USBOTG_TXRTUNE | D21 | usbotg_txrtune | | | | | A | | | NA | |
| USIC_STROBE | B27 | usic_strobe | | | | | A | | | NA | USIC |
| USIC_DATA | A27 | usic_data | | | | | A | | | NA | |

Notes :

①: Pad types : I = input , O = output , I/O = input/output (bidirectional) ,
 AP = Analog Power , AG = Analog Ground
 DP = Digital Power , DG = Digital Ground
 A = Analog

②: Output Drive strength is configurable, it's the suggested value in this table. Unit is mA , only Digital IO have drive value

③:Reset state: I = input without any pull resistor O = output

④:It is die location. For examples, "Left side" means that all the related IOs are always in left side of die

⑤:Power supply means that all the related IOs are in this IO power domain. If multiple powers are included, they are connected together in one IO power ring

⑥:The pull up/pull down is configurable.

2.8 IO pin name descriptions

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-3 RK3288 IO function description list

| Interface | Pin Name | Direction | Description |
|-----------|---------------|-----------|--|
| Misc | XIN24M | I | Clock input of 24MHz crystal |
| | XOUT24M | O | Clock output of 24MHz crystal |
| | CLK32K | I | Clock input of 32.768KHz |
| | NPOR | I | Chip hardware reset |
| | SECURITYSEL | I | Security solution selection |
| | clk_27m | I | External 27MHz clock input |
| | global_pwroff | O | Request signal to external PMIC for power down CPU subsystem with qual-core Cortex-A17 or power down SoC Core logic w/o Cortex-A17 subsystem and PMU logic |
| | ddrio_pwroff | O | Request signal to external PMIC for power down DDR IO |
| | ddrio0_reten | O | DDR0 IO retention control |
| | ddrio1_reten | O | DDR1 IO retention control |
| | tsadc_int | O | TSADC trigger to shut down chip |

| Interface | Pin Name | Direction | Description |
|-----------|------------|-----------|--|
| | jtag_trstn | I | JTAG interface reset input |
| | jtag_tck | I | JTAG interface clock input/SWD interface clock input |
| | jtag_tdi | I | JTAG interface TDI input |
| | jtag_tms | I/O | JTAG interface TMS input/SWD interface data out |
| | jtag_tdo | O | JTAG interface TDO output |

| Interface | Pin Name | Direction | Description |
|-----------|---------------------------------------|-----------|-----------------------------------|
| ETM Trace | trace_clk | O | Cortex-A17 ETM trace port clk |
| | trace_ctl | O | Cortex-A17 ETM trace port control |
| | trace_data <i>i</i> (<i>i</i> =0~15) | O | Cortex-A17 ETM trace port data |

| Interface | Pin Name | Direction | Description |
|------------------------|---------------------------------------|-----------|--|
| SD/MMC Host Controller | sdmmc0_clkout | O | sdmmc card clock. |
| | sdmmc0_cmd | I/O | sdmmc card command output and reponse input. |
| | sdmmc0_data <i>i</i> (<i>i</i> =0~3) | I/O | sdmmc card data input and output. |
| | sdmmc0_detect_n | I | sdmmc card detect signal, a 0 represents presence of card. |

| Interface | Pin Name | Direction | Description |
|----------------------|------------------------------|-----------|---|
| SDIO Host Controller | sdiox_clkout(<i>x</i> =0,1) | O | sdio card clock. |
| | sdiox_cmd(<i>x</i> =0,1) | I/O | sdio card command output and reponse input. |

| Interface | Pin Name | Direction | Description |
|-------------|--|-----------|--|
| (2 channel) | sdiox_data <i>i</i> (<i>i</i> =0~3) (<i>x</i> =0,1) | I/O | sdio card data input and output. |
| | sdiox_detectn(<i>x</i> =0,1) | I | sdio card detect signal, a 0 represents presence of card. |
| | sdiox_wrprt(<i>x</i> =0,1) | I | sdio card write protect signal, a 1 represents write is protected. |
| | sdiox_pwren(<i>x</i> =0,1) | O | sdio card power-enable control signal |
| | sdiox_intn(<i>x</i> =0,1) | O | sdio card interrupt indication |
| | sdiox_bkpwr(<i>x</i> =0,1) | O | the back-end power supply for embedded device |

| Interface | Pin Name | Direction | Description |
|----------------|--|-----------|---|
| eMMC Interface | emmc_clkout | O | emmc card clock. |
| | emmc_cmd | I/O | emmc card command output and reponse input. |
| | emmc_data <i>i</i> (<i>i</i> =0~7) | I/O | emmc card data input and output. |
| | emmc_pwren | O | emmc card power-enable control signal |
| | emmc_rstnout | O | emmc card reset signal |

| Interface | Pin Name | Direction | Description |
|--------------------|--|-----------|---|
| DMC (2 channel) | DDR _x _CK(<i>x</i> =0,1) | O | Active-high clock signal to the memory device. |
| | DDR _x _CK_N(<i>x</i> =0,1) | O | Active-low clock signal to the memory device. |
| | DDR _x _CKE <i>i</i> (<i>i</i> =0,1) (<i>x</i> =0,1) | O | Active-high clock enable signal to the memory device for two chip select. |
| | DDR _x _CSN <i>i</i> (<i>i</i> =0,1) (<i>x</i> =0,1) | O | Active-low chip select signal to the memory device. A There are two chip select. |
| | DDR _x _RASN(<i>x</i> =0,1) | O | Active-low row address strobe to the memory device. |
| | DDR _x _CASN(<i>x</i> =0,1) | O | Active-low column address strobe to the memory device. |
| | DDR _x _WEN(<i>x</i> =0,1) | O | Active-low write enable strobe to the memory device. |
| | DDR _x _BA[2:0] (<i>x</i> =0,1) | O | Bank address signal to the memory device. |
| | DDR _x _ADDR[15:0] (<i>x</i> =0,1) | O | Address signal to the memory device. |
| | DDR _x _DQ[31:0] (<i>x</i> =0,1) | I/O | Bidirectional data line to the memory device. |
| | DDR _x _DQS[3:0] (<i>x</i> =0,1) | I/O | Active-high bidirectional data strobes to the memory device. |
| | DDR _x _DQS_B[3:0] (<i>x</i> =0,1) | I/O | Active-low bidirectional data strobes to the memory device. |
| | DDR _x _DM[3:0] (<i>x</i> =0,1) | O | Active-low data mask signal to the memory device. |
| | DDR _x _ODT <i>i</i> (<i>i</i> =0,1) (<i>x</i> =0,1) | O | On-Die Termination output signal for two chip select. |
| | DDR _x _RETEN(<i>x</i> =0,1) | I | Active-low retention latch enable input |
| | DDR _x _RESET(<i>x</i> =0,1) | O | DDR3 reset signal to the memory device |
| | DDR _x _VREF <i>i</i> (<i>i</i> =0,1,2,3) (<i>x</i> =0,1) | I/O | Reference Voltage input for three regions of DDR IO |
| | DDR _x _PZQ(<i>x</i> =0,1) | I/O | ZQ calibration pad which connects 240ohm±1% resistor |

| Interface | Pin Name | Direction | Description |
|----------------------|---|-----------|-----------------------------------|
| NandC (2 channel) | flash _x _wp(<i>x</i> =0,1) | O | Flash write-protected signal |
| | flash _x _ale(<i>x</i> =0,1) | O | Flash address latch enable signal |

| Interface | Pin Name | Direction | Description |
|-----------|--|-----------|---|
| | flashx_cle($x=0,1$) | O | Flash command latch enable signal |
| | flashx_wrn($x=0,1$) | O | Flash write enable and clock signal |
| | flashx_rdn($x=0,1$) | O | Flash read enable and write/read signal |
| | flashx_datai($i=0\sim7$) ($x=0,1$) | I/O | Flash data inputs/outputs signal |
| | flashx_dqs($x=0,1$) | I/O | Flash data strobe signal |
| | flashx_rdy($x=0,1$) | I | Flash ready/busy signal |
| | flashx_csni($i=0\sim7$) ($x=0,1$) | O | Flash chip enable signal for chip i, $i=0\sim7$ |

| Interface | Pin Name | Direction | Description |
|-----------------|---------------------------|-----------|---|
| HSADC Interface | hsadc_clkout | I/O | hsadc input /output clock |
| | hsadc_datai($i=0\sim9$) | I | hsadc($i=0\sim9$)/tsi($i=0\sim7$)/gps data($i=0,1$) |
| | hsadc_sync | I | ts synchronizer signal |
| | hsadc_valid | I | ts valid signal |
| | hsadc_fail | I | ts fail signal |
| | gps_clk | I | hsadc/tsi/gps reference clock |

| Interface | Pin Name | Direction | Description |
|---------------|-------------------------|-----------|-------------------------|
| TSP Interface | ts0_clk | I/O | TSI reference clock |
| | ts0_datai($i=0\sim7$) | I | TSI data($i=0\sim7$) |
| | ts0_sync | I | TSI synchronizer signal |
| | ts0_valid | I | TSI valid signal |
| | ts0_err | I | TSI fail signal |

| Interface | Pin Name | Direction | Description |
|--------------------|------------------------|-----------|---|
| I2S/PCM Controller | i2s_clk | O | I2S/PCM1 clock source |
| | i2s_sclk | I/O | I2S/PCM1 serial clock |
| | i2s_lrckrx | I/O | I2S/PCM1 left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode |
| | i2s_sdi | I | I2S/PCM1 serial data input |
| | i2s_sdoi($i=0\sim9$) | O | I2S/PCM1 serial data output |
| | i2s_lrcktx | I/O | I2S/PCM1 left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode |

| Interface | Pin Name | Direction | Description |
|-------------------|----------|-----------|--------------------------|
| SPDIF transmitter | spdif_tx | O | spdif biphas data output |

| Interface | Pin Name | Direction | Description |
|----------------|---------------------------------|-----------|------------------------------------|
| SPI Controller | spix_clk($x=0,2$) | I/O | spi serial clock |
| | spix_csny($x=0,2$)($y=0,1$) | I/O | spi chip select signal, low active |
| | spix_txd($x=0,2$) | O | spi serial data output |

| Interface | Pin Name | Direction | Description |
|-----------|-----------------|-----------|-----------------------|
| | spix_rxd(x=0,2) | I | spi serial data input |

| Interface | Pin Name | Direction | Description |
|-----------|------------------------------|-----------|---|
| LCD | lcdc0_dclk | O | LDC RGB interface display clock out, MCU i80 interface RS signal |
| | lcdc0_vsync | O | LDC RGB interface vertical sync pulse, MCU i80 interface CSN signal |
| | lcdc0_hsync | O | LDC RGB interface horizontal sync pulse, MCU i80 interface WEN signal |
| | lcdc0_den | O | LDC RGB interface data enable, MCU i80 interface REN signal |
| | lcdc0_data <i>i</i> (i=0~23) | O | LDC data output |
| | vop0_pwm | O | VOP_BIG CABAC PWM control signal |
| | vop1_pwm | O | VOP_LIT CABAC PWM control signal |

| Interface | Pin Name | Direction | Description |
|-----------|----------------------------|-----------|--|
| Camera IF | cif_clk | I | Camera0 interface input pixel clock |
| | cif_clkout | O | Camera0 interface output work clock |
| | cif_vsync | I | Camera0 interface vertical sync signal |
| | cif_href | I | Camera0 interface horizontal sync signal |
| | cif_data <i>i</i> (i=0~11) | I | Camera0 interface input pixel data |

| Interface | Pin Name | Direction | Description |
|-----------|----------|-----------|-------------------------------|
| PWM | pwm3 | I/O | Pulse Width Modulation output |
| | pwm2 | I/O | Pulse Width Modulation output |
| | pwm1 | I/O | Pulse Width Modulation output |
| | pwm0 | I/O | Pulse Width Modulation output |

| Interface | Pin Name | Direction | Description |
|-----------|------------|-----------|---------------------|
| GPS | gps_rfcclk | I | GPS reference clock |
| | gps_sig | I | GPS SIG input |
| | gps_mag | I | GPS MAG input |

| Interface | Pin Name | Direction | Description |
|-----------|----------|-----------|------------------|
| PS2 | ps2_clk | I/O | P2S clock signal |
| | ps2_data | I/O | P2S data signal |

| Interface | Pin Name | Direction | Description |
|-----------|----------------|-----------|-------------------|
| I2C | i2c0pmu_sda | I/O | I2C_PMU data |
| | i2c0pmu_scl | I/O | I2C_PMU clock |
| | i2c1sensor_sda | I/O | I2C1_SENSOR data |
| | i2c1sensor_scl | I/O | I2C1_SENSOR clock |
| | i2c2audio_sda | I/O | I2C2_AUDIO data |
| | i2c2audio_scl | I/O | I2C2_AUDIO clock |
| | i2c3cam_sda | I/O | I2C3_CAM data |
| | i2c3cam_scl | I/O | I2C3_CAM clock |
| | i2c4tp_sda | I/O | I2C4_TP data |

| Interface | Pin Name | Direction | Description |
|-----------|--------------|-----------|-----------------|
| | i2c4tp_scl | I/O | I2C4_TP clock |
| | i2c4hdmi_sda | I/O | I2C5_HDMI data |
| | i2c4hdmi_scl | I/O | I2C5_HDMI clock |

| Interface | Pin Name | Direction | Description |
|-----------|---------------|-----------|------------------------------|
| UART | uart0bt_sin | I | UART_BT searial data input |
| | uart0bt_sout | O | UART_BT searial data output |
| | uart0bt_ctsn | I | UART_BT clear to send |
| | uart0bt_rtsn | O | UART_BT request to send |
| | uart1bb_sin | I | UART_BB searial data input |
| | uart1bb_sout | O | UART_BB searial data output |
| | uart1bb_ctsn | O | UART_BB clear to send |
| | uart1bb_rtsn | I | UART_BB request to send |
| | uart2dbg_sin | I | UART_DBG searial data input |
| | uart2dbg_sout | O | UART_DBG searial data output |
| | uart3gps_sin | I | UART_GPS searial data input |
| | uart3gps_sout | O | UART_GPS searial data output |
| | uart3gps_ctsn | I | UART_GPS clear to send |
| | uart3gps_rtsn | O | UART_GPS request to send |
| | uart4exp_sin | I | UART_EXP searial data input |
| | uart4exp_sout | O | UART_EXP searial data output |
| | uart4exp_ctsn | I | UART_EXP clear to send |
| | uart4exp_rtsn | O | UART_EXP request to send |

| Interface | Pin Name | Direction | Description |
|-----------|------------------------|-----------|--|
| GMAC | mac_clk | I/O | RMII REC_CLK output or GMAC external clock input |
| | mac_txclk | O | RGMIITX clock output |
| | mac_rxclk | I | RGMIIRX clock input |
| | mac_mdc | O | GMAC management interface clock |
| | mac_mdio | I/O | GMAC management interface data |
| | mac_txd <i>(i=0~3)</i> | O | GMAC TX data |
| | max_rxd <i>(i=0~3)</i> | I | GMAC RX data |
| | mac_txen | O | GMAC TX data enable |
| | mac_rxdv | I | GMAC RX data valid signal |
| | mac_rxer | I | GMAC RX error signal |
| | mac_col | I | PHY Collision signal |
| | mac_crs | I | PHY CRS signal |

| Interface | Pin Name | Direction | Description |
|----------------|---------------------------|-----------|--|
| HOST interface | host_dini <i>(i=0~7)</i> | I/O | Host data(8bit for input or output) |
| | host_dout <i>(i=0~15)</i> | I/O | Host data(16bit for input or output) |
| | host_ckinp | I/O | Host differential clock p pin(for input or output) |
| | host_ckinn | I/O | Host differential clock n pin(for input or output) |
| | host_ckoutp | I/O | Host differential clock p pin(for input or output) |
| | host_ckoutn | I/O | Host differential clock n pin(for input or output) |

| Interface | Pin Name | Direction | Description |
|-----------|------------|-----------|-----------------------------------|
| | host_wkack | I | Host interface wakeup acknowledge |
| | host_wkreq | O | Host interface wakeup request |

| Interface | Pin Name | Direction | Description |
|-------------|-------------|-----------|--|
| USB OTG 2.0 | OTG_DM | N/A | USB OTG 2.0 Data signal DM |
| | OTG_RKELVIN | N/A | USB OTG 2.0 Transmitter Kelvin Connection to Resistor Tune Pin |
| | OTG_DP | N/A | USB OTG 2.0 Data signal DP |
| | OTG_VBUS | N/A | USB OTG 2.0 5-V power supply pin |
| | usb_drvvbus | O | USB OTG 2.0 drive VBUS |

| Interface | Pin Name | Direction | Description |
|-----------------------------|------------------------|-----------|--|
| USB Host 2.0 (2 channel) | HOSTx_DM($x=0,1$) | N/A | USB HOST 2.0 Data signal DM |
| | HOSTx_RBIAS($x=0,1$) | N/A | 135 Ω Reference external resistance |
| | HOSTx_DP($x=0,1$) | N/A | USB HOST 2.0 Data signal DP |

| Interface | Pin Name | Direction | Description |
|-----------|-------------|-----------|--------------------|
| USIC | USIC_DATA | N/A | USIC DATA signal |
| | USIC_STROBE | N/A | USIC STROBE signal |

| Interface | Pin Name | Direction | Description |
|-----------|---------------------------------|-----------|------------------------------------|
| SAR-ADC | SARADC_AIN[i] ($i=0\sim2$) | N/A | SAR-ADC input signal for 3 channel |

| Interface | Pin Name | Direction | Description |
|-----------|------------|-----------|-------------------------------|
| eFuse | EFUSE_VDDQ | N/A | eFuse program and sense power |

| Interface | Pin Name | Direction | Description |
|-----------|-----------|-----------|--------------------------------|
| SIM Card | sc_clk | O | Smart card clock output |
| | sc_rst | O | Smart card reset output |
| | sc_io | I/O | Smart card data |
| | sc_detect | O | Smart card detect input |
| | sc_vcc18v | O | Smart card 1.8V voltage select |
| | sv_vcc33v | O | Smart card 3.3V voltage select |

| Interface | Pin Name | Direction | Description |
|-----------|------------------|-----------|--------------------------------|
| ISP | isp_shutteren | O | Hold signal for shutter open |
| | isp_flashtrigout | O | Hold signal for flash light |
| | isp_prelighttrig | O | Hold signal for prelight |
| | isp_shuttertrig | I | External shutter trigger pulse |
| | isp_flashtrigin | I | External flash trigger pulse |

| Interface | Pin Name | Direction | Description |
|-----------|-------------------------|-----------|-------------------------------|
| LVDS | LVDS_PADP($i=0\sim9$) | I/O | LVDS/TTL data lane serial pin |

| Interface | Pin Name | Direction | Description |
|-----------|--------------------------|-----------|--|
| | LVDS_PADNi($i=0\sim9$) | I/O | LVDS/TTL data lane serial pin |
| | LVDS_CLKPi($i=0\sim1$) | I/O | LVDS clock lane/TTL data lane serial pin |
| | LVDS_CLKNi($i=0\sim1$) | I/O | LVDS clock lane/TTL data lane serial pin |

| Interface | Pin Name | Direction | Description |
|-----------|------------------------|-----------|---|
| eDP | EDP_TXiP($i=0\sim3$) | O | eDP data lane positive output |
| | EDP_TXiN($i=0\sim3$) | O | eDP data lane negative output |
| | EDP_DC_TP | O | eDP PHY DC test point |
| | EDP_AUXP | I/O | eDP CH-AUX positive differential output |
| | EDP_AUXN | I/O | eDP CH-AUX negative differential output |
| | EDP_R_BIAS | I | Let it floating |
| | EDP_OSC_CLK_24M | I | 24MHz input reference clock |
| | edp_hotplug | I | eDP external hot plug signal |
| | edphdmi_cecinout | I/O | eDP HDMI CEC bus |
| | edphdmii2c_sda | I/O | eDP HDMI I2C data |
| | edphdmii2c_scl | I/O | eDP HDMI I2C clock |

| Interface | Pin Name | Direction | Description |
|-----------|-------------------------------|-----------|--|
| HDMI | HDMI_TMDSDATANi($i=0\sim2$) | O | HDMI negative TMDS differential line driver data output |
| | HDMI_TMDSDATAPi($i=0\sim2$) | O | HDMI positive TMDS differential line driver data output |
| | HDMI_TMDSCLKN | O | HDMI negative TMDS differential line driver clock output |
| | HDMI_TMDSCLKP | O | HDMI positive TMDS differential line driver clock output |
| | HDMI_RESREF | I/O | HDMI reference resistor connection |
| | HDMI_HPD | I/O | HDMI hot plug detect signal |
| | HDMI_DDCCEC | I/O | HDMI ground reference for the hot plug detect signal |



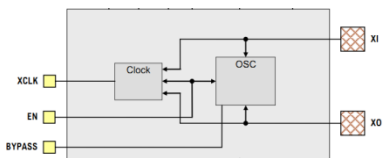
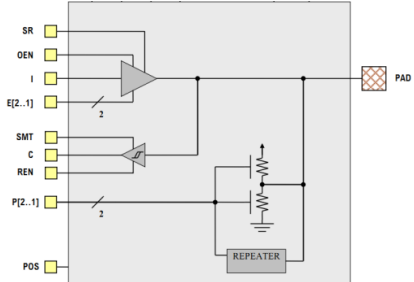
| Interface | Pin Name | Direction | Description |
|-----------|--------------------------------|-----------|---|
| MIPI | MIPI_TXRX_DATANi($i=0\sim3$) | I/O | MIPI TXRX negative differential data line transceiver output |
| | MIPI_TXRX_DATAPi($i=0\sim3$) | I/O | MIPI TXRX positive differential data line transceiver output |
| | MIPI_TXRX_CLKP | I/O | MIPI TXRX positive differential clock line transceiver output |
| | MIPI_TXRX_CLKN | I/O | MIPI TXRX negative differential clock line transceiver output |
| | MIPI_TXRX_REXT | I/O | MIPI TXRX external resistor connection |
| | MIPI_TX0_DATANi($i=0\sim3$) | I/O | MIPI TX0 negative differential data line transceiver output |
| | MIPI_TX0_DATAPi($i=0\sim3$) | I/O | MIPI TX0 positive differential data line transceiver output |
| | MIPI_TX0_CLKP | I/O | MIPI TX0 positive differential clock line transceiver output |
| | MIPI_TX0_CLKN | I/O | MIPI TX0 negative differential clock line transceiver output |
| | MIPI_TX0_REXT | I/O | MIPI TX0 external resistor connection |
| | MIPI_RX0_DATANi($i=0\sim3$) | I/O | MIPI RX0 negative differential data line transceiver output |
| | MIPI_RX0_DATAPi($i=0\sim3$) | I/O | MIPI RX0 positive differential data line transceiver output |
| | MIPI_RX0_CLKP | I/O | MIPI RX0 positive differential clock line transceiver output |

| Interface | Pin Name | Direction | Description |
|-----------|---------------|-----------|--|
| | MIPI_RX0_CLKN | I/O | MIPI RX0 negative differential clock line transceiver output |
| | MIPI_RX0_REXT | I/O | MIPI RX0 external resistor connection |

2.9 IO Type

The following list shows IO type except DDR IO and all of Power/Ground IO.

Table 2-4 RK3288 IO Type List

| Type | Diagram | Description | Pin Name |
|------|--|--|----------------------|
| A |  | Analog IO Cell with IO voltage | EFUSE_VQPS |
| B |  | Dedicated Power supply to Internal Macro with IO voltage | SARADC_AIN[2:0] |
| C |  | Crystal Oscillator with high enable | XIN24M/XOUT24M |
| D |  | Tri-state output pad with input, which pullup/pulldown, slew rate and drive strength is configurable | Part of digital GPIO |

Chapter 3 Electrical Specification

3.1 Absolute Maximum Ratings

Table 3-1 RK3288 absolute maximum ratings

| Parameters | Related Power Group | Max | Unit |
|---|--|--------------------|------|
| DC supply voltage for CPU | CPU_VDD, | 1.5 | V |
| DC supply voltage for Internal digital logic | LOGIC_VDD | 1.5 | V |
| DC supply voltage for GPU | GPU_VDD | 1.5 | V |
| DC supply voltage for PMU | PMU_VDD_1V0, | 1.2 | V |
| DC supply voltage for Analog part of USB | USB_AVDD_1V0 | 1.2 | V |
| DC supply voltage for Digital GPIO (except for SAR-ADC, PLL, USB, DDR, MIPI PHY, LVDS, eDP, HDMI IO) | PMUIO_VDD APIO1_VDD APIO2_VDD APIO3_VDD APIO4_VDD APIO5_VDD LDC_VDD SDMMC0_VDD FLASH0_VDD FLASH1_VDD DVPIO_VDD | 3.6 | V |
| DC supply voltage for DDR IO | DDR0_VDD DDR1_VDD DDR0_VDDAO DDR1_VDDAO | 1.65 | V |
| DC supply voltage for Analog part of PLL | PLL_AVDD_1V0 | 1.2 | V |
| DC supply voltage for Analog part of USB OTG/Host2.0 | USB_AVDD_1V8 USB_AVDD_3V3 | 1.98 3.63 | V |
| DC supply voltage for Analog part of USIC | USIC_AVDD_1V2 | 1.32 | V |
| Analog Input voltage for SAR-ADC/TS-ADC | ADC_AVDD_1V8 | 1.98 | V |
| DC supply voltage for Analog part of LVDS | LVDS_AVDD_1V0 LVDS_AVDD_1V8 LVDS_AVDD_3V3 | 1.2 1.98 3.6 | V |
| DC supply voltage for Analog part of eDP | EDP_AVDD_1V0 EDP_AVDD_1V8 | 1.2 1.98 | V |
| DC supply voltage for Analog part of HDMI | HDMI_AVDD_1V0 HDMI_AVDD_1V8 | 1.2 1.98 | V |
| DC supply voltage for Analog part of MIPI PHY | MIPI_TX/RX_AVDD_1V8 MIPI_TX_AVDD_1V8 MIPI_RX_AVDD_1V8 | 1.98 | V |
| Analog Input voltage for DP/DM/VBUS of USB OTG/Host2.0 | | 5.0 | V |
| Digital input voltage for input buffer of GPIO | | 3.6 | V |
| Digital output voltage for output buffer of GPIO | | 3.6 | V |
| Highest Storage Temperature | Tstg | 125 | °C |
| Lowest Storage Temperature | Tstg | -40 | °C |
| Max Conjunction Temperature | Tj | 125 | °C |

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

3.2 Recommended Operating Conditions

Table 1-6 describes the recommended operating condition for every clock domain.

Table 3-2 RK3288 recommended operating conditions

| Parameters | Symbol [®] | Min | Typ | Max | Units |
|------------------------------|---------------------|-----|-----|------|-------|
| Internal CPU Power | CPU_VDD, | 0.9 | 1.0 | 1.4 | V |
| Internal digital logic Power | LOGIC_VDD, | 0.9 | 1.0 | 1.35 | V |

| Parameters | Symbol [®] | Min | Typ | Max | Units |
|--|---|---------------------|-------------------|---------------------|-------|
| Internal GPU Power | GPU_VDD, | 0.9 | 1.0 | 1.35 | V |
| Internal digital logic Power | PMU_VDD_1V0 | 0.9 | 1.0 | 1.1 | V |
| Digital GPIO Power(3.3V/2.5V/1.8V) | PMUIO_VDD APIO1_VDD APIO2_VDD APIO3_VDD APIO4_VDD APIO5_VDD LCDC_VDD SDMMC0_VDD FLASH0_VDD FLASH1_VDD DVPIO_VDD | 3.0 2.25 1.62 | 3.3 2.5 1.8 | 3.6 2.75 1.98 | V |
| DDR IO (DDR3 mode) Power | DDR0_VDD DDR1_VDD DDR0_VDDAO DDR1_VDDAO | 1.425 | 1.5 | 1.575 | V |
| DDR IO (DDR3L mode) Power | DDR0_VDD DDR1_VDD DDR0_VDDAO DDR1_VDDAO | 1.283 | 1.35 | 1.45 | V |
| DDR IO (LPDDR2/LPDDR3 mode) Power | DDR0_VDD DDR1_VDD DDR0_VDDAO DDR1_VDDAO | 1.14 | 1.2 | 1.3 | V |
| DDR reference supply (VREF) Input | VREF | 0.49* DDR_VDD | 0.5* DDR_VDD | 0.51*DDR_VDD | V |
| DDR External termination voltage | | VREF- 40mV | VREF | VREF+ 40mV | V |
| PLL Analog Power | PLL_AVDD_1V0 | 0.9 | 1.0 | 1.1 | V |
| SAR-ADC/TSADC Analog Power | ADC_AVDD_1V8 | 1.62 | 1.8 | 1.98 | V |
| USB OTG/Host2.0 Digital Power | USB_AVDD_1V0 | 0.9 | 1.0 | 1.1 | V |
| USB OTG/Host2.0 Analog Power(1.8V) | USB_AVDD_1V8 | 1.62 | 1.8 | 1.98 | V |
| USB OTG/Host2.0 Analog Power(3.3V) | USB_AVDD_3V3 | 3.0 | 3.3 | 3.6 | V |
| USB OTG/Host2.0 external resistor | REXT | NA | 200 | NA | Ohm |
| USIC Analog Power | USIC_AVDD_1V2 | 1.0 | 1.2 | 1.32 | V |
| LVDS Analog Power(1.0V) | LVDS_AVDD_1V0 | 0.9 | 1.0 | 1.1 | V |
| LVDS Analog Power(1.8V) | LVDS_AVDD_1V8 | 1.62 | 1.8 | 1.98 | V |
| LVDS Analog Power(3.3V) | LVDS_AVDD_3V3 | 3.0 | 3.3 | 3.6 | V |
| eDP Analog Power(1.0V) | EDP_AVDD_1V0 | 0.9 | 1.0 | 1.1 | V |
| eDP Analog Power(1.8V) | EDP_AVDD_1V8 | 1.62 | 1.8 | 1.98 | V |
| HDMI Analog Power(1.0V) | HDMI_AVDD_1V0 | 0.9 | 1.0 | 1.1 | V |
| HDMI Analog Power(1.8V) | HDMI_AVDD_1V8 | 1.62 | 1.8 | 1.98 | V |
| MIPI PHY Analog Power | MIPI_TXRX_AVDD_1V8 MIPI_TX_AVDD_1V8 MIPI_RX_AVDD_1V8 | 1.62 | 1.8 | 1.98 | V |
| PLL input clock frequency | | N/A | 24 | N/A | MHz |
| SDIO IO frequency | | N/A | N/A | 150 | MHz |
| Max CPU frequency 0℃~80℃ | RK3288 | N/A | N/A | 1.6 | GHz |
| | RK3288 W version | N/A | N/A | 1.6 | GHz |
| | RK3288-D | N/A | N/A | 1.6 | GHz |
| | RK3288-CG | N/A | N/A | 1.8 | GHz |
| | RK3288-CG W Version | N/A | N/A | 1.8 | GHz |
| | RK3288-C | N/A | N/A | 1.8 | GHz |
| Max CPU frequency ^② -20℃~0℃and 80℃~85℃ | RK3288K | N/A | N/A | 1.8 | GHz |
| | RK3288K | N/A | N/A | 1.6 | GHz |

| Parameters | Symbol ^① | Min | Typ | Max | Units |
|---|---------------------|-----|-----|-----|-------|
| Max GPU frequency 0℃~80℃ | RK3288 | N/A | N/A | 500 | MHz |
| | RK3288 W version | N/A | N/A | 500 | MHz |
| | RK3288-D | N/A | N/A | 500 | MHz |
| | RK3288-CG | N/A | N/A | 600 | MHz |
| | RK3288-CG W Version | N/A | N/A | 600 | MHz |
| | RK3288-C | N/A | N/A | 600 | MHz |
| | RK3288K | N/A | N/A | 600 | MHz |
| Max GPU frequency ^② -20℃~0℃and 80℃~85℃ | RK3288K | N/A | N/A | 500 | MHz |
| Ambient Operating Temperature for RK3288, RK3288 W Version, RK3288-C, RK3288-CG, RK3288-CG W Version, RK3288-D, | Ta | 0 | 25 | 80 | ℃ |
| Ambient Operating Temperature for RK3288K | Ta | -20 | 25 | 85 | ℃ |

Notes :

- ① Symbol name is same as the pin name in the io descriptions
- ② The max frequency is affected by the heat emission condition and the temperature control system.

3.3 DC Characteristics

Table 3-3 RK3288 DC Characteristics

| Parameters | | Symbol | Min | Typ | Max | Units |
|--------------------------------------|--|---------|-----------------|-----------------|-----------------|-------|
| Digital GPIO @3.3V | Input Low Voltage | Vil | -0.3 | 0 | 3.3x0.3 | V |
| | Input High Voltage | Vih | 3.3x0.7 | 3.3 | 3.3+0.3 | V |
| | Output Low Voltage | Vol | -0.3 | NA | NA | V |
| | Output High Voltage | Voh | NA | NA | 3.6 | V |
| | Pullup Resistor | Rpu | 33.7 | 58 | 101.5 | Kohm |
| | Pulldown Resistor | Rpd | 34.2 | 60.1 | 109.3 | Kohm |
| Digital GPIO @1.8V | Input Low Voltage | Vil | -0.3 | 0 | 1.8x0.3 | V |
| | Input High Voltage | Vih | 1.8x0.7 | 1.8 | 1.8 + 0.3 | V |
| | Output Low Voltage | Vol | -0.3 | NA | NA | V |
| | Output High Voltage | Voh | NA | NA | 1.8+0.3 | V |
| | Pullup Resistor | Rpu | 35 | 62.9 | 120 | Kohm |
| | Pulldown Resistor | Rpd | 35.1 | 61 | 113.9 | Kohm |
| DDR IO @DDR3 mode | Input High Voltage | Vih_ddr | VREF + 0.09 | NA | MVDD | V |
| | Input Low Voltage | Vil_ddr | -0.3 | 0 | VREF - 0.09 | V |
| | Output High Voltage | Voh_ddr | 0.8xMVDD | NA | N/A | V |
| | Output Low Voltage | Vol_ddr | N/A | NA | 0.2*MVDD | V |
| | Input termination resistance(ODT) to VDDIO_DDRi/2 (i=0~6) | Rtt | 100 54 36 | 120 60 40 | 140 66 44 | Ohm |
| DDR IO @DDR3L mode | Input High Voltage | Vih_ddr | VREF + 0.09 | NA | MVDD | V |
| | Input Low Voltage | Vil_ddr | -0.3 | 0 | VREF - 0.09 | V |
| | Output High Voltage | Voh_ddr | 0.8xMVDD | NA | N/A | V |
| | Output Low Voltage | Vol_ddr | N/A | NA | 0.2*MVDD | V |
| | Input termination resistance(ODT) to VDDIO_DDRi/2 (i=0~6) | Rtt | 100 54 36 | 120 60 40 | 140 66 44 | Ohm |
| DDR IO @LPDDR2/ LPDDR3 mode | Input High Voltage | Vih_ddr | VREF + 0.13 | NA | MVDD | V |
| | Input Low Voltage | Vil_ddr | -0.3 | NA | VREF - 0.13 | V |
| | Output High Voltage | Voh_ddr | 0.9*VREF | NA | NA | V |

| Parameters | | Symbol | Min | Typ | Max | Units |
|--------------------------|--|--------------|---------------|-----|--------------|---------|
| | Output Low Voltage | Vol_dds | NA | NA | 0.1*VREF | V |
| LVDS IO @LVDS mode | Output High Voltage | Voh | NA | NA | 1060 | mV |
| | Output Low Voltage | Vol | 660 | NA | NA | mV |
| | Output differential voltage | Vod | 202 | NA | 354 | mV |
| | Output offset voltage | Vos | 885 | NA | 915 | mV |
| | Output impedance, single ended | Ro | 40 | NA | 140 | Ω |
| | Ro mismatch between A & B | ΔRo | NA | NA | 10 | % |
| | Change in Vod between 0 and 1 | ΔVod | NA | NA | 25 | mV |
| | Change in Vod between 0 and 1 | ΔVos | NA | NA | 25 | mV |
| LVDS IO @TTL mode | Output High Voltage | Voh | 3 | 3.3 | NA | V |
| | Output Low Voltage | Vol | NA | 0 | 0.2 | V |
| | Input High Current | Iih | NA | ±1 | ±10 | uA |
| | Input Low Current | Iil | NA | ±1 | ±10 | uA |
| | Short-Circuit Output Current | Ios | NA | 35 | 60 | mA |
| | Output impedance | Ro | 40 | NA | 460 | Ω |
| | Device active current | Icc | 17 | 20 | 23 | mA/lane |
| HDMI | Single-ended standby voltage | Voff | avddtmds±10 | | | mV |
| | Single-ended output swing voltage RT=50Ω | Vswing | 400 | NA | 600 | mV |
| | | Vswing_data | 400 | NA | 600 | mV |
| | | Vswing_clock | 200 | NA | 600 | mV |
| | Single-ended output high voltage | Vh | avddtmds±10 | | | mV |
| | | | avddtmds-200 | NA | avddtmds+10 | mV |
| | | Vh_data | avddtmds-400 | NA | avddtmds+10 | mV |
| | | Vh_clock | avddtmds-400 | NA | avddtmds+10 | mV |
| | Single-ended output low voltage | VI | avddtmds-600 | NA | avddtmds-400 | mV |
| | | | avddtmds-700 | NA | avddtmds-400 | mV |
| | | VI_data | avddtmds-1000 | NA | avddtmds-400 | mV |
| | | VI_clock | avddtmds-1000 | NA | avddtmds-200 | mV |
| | Differential source termination load | Rterm | 50 | NA | 200 | Ω |
| MIPI PHY | Input signal voltage range | Vi | -50 | NA | 1350 | mV |
| | Input leakage current | Ileak | -10 | NA | 10 | uA |
| | Ground | Vgndsh | -50 | NA | 50 | mV |
| | Maximum transient output voltage level | Voh(absmax) | -0.15 | NA | 1.45 | V |
| | Maximum transient time above Voh(absmax) | tVoh(absmax) | NA | NA | 20 | ns |
| | HS transmit differential output voltage magnitude | Vod | 140 | 200 | 270 | mV |
| | Change in differential output voltage magnitude between logic states | Δ Vod | NA | NA | 14 | mV |
| | Steady-state common-mode output voltage | Vcmtx | 150 | 200 | 250 | mV |
| | Change in steady-state common-mode output voltage between logic states | ΔVcmtx(1,0) | NA | NA | 5 | mV |
| | HS output high voltage | Vohhs | NA | NA | 360 | mV |
| | Single-ended output impedance | Zos | 40 | 50 | 62.5 | Ω |
| | Single-ended output impedance mismatch | ΔZos | NA | NA | 10 | Ω |
| | Output low-level SE output | Vol | -50 | NA | 50 | mV |
| | Output high-level SE output | Voh | 1.1 | 1.2 | 1.3 | V |
| | Single-ended output impedance | Zolp | 110 | NA | NA | Ω |
| | Single-ended output impedance mismatch driving opposite level | ΔZolp(01,10) | NA | NA | 20 | % |
| | Single-ended output impedance mismatch driving same level | ΔZolp(00,11) | NA | NA | 5 | % |

| Parameters | | Symbol | Min | Typ | Max | Units |
|------------|---|--------|-----|-----|-----|----------|
| | Differential input high voltage threshold | Vidth | NA | NA | 70 | mV |
| | Differential input low voltage threshold | Vidtl | -70 | NA | NA | mV |
| | Single ended input high voltage | Vihhs | NA | NA | 460 | mV |
| | Single ended input low voltage | Vilhs | -40 | NA | NA | mV |
| | Input common mode voltage | Vcmrxd | 70 | NA | 330 | mV |
| | Differential input impedance | Zid | 80 | NA | 125 | Ω |
| | Input low voltage | Vil | NA | NA | 550 | mV |
| | Input high voltage | Vih | 880 | NA | NA | mV |
| | Input hysteresis | Vhyst | 25 | NA | NA | mV |
| | Input low fault threshold | Vilf | NA | NA | 200 | mV |
| | Input high fault threshold | Vihf | 450 | NA | NA | mV |

3.4 Electrical Characteristics for General IO

Table 3-4 RK3288 Electrical Characteristics for Digital General IO

| Parameters | | Symbol | Test condition | Min | Typ | Max | Units |
|--------------------|----------------------------------|--------|-------------------------------|-----|-----|-------|---------|
| Digital GPIO @3.3V | Input leakage current | Ii | Vin = 3.3V or 0V | NA | NA | 10 | μ A |
| | Tri-state output leakage current | Ioz | Vout = 3.3V or 0V | NA | NA | 10 | μ A |
| | High level input current | Iih | Vin = 3.3V, pulldown disabled | NA | NA | 10 | μ A |
| | | | Vin = 3.3V, pulldown enabled | NA | NA | 106.4 | μ A |
| | Low level input current | Iil | Vin = 0V, pullup disabled | NA | NA | 10 | μ A |
| | | | Vin = 0V, pullup enabled | NA | NA | 107.8 | μ A |
| Digital GPIO @1.8V | Input leakage current | Ii | Vin = 1.8V or 0V | NA | NA | 10 | μ A |
| | Tri-state output leakage current | Ioz | Vout = 1.8V or 0V | NA | NA | 10 | μ A |
| | High level input current | Iih | Vin = 1.8V, pulldown disabled | NA | NA | 10 | μ A |
| | | | Vin = 1.8V, pulldown enabled | NA | NA | 61.3 | μ A |
| | Low level input current | Iil | Vin = 0V, pullup disabled | NA | NA | 10 | μ A |
| | | | Vin = 0V, pullup enabled | NA | NA | 61.4 | μ A |

3.5 Electrical Characteristics for PLL

Table 3-5 RK3288 Electrical Characteristics for PLL

| Parameters | | Symbol | Test condition | Min | Typ | Max | Units |
|------------|-----------------------------------|--------|----------------|-------|-----|--------|-----------------------------------|
| PLL | Divided reference frequency range | Fin | | 0.269 | NA | 2200 | MHz |
| | output frequency range | Fout | | 0.440 | N/A | 2200 | MHz |
| | Lock time | Tlt | | N/A | NA | 500 | Cycles of divided reference clock |
| | Power consumption (normal mode) | N/A | | N/A | 3 | N/A | mW |
| | Period jitter (P-P) | N/A | | N/A | NA | +/-2.5 | % |
| | Junction temperature | N/A | | | 70 | 125 | $^{\circ}$ C |

3.6 Electrical Characteristics for SAR-ADC

Table 3-6 RK3288 Electrical Characteristics for SAR-ADC

| Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|------------------------------------|---------|--|-----|-----|-----|-------|
| ADC resolution | | | N/A | 10 | N/A | bits |
| Conversion speed | Fs | The duty cycle should be between 40%~60% | NA | N/A | 1 | MSPS |
| Differential Non Linearity | DNL | | N/A | ±1 | N/A | LSB |
| Integral Non Linearity | INL | | N/A | ±2 | N/A | LSB |
| Gain Error | Egain | | -8 | N/A | 8 | LSB |
| Offset Error | Eoffset | | -8 | N/A | 8 | mV |
| Analog Supply Current(VDDA_SARADC) | | | N/A | 200 | N/A | uA |
| Digital Supply Current | | | N/A | 50 | N/A | uA |
| Power Down Current from AVDD | | | NA | 0.5 | NA | uA |
| Power Down Current from DVDD | | | N/A | 1 | N/A | uA |
| Power up time | | | N/A | 7 | N/A | 1/Fs |

3.7 Electrical Characteristics for TSADC

Table 3-7 RK3288 Electrical Characteristics for TSADC

| Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|------------------------------|--------|----------------|-----|-----|------|-------|
| ADC resolution | | | N/A | 12 | N/A | bits |
| TSADC Accuracy | Fs | | NA | N/A | +/-5 | °C |
| Active power | | | N/A | 0.4 | N/A | mW |
| Clock Frequency | Fclk | | NA | NA | 50 | KHz |
| Power Down Current from AVDD | | | NA | 1 | NA | uA |
| Power Down Current from DVDD | | | N/A | 2 | N/A | uA |
| Power up time | | | N/A | 7 | N/A | 1/Fs |

3.8 Electrical Characteristics for USB Interface

Table 3-8 RK3288 Electrical Characteristics for USB Interface

| Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|---|------------------------|---|-----|-------|-----|-------|
| HS transmit, maximum transition density (all 0's data in DP/DM) | Current From OTG_DVDD | 55°C ,USBVDD_1V0 = 1.0V USBVDD_1V8=1.8V USBVDD_3V3=3.3V, 15-cm USB cable attached to DP/DM | N/A | 6.151 | N/A | mA |
| | Current From OTG_VDD33 | | N/A | 4.97 | N/A | mA |
| | Current From OTG_VDD18 | | N/A | 18.5 | N/A | mA |
| HS transmit, minimum transition density (all 1's data in DP/DM) | Current From OTG_DVDD | | N/A | 5.521 | N/A | mA |
| | Current From OTG_VDD33 | | N/A | 3.63 | N/A | mA |
| | Current From OTG_VDD18 | | N/A | 15.5 | N/A | mA |
| HS idle mode | Current From OTG_DVDD | | N/A | 5.841 | N/A | mA |
| | Current From OTG_VDD33 | | N/A | 3.19 | N/A | mA |
| | Current From OTG_VDD18 | | N/A | 6.58 | N/A | mA |
| FS transmit, maximum transition density (all 0's data in DP/DM) | Current From OTG_DVDD | | N/A | 4.251 | N/A | mA |
| | Current From OTG_VDD33 | | N/A | 11.81 | N/A | mA |

| Parameters | | Symbol | Test condition | Min | Typ | Max | Units |
|---|------------------------|--------|----------------|-----|-------|-----|-------|
| DP/DM) | Current From OTG_VDD18 | | | N/A | 6.56 | N/A | mA |
| LS transmit, maximum transition density (all 0's data in DP/DM) | Current From OTG_DVDD | | | N/A | 5.171 | N/A | mA |
| | Current From OTG_VDD33 | | | N/A | 12.81 | N/A | mA |
| | Current From OTG_VDD18 | | | N/A | 6.61 | N/A | mA |
| Suspend mode | Current From OTG_DVDD | | | N/A | 53.4 | N/A | uA |
| | Current From OTG_VDD33 | | | N/A | 1.1 | N/A | uA |
| | Current From OTG_VDD18 | | | N/A | 6.6 | N/A | uA |
| Sleep mode | Current From OTG_DVDD | | | N/A | 0.113 | N/A | mA |
| | Current From OTG_VDD33 | | | N/A | 0.1 | N/A | uA |
| | Current From OTG_VDD18 | | | N/A | 0.004 | N/A | mA |

3.9 Electrical Characteristics for USIC Interface

Table 3-9 RK3288 Electrical Characteristics for USIC Interface

| Parameters | | Symbol | Test condition | Min | Typ | Max | Units |
|---|--------------------|--------|--|-----|-------|-----|-------|
| HS transmit, maximum transition density | Current From DVDD | | 55°C , VDD12 = 1.2V, DVDD = 1.0V , 12MHz reference clock 10pF load on STROBE | N/A | 3.26 | N/A | mA |
| | Current From VDD12 | | | N/A | 10.20 | N/A | mA |
| HS transmit, minimum transition density | Current From DVDD | | | N/A | 3.05 | N/A | mA |
| | Current From VDD12 | | | N/A | 8.28 | N/A | mA |
| HS idle mode | Current From DVDD | | | N/A | 2.71 | N/A | mA |
| | Current From VDD12 | | | N/A | 0.001 | N/A | mA |
| HS Receive | Current From DVDD | | | N/A | 3.07 | N/A | mA |
| | Current From VDD12 | | | N/A | 1.58 | N/A | mA |
| Suspend mode | Current From DVDD | | | N/A | 0.012 | N/A | mA |
| | Current From VDD12 | | | N/A | 0.3 | N/A | uA |
| Sleep mode | Current From DVDD | | | N/A | 0.049 | N/A | mA |
| | Current From VDD12 | | | N/A | 0.6 | N/A | uA |

3.10 Electrical Characteristics for DDR IO

Table 3-10 RK3288 Electrical Characteristics for DDR IO

| Parameters | | Symbol | Test condition | Min | Typ | Max | Units |
|----------------------------|--|--------|-----------------|-----|------|------|-------|
| DDR IO @DDR3 mode | VDDIO_DDR standby current, ODT OFF | | @ 1.5V , 125°C | NA | 0.01 | 2.11 | uA |
| | Input leakage current, SSTL mode, unterminated | | @ 1.5V , 125°C | NA | 0 | 0.53 | uA |
| DDR IO @DDR3L mode | Input leakage current | | @ 1.35V , 125°C | NA | 0.01 | 2.01 | nA |
| | VDD(1.2V) quiescent current | | @ 1.35V , 125°C | NA | 0 | 0.51 | uA |
| DDR IO @LPDDR2/LPDDR3 mode | Input leakage current | | @ 1.2V , 125°C | NA | 0 | 0.49 | nA |
| | VDD(1.2V) quiescent current | | @ 1.2V , 125°C | NA | 0 | 1.89 | uA |

3.11 Electrical Characteristics for eFuse

Table 3-11 RK3288 Electrical Characteristics for eFuse

| | Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|-------------|--------------------------|-----------|----------------|-----|-----|-----|-------|
| Active mode | VDD current in Read mode | Iread_vdd | normal read | 15 | 20 | 30 | mA |

| | Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|--------------|-----------------------------|--------------|----------------|-----|-----|-----|-------|
| | VDD current in PGM mode | Ipgm_vdd | STROBE high | 0.5 | 1 | 2.5 | mA |
| | VQPS current in PGM mode | Ipgm_vqps | STROBE high | 5 | 10 | 15 | mA |
| standby mode | VDD current in standby mode | Istandby_vdd | Standby | 0.2 | 0.5 | 2 | mA |

3.12 Electrical Characteristics for HDMI

Table 3-12 RK3288 Electrical Characteristics for HDMI

| Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|--------------------------------------|----------|------------------|------|-----|-------|-------|
| Differential output signal rise time | tR | 20~80% RL=50Ω | 75 | NA | 0.4UI | ps |
| | tR_DATA | 20~80% RL=50Ω | 42.5 | NA | NA | ps |
| | tR_CLOCK | 20~80% RL=50Ω | 75 | NA | NA | ps |
| Differential output signal fall time | tF | 20~80% RL=50Ω | 75 | NA | NA | ps |
| | tF_DATA | 20~80% RL=50Ω | 42.5 | NA | NA | ps |
| | tF_CLOCK | 20~80% RL=50Ω | 75 | NA | NA | ps |

3.13 Electrical Characteristics for MIPI PHY

Table 3-13 RK3288 Electrical Characteristics for MIPI PHY

| Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|---|------------|-----------------------|-----|-----|-----|-------|
| HS Transmitter AC specifications | | | | | | |
| Common-mode variations above 450 MHz | ΔVCMTX(HF) | 80Ω≤RL≤125Ω | NA | NA | 15 | mVrms |
| Common-mode variations between 50MHz – 450MHz | ΔVCMTX(LF) | 80Ω≤RL≤125Ω | NA | NA | 25 | mVp |
| Differential output signal rise time | tr | 20% to 80%, RL=50Ω | 100 | NA | NA | ps |
| Differential output signal fall time | tf | 20% to 80%, RL=50Ω | 100 | NA | NA | ps |
| LS Transmitter AC specifications | | | | | | |
| Single ended output rise/fall time | trlp, tflp | 15% to 85%, CL < 70pF | NA | NA | 25 | ns |
| | treop | 30% to 85%, CL < 70pF | NA | NA | 35 | ns |
| Signal slew rate | | 15% to 85%, CL < 70pF | NA | NA | 150 | mV/ns |
| Load capacitance | CL | | 0 | NA | 70 | pF |
| HS Receiver AC specifications | | | | | | |
| Common mode interference beyone 450MHz | ΔVCMRX(HF) | | NA | NA | 200 | mVpp |
| Common mode interference between 50MHz and 450MHz | ΔVCMRX(LF) | | -50 | NA | 50 | mVpp |
| Common-mode termination amplitude | CCM | | NA | NA | 60 | pF |
| LP Receiver AC Specifications | | | | | | |
| Input pulse rejection | eSPIKE | | NA | NA | 300 | V.ps |
| Minimum pulse response | TMIN | | 20 | NA | NA | ns |
| Pk-to-Pk interference voltage | VINT | | NA | NA | 400 | mVpp |
| interference frequency | fINT | | 450 | NA | NA | MHz |

3.14 Electrical Characteristics for LVDS

Table 3-14 RK3288 Electrical Characteristics for LVDS

| | Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|-----------|--|-------------------|----------------------------------|-----|-----|-----|--------|
| LVDS mode | Clock signal duty cycle | clock | 1.2GHz | 45 | NA | 30 | % |
| | Vod fall time, 20~80% | t _{fall} | R _{load} =100Ω±1% | 100 | NA | 250 | ps |
| | Vod rise time, 20~80% | t _{rise} | R _{load} =100Ω±1% | 100 | NA | 250 | ps |
| | t _{PHLA} -t _{PLHB} or t _{PHLB} -t _{PLHA} , differential skew | tskew1 | Any differential pair on package | NA | NA | 30 | ps |
| | t _{pdiff} [m]-t _{pdiff} [n] Channel to channel skew | tskew2 | Any two signal on package | NA | NA | 50 | ps |
| TTL mode | Maximum data rate | | CL=10pF, RL=300kΩ | NA | 200 | NA | Mbit/s |
| | TRLP/TFLP | | DOUT at RL=300kΩ to GND | 1 | 1.5 | 2 | ns |
| | Pulse skew | tsk | CL=1-10pF, RL=30kΩ | NA | 10 | NA | ns |
| | Slew rate, transition region | SR | V _{cc} =3.3V, CL=10pF | NA | 27 | NA | V/ns |

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature of RK3288 has to be below 125°C

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on RK3288. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 RK3288 Thermal Resistance Characteristics

| Package (FCBGA636LD) | θ_{JA}(°C/W) | θ_{JB}(°C/W) | θ_{JC}(°C/W) |
|---------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|
| RK3288 | 16.1 | 8.7 | 0.4 |

Note: The testing PCB is base on 4 layers(2S2P), 4 inch x 4.5 inch, 1.6 mm Thickness, Ambient temperature is 25 ° C.