RK3288 Hardware Design Guide

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Foreword

Overview

This document mainly introduces the main points of RK3288 hardware design, aiming to help Rockchip customers shorten the design cycle, improve the design stability and reduce the failure rate. Please refer to the requirements of this guide for hardware design, and use the relevant core templates released by Rockchip as much as possible. If it needs to be changed for special reasons, designs should be confirmed by Rockchip engineers.

Product Version

The product version corresponding to this document is shown below:

Product Name	Product Version
RK3288	

Applicable Object

This document is mainly suitable for the following engineers:

- Single Board Hardware Development Engineers
- Field Application Engineers
- Test Engineers

Revision History

Version	Modified by	Revision Date	Revision Description	Remark
			Initial Release	

Acronym

Acronym includes the abbreviations of phases commonly used in this document.

CABC	Content Adaptive Backlight Control	动态背光控制
DVP	Digital Video Parallel	数字视频并行接口
eDP	Embedded DisplayPort	嵌入式数码音视讯传输接口
ESD	Electro-Static discharge	静电释放
ESR	Equivalent Series Resistance	等效并联电阻
HDMI	High Definition Multimedia Interface	高清晰度多媒体接口
I^2C	Inter-Integrated Circuit	内部整合电路(两线式串行通讯总线)
JTAG	Joint Test Action Group	联合测试行为组织定义的一种国际标准测试协议(IEEE 1149.1兼容)
LCM	LCD Module	LCD显示模组
LVDS	Low-Voltage Differential Signaling	低电压差分信
MIPI	Mobile Industry Processor Interface	移动产业处理器接口
PMIC	Power Management IC	电源管理芯片
PMU	Power Management Unit	电源管理单元
PS/2	Personal System/2	
PCB	Printed Circuit Board	印制电路板
RK	Rockchip Electronics Co.,Ltd.	瑞芯微电子有限公司
SPDIF	Sony/Philips Digital Interface Format	SONY,PHILIPS数字音频接口
TF Card	Micro SD Card(Trans-flash Card)	外置记忆卡
USB	Universal Serial Bus	通用串行总线

Contents

Chapter 1 Brief Introduction

1.1 Overview

RK3288 is a high performance processor, which is suitable for high-end tablets, laptops and smart monitors, and is one of the powerful solutions of 4Kx2K set-top box.
It integrates the quad-core ARM Cortex-A17 CPU including Neon and FPU, and shares with 1MB secondary cache. Dual channel 64 bits DDR3/LPDDR2/LPDDR3 controller provides memory bandwidths required by high performance and high resolution applications. More than 32bit address can support up to 8GB memory space.
Meanwhile, it embedded latest and most powerful GPU(Mali-T764) which can favorably support high-resolution display(3840X2160) and mainstream games. It also supports OpenVG1.1, OpenGL ES1.1/2.0/3.0, OpenCL1.1, RenderScript and DirectX11 etc. It has a great improvement in 3D effect compared to other competing products.
RK3288 also supports all mainstream video format decoding, H.265 video decoding and 4Kx2K video decoding.
Multiple high performance interfaces make display output solution flexible such as dual channel LVDS, dual channel MIPI-DSI, eDP1.1, HDMI2.0 etc. It also supports dual channel MIPI-CSI2 interface which has the capability to deal with 13 million pixels ISP.

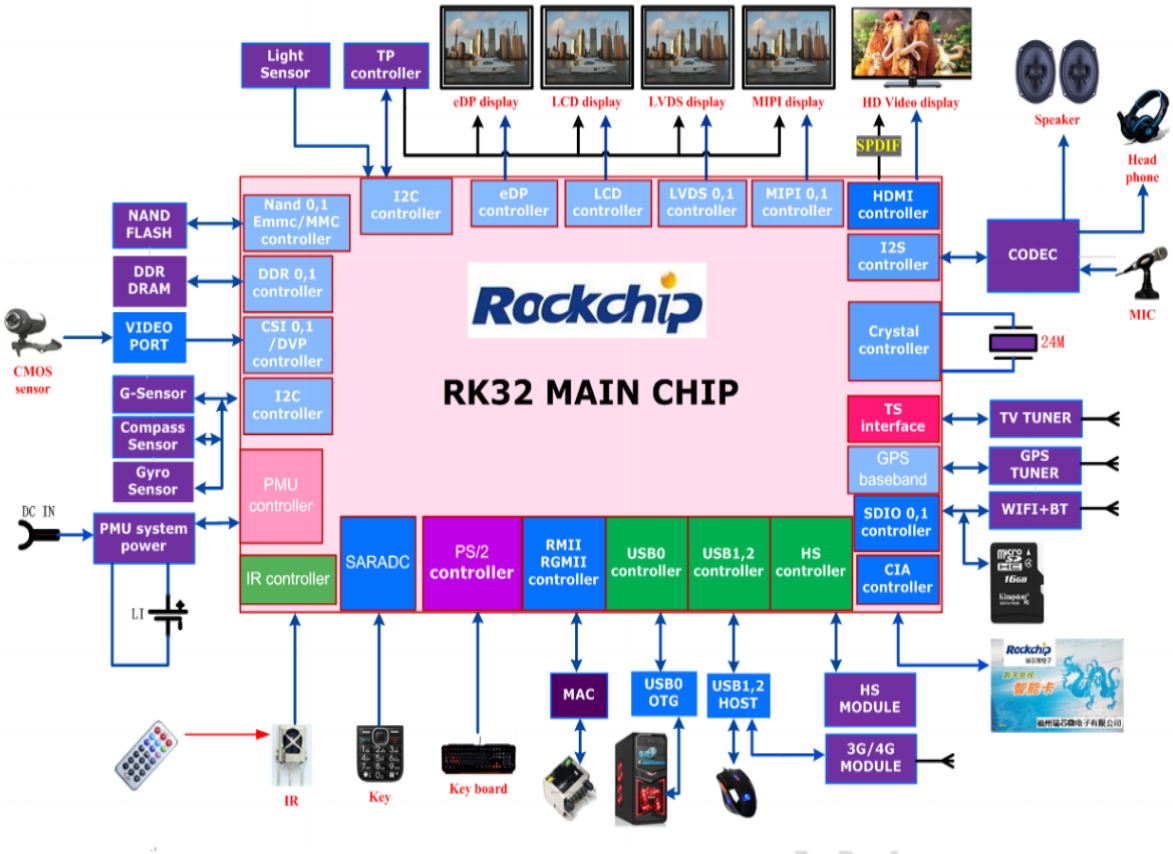


Figure 1-1

1.2 Feature

CPU

- Quad-core Cortex-A17
- Separately Integrated Neon and FPU per CPU
- 32KB/32KB L1 ICache/DCache per CPU
- Unified 1MB L2 Cache

- LPAE (Large Physical Address Extensions), Support up to 8GB address space
- Virtualization Extensions Support
- DVFS support

GPU

- 3D GPU
  - Quad-Core Mali-T7 series, latest powerful graphics processor
  - Architected for GPU computing
  - Support OpenGL ES1.1/2.0/3.0, OpenVG1.1, OpenCL1.1 and Renderscript, Directx11
  - DVFS support
- 2D GPU
  - Multi-Core architecture
  - Up to 8Kx8K input and 4Kx4K output
  - High-quality image scale up/down
  - Dither operation
  - Image rotation with 90/180/270 degree or x/y-mirror
  - BitBLT, Alpha Blending, Raster Operation

VPU

- Video Decoder
  - Support MPEG-2, MPEG-4, AVS, VC-1, VP8, MVC with up to 1080p@60fps
  - Support multi-format video decoder with up to 4Kx2K
  - High-quality deinterleave
- Video Encoder
  - Support multi-format video encoder with up to 1080p@30fps

Video Interface

- Video Input
  - Dual-channel input for front and rear camera
  - Dual-channel MIPI-CSI2 interface with 4-lane per channel
  - 8/10/12 bits standard DVP interface
  - Maximum 5Mpixel for front camera
  - Maximum 13Mpixel for rear camera with high-performance ISP
- Video display
  - Dual-panel display with 2 separately interface
  - Maximum resolution is 4Kx2K
  - CABC support to decrease interface power
  - Dual channel 8/10bits LVDS
  - Dual channel MIPI-DSI
  - HDMI2.0 to support maximum 4Kx2K display
  - Optional eDP1.1 interface

Memory Interface

- Nand Flash Interface

- Dual-channel, 8bits per channel
- Compatible with all of SLC/MLC/TLC Nand Flash, including DDR Nand
- Embedded 60bits hardware ECC
- 8 chip selects to support more device

➢ eMMC Interface
- Compatible with eMMC4.5 standard
- 8bits data width
- Support DDR-50, SDR-100

➢ DDR interface
- Dual channel 64bits interface
- Support DDR3/DDR3L/LPDDR2/LPDDR3

Rich Connectivity
- Three SD/MMC/SDIO interfaces, compatible with SD3.0, SDIO3.0 and MMC4.5
- One 8-channel I2S/PCM interface, One 8-channel SPDIF interface
- One USB2.0 OTG, Two USB2.0 Host
- One 100M/1000M RMII/RGMII Ethernet interface
- Dual-channel TS stream interface, support descramble and demux
- Smart Card interface
- GPS baseband interface
- PS/2 master interface
- 5 UART, 3 SPI (master or slave), 6 I2C (up to 4Mbps), 5 PWM

Others
- Standalone crypto and decrypto, compatible with AES 128bits/ DES/3DES/SHA-1/
- SHA-256/MD5/160bits PRNG
- Full security solution to support HDCP2.x, secure boot, secure debug and DRM
- Temperature Sensor to support better temperature control inside chip

Chapter 1 Reference

RK3288 integrates different function modules and each function module basically has independent power supply mode, therefore in packaging design of schematic diagram, power pins having independent power supply mode are placed in each function module. In the published reference design document of RK3288, for easy to management, adopting design of packet and page modules and adding many common options to avoid problems of various versions of the schematic diagram and repetitive modification for errors, as shown in Figure 2-1. Customers can modify the schematic diagram to acquire the complete schematic diagram according to the demand of actual product. For the details, please refer to the reference design document of RK3288 which released by Rockchip.

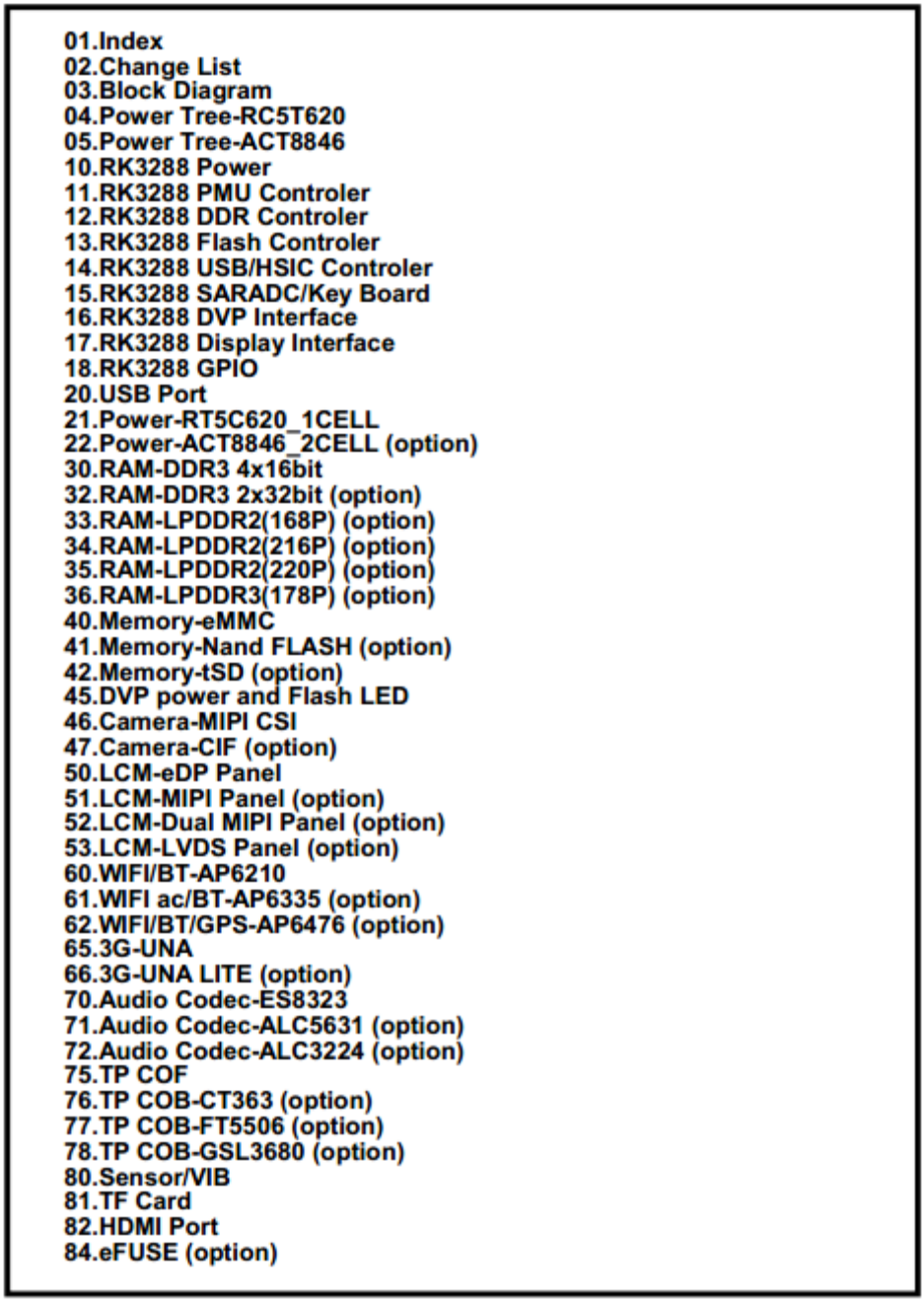


Figure 2-1

For example, customers put forward the following demand table:

RK3288 Product Planning 1	
DC 5V Adapter	No
USB Recharge	Yes
Battery	1-Cell
DRAM	1GB,4 x 16bit DDR3
FLASH	8GB,Emmc
LCM	10.05'' eDP,2560 x 1600
Front Camera	OV2659
Rear Camera	MIPI FX288A R2.0(OV8825)
HDMI	Yes(Type C)
USB OTG 2.0	Micro-B
TF Card	Yes
Audio Codec	Yes
Microphone	Yes
Audio Jack	Yes
Vibration	Yes
G-Sensor	Yes
GyrSOCope	Yes
WIFI Module	802.11 a/b/g/n, BT 4.0
GPS	No
3G	No
4G	No

According to this requirement, deleting the schematic diagram correspondingly, the complete schematic diagram will be acquired, as shown in Figure2-2:

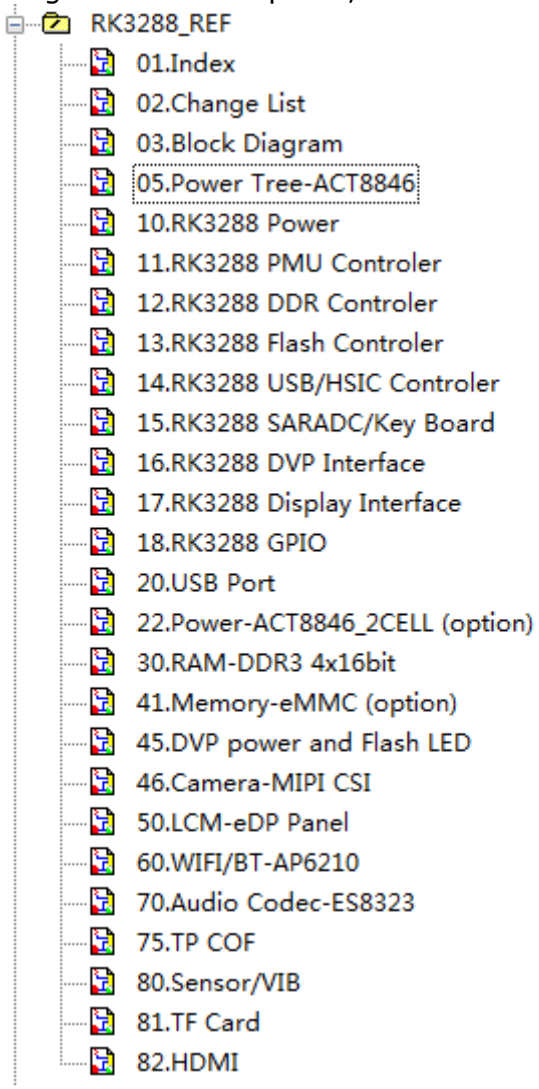


Figure 2-2

Tip: When using 9.7-inch eDP screen, please use double batteries power supply solution to ensure the stability of system and display. Other screens advise to use single battery power supply to reduce cost.

For example, customers put forward the following demand table:

RK3288 Product Planning 2	
DC 5V Adapter	No
USB Recharge	Yes
Battery	1-Cell
DRAM	2 x 32bit LPDDR2(POP Package)
FLASH	8GB,EMMC and NAND FLASH double Layout
LCM	2:8.9'' Dual MIPI,2560 x 1600
Front Camera	No
Rear Camera	MIPI FX288A R2.0(OV8825)
HDMI	No
USB OTG 2.0	Micro-B
Touch	COB,CT363
TF Card	Yes
Audio Codec	Yes
Microphone	Yes
Audio Jack	Yes
Vibration	Yes
G-Sensor	Yes
Gyroscope	Yes
WIFI Module	802.11 a/b/g/n, BT 4.0
GPS	Yes
3G	Yes
4G	No
Efuse	Yes

According to this requirement, deleting the schematic diagram correspondingly, the complete schematic diagram will be acquired, as shown in Figure2-3:

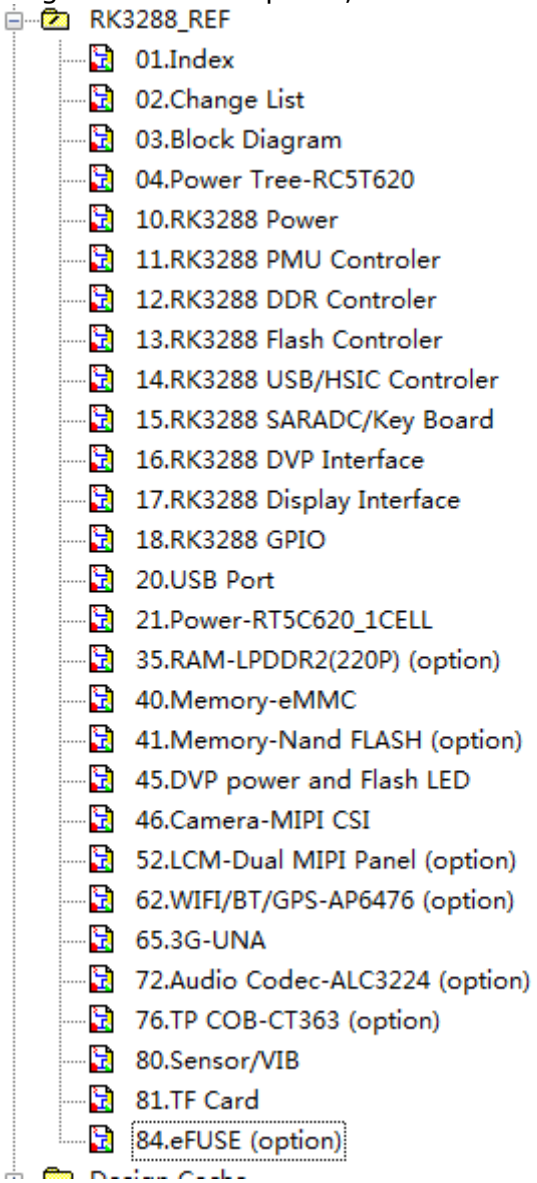


Figure 2-3

Chapter 3 PCB Design

3.1 Structure

To ensure performance and stability of the product, the design of PCB should be highlighted. It is recommended to use 6 layers or 6 layers above PCB Stack in RK3288 to ensure higher performance, and devices are recommended to use double-sided surface-mounted. Copper thickness advise to use 1oz to improve heat dissipation of PCB.

6-Layer PCB Stack (Take 1.2mm thickness of PCB board for example)

Name	Attribute	Specification	Thickness(mil)	Permittivity	Remark
Top	Signal1	Cu	0.7	-	Plating to 1oz
	pp	FR-4	3.8	4.3	-
L2	Gnd1	Cu	1.5	-	1oz
	core	FR-4	8	4.3	-
L3	Signal2	Cu	1.5	-	1oz
	PP	FR 4	-	4.3	Adjust according to the thickness of PCB Board
L4	Power	Cu	1.5	-	1oz
	core	FR-4	8	4.3	-
L5	Gnd2	Cu	1.5	-	1oz
	pp	FR-4	3.8	4.3	-
Bottom	Signal3	Cu	0.7	-	Plating to 1oz

If having GPS, it is recommended to swap Bottom layer with L5, and Bottom layer is GND2 layer. The area of L3 corresponding to DDR area is DDR power supply, DDR traces are in the L5, the area of L4 corresponding to DDR area needs be kept-out, and the traces of L5 only refer Bottom to perform impedance control.

8-Layer PCB Stack (Recommend to use in GPS)

Name	Attribute	Specification	Thickness(mil)	Permittivity	Remark
Top	Signal1	Cu	0.7	-	Plating to 1oz
	pp	FR-4	3.8	4.3	-
L2	Gnd1	Cu	1.5	-	1oz
	pp	FR-4	3.8	4.3	-
L3	Signal2	Cu	1.5	-	1oz
	core	FR-4	8	4.3	-
L4	Gnd2	Cu	1.5	-	1oz
	pp	FR-4	-	4.3	Adjust according to the thickness of PCB Board
L5	Power	Cu	1.5	-	1oz
	core	FR-4	8	4.3	-
L6	Signal3	Cu	1.5	-	1oz
	pp	FR-4	3.8	4.3	-
L7	Signal4	Cu	1.5	-	1oz
	pp	FR-4	3.8	4.3	-
Bottom	Gnd3	Cu	0.7	-	Plating to 1oz

3.2 Design Rule

- In the product planning stage, it is recommended to choose the structure design which the capacitor can be placed under SOC;
- Via size under SOC is 0.22mm/0.35mm (inner/outer diameter);
- In order to suppress the EMI, the traces should follow 3W rule, which keep 3 times the width between traces, shown as Figure 3-1, and trace width and trace distance respectively are 4mil and 8mil;

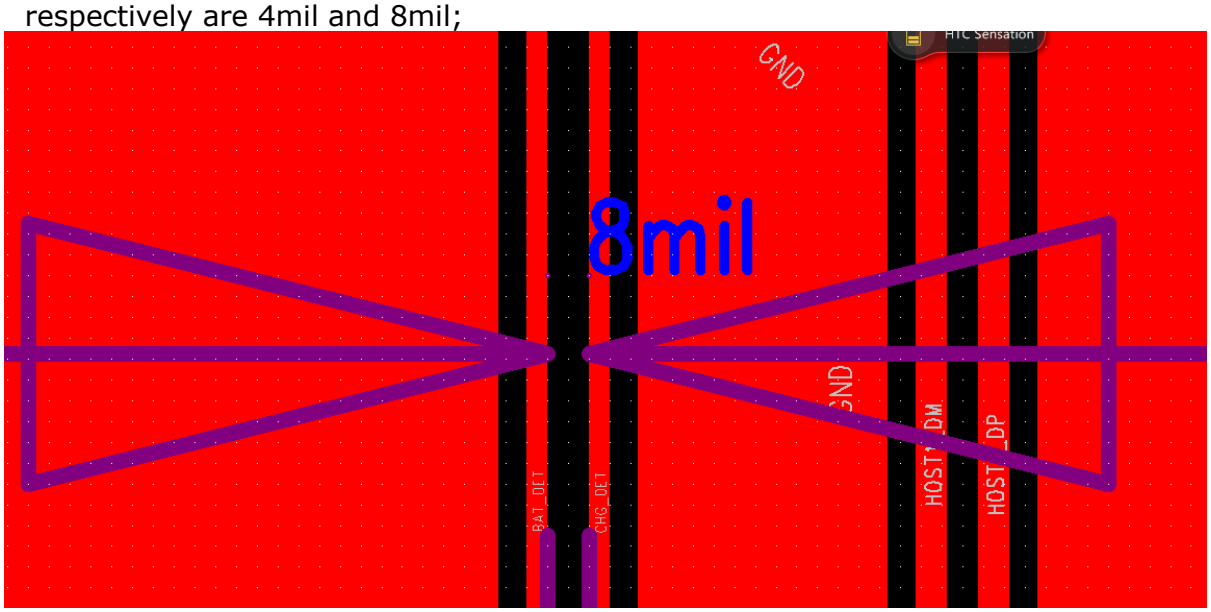


Figure 3-1

- In order to suppress the EMI, power plane should follow 20H rule;
- The shielding need to keep away from the PCB edge about 2mm;
- Top layer and Bottom layer are mainly used to place main devices and signal traces, such as CPU, DDR3 etc.;
- Bottom layer or Top layer are mainly used to place small devices like filter capacitor; if the structure permits, the big devices can be also placed;
- Shielding:
  - PCB needs add a place for shielding shells on the TOP layer to lower EMI and promote the reliability of product, and can use shielding shells as the heat sink of SOC to improve the heat dissipation;
  - If space allows, it is recommended to reserve a place for shielding shells on the Bottom layer of PCB; or to reserve a large area of bare copper on the GND net and to match structure to achieve the shielding effect.

- Copper Integrity: To ensure the copper integrity and continuity can supply good return current, boost the quality of signal transmission, enhance the stability of product, and also improve the performance of heat dissipation of copper. Achieving the following points can ensure the copper integrity and continuity, as shown below, to stabilize the product performance.

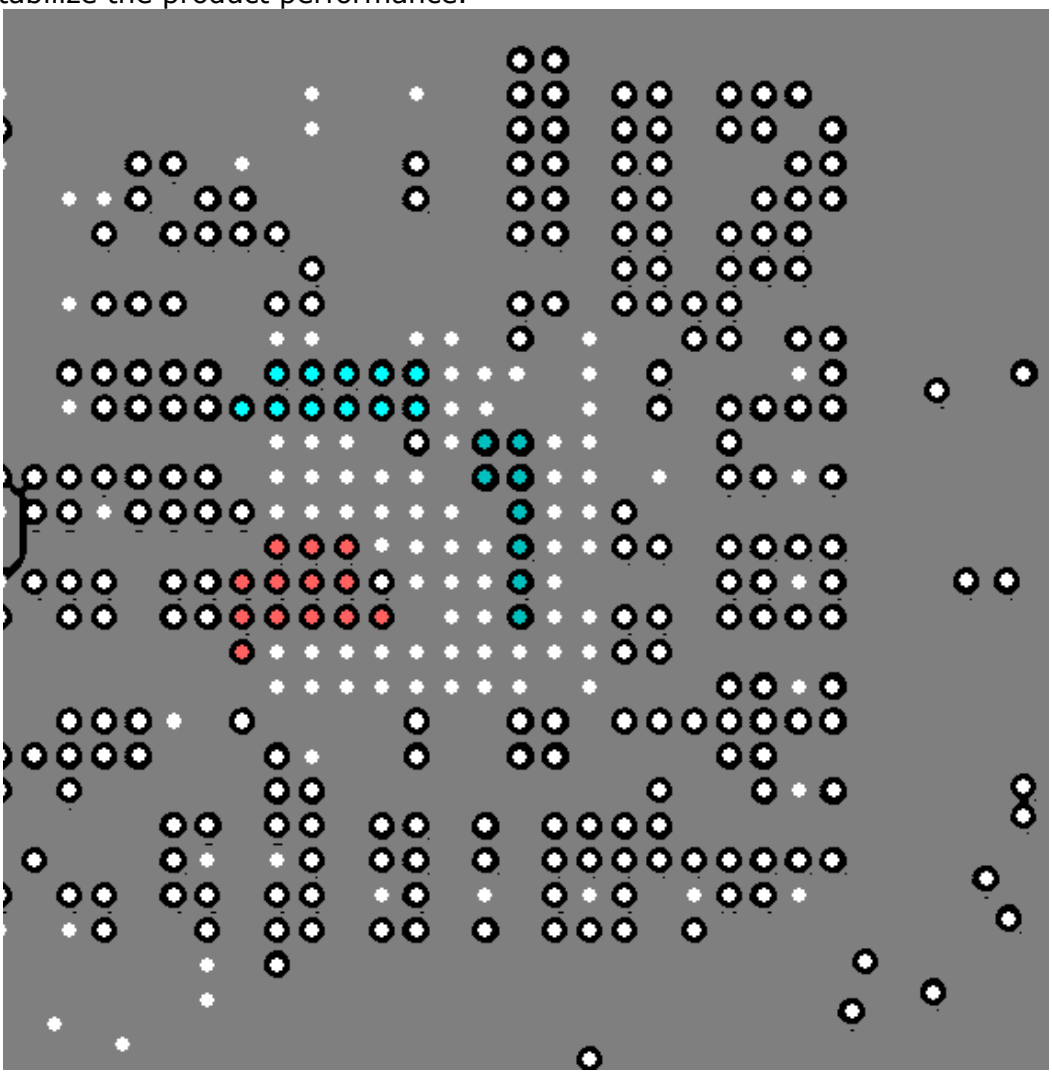


Figure 3-2

- Setting copper layer as split/mixed plane;
- Setting 5.5miles clearance between vias and copper;

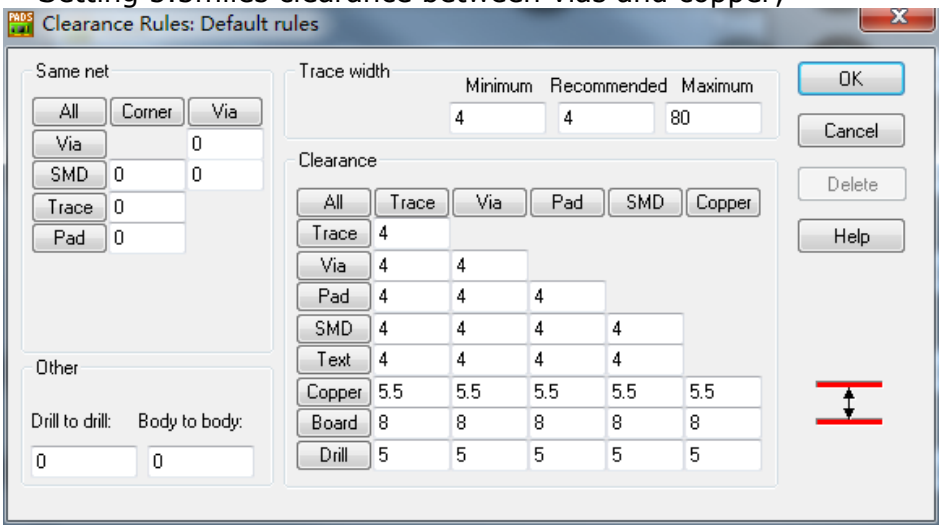


Figure 3-3

- Setting the width of copper as 4mils;
- CPU pin signal fan out and punch vias, then the vias should be regularly arranged and reasonably distributed, shown as Figure 3-4.

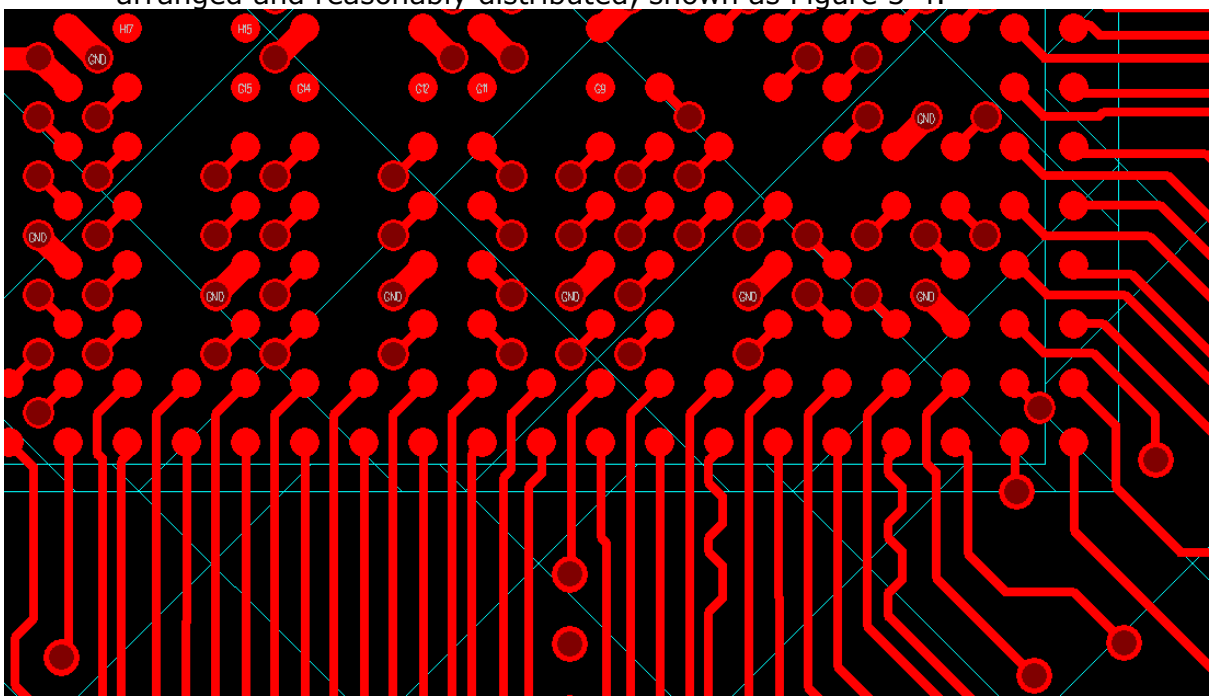


Figure 3-4

Tips:

- **3W rule: To reduce the crosstalk between traces, the clearance should be as wide as possible; if the center-center distance of traces is not less than 3 times the width of traces, 70 percent of the electric field between traces can maintain without interference;**
- **20H rule: retracting the power plane which makes the electric field transmit only within the range of stratum. Taking one H as unit, if retracting 20H can restrain 70 percent of the electric field in the grounding edge, then retracting 100H can restrain 98 percent of the electric field in the grounding edge.**

3.3 Test Point

- eMMC, Nand Flash need add the test point in the signal of EMMC_CLKO, FLASH_CLE that is convenient to enter maskrom mode when debugging;

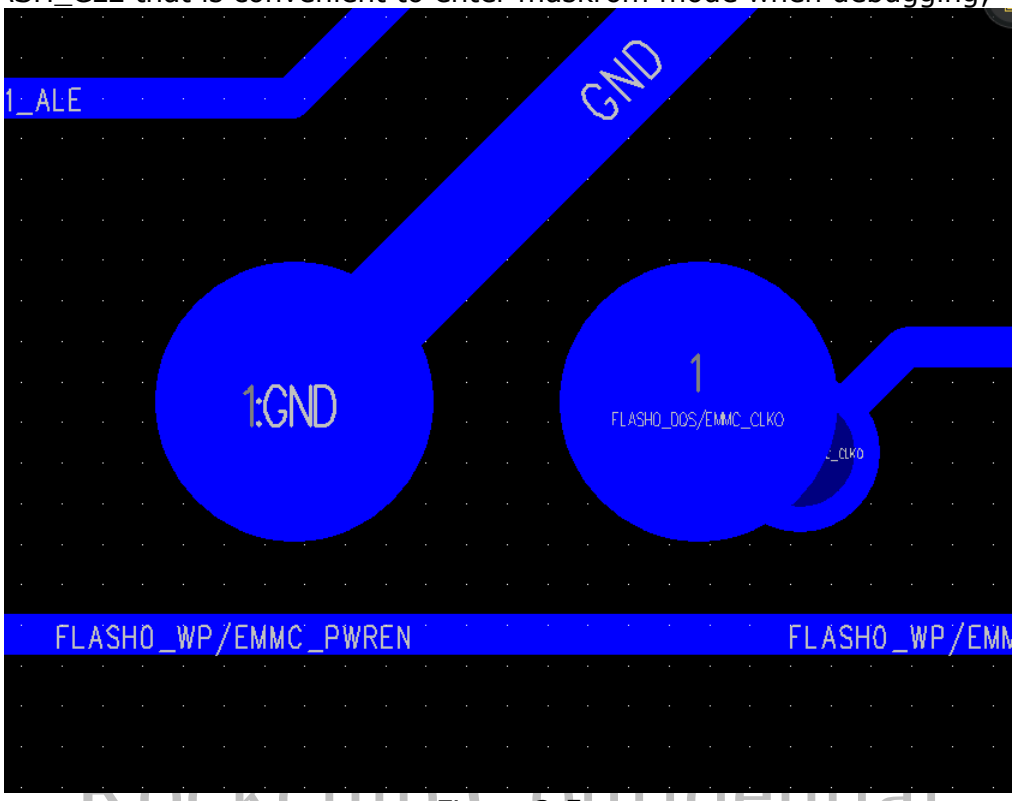


Figure 3-5

- Interfaces like webcam, TP, LCM, are recommended to increase the signal test points so as to facilitate the factory testing;

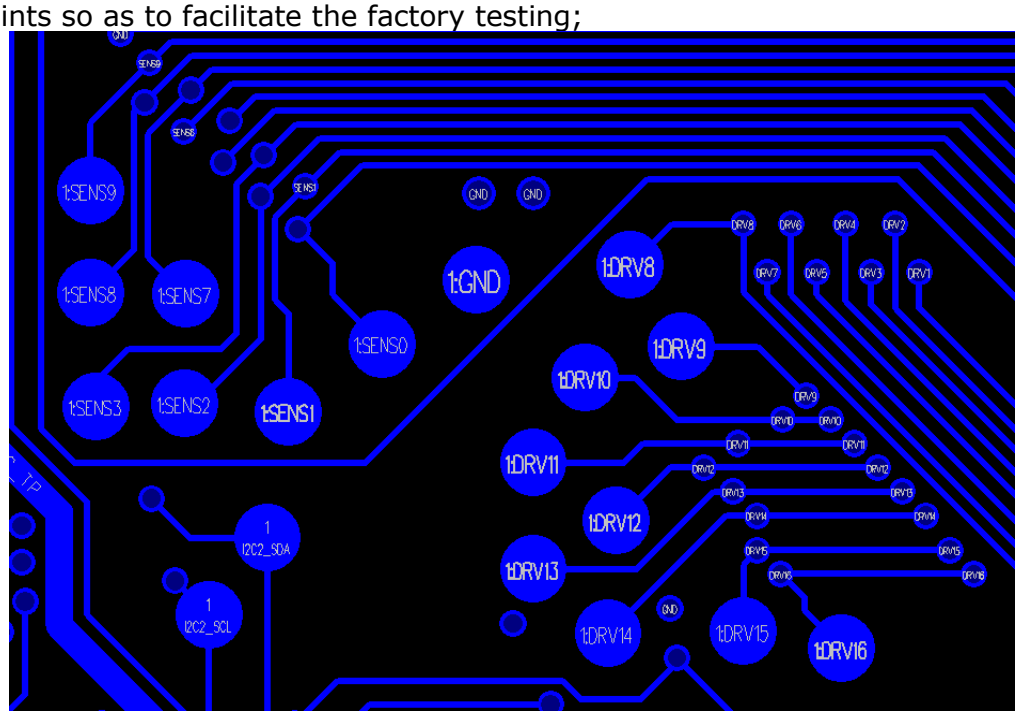


Figure 3-6

3.4 Silk-screen and Decal

- Add PCB name, Layout time and date to facilitate query and debugging
- Add part reference in PCB board to facilitate debugging;
- Add silk-screen description on key signals, such as the pin of battery pad, the sequence of pin of connector etc.;
- The first pin on the chip needs to be marked clearly, and the tag cannot be overlapped or hidden under the device body;
- Confirm whether the package size is correct and the height is in the limit;
- Confirm whether the welding direction of interfaces like headphone socket and USB (especially the sinking-mode) is the mirror image;
- The back of BGA cannot be placed big components when using double-sided surface-mounted. If using slot-type single side surface-mounted, please make sure the devices is in the range of slots.

Chapter 4 Thermal Dissipation

On RK3288, CPU is the device which generates the largest amount of heat, all the heat dissipation methods are mainly for RK3288.
In addition to RK3288, other major heat sources are: PMIC, charging IC, backlight IC and inductance. The high-current power traces (such as DC 5V to charging IC traces, the battery to VCC_SYS of PMU traces) also affect the chip heat; Please note that these heat sources cannot be put together in Layout, but should be placed dispersedly. Try to keep the power traces of high current as short and wide as possible.
According to the radiation diffusion characteristics of the heat, when CPU uses the heat sink, it had better center on the heat source and use square or circular heat sink, and not to use the long strip-shaped heat sink. The heat dissipation effect of heat sink is equal to its size, according to Figure 4-3, the size of graphite heat sink having the economic efficiency is about 6cm*6cm, shown as Figure 4-1.

Figure 4-1

- The following three ways to enhance heat dissipation in PCB heat conduction:
  - Punch vias on bottom of PAD of PCB heating devices;
  - Pour the continuous copper on the PCB surface;
  - Increase the copper content of PCB (the thickness of copper is 1oz);
- Mounting the heat spreader on the top of the CPU and below PCB which is corresponding to the area of CPU, and dissipating the heat of CPU to the back cover and the LCD screen or the middle frame, which can greatly reduce the temperature of the CPU itself. However, the way to dissipate the heat of CPU to the LCD screen should be considered in compromise. As for a high-power screen like 9.7-inch eDP, try to prevent the heat spreader on the bottom of the CPU to touch the screen, which will cause part of the screen overheat in the long run and form the image color block.
- As for the machine with metal back cover, it is best to conduct the heat of the CPU to the back cover by thermal silica.

- As for the machine which its rear end is the plastic (RF antennae) and its middle is the mental, please note that the main heat sources must be placed below the mental part of the back cover in Layout.
- The machine having the plastic back cover should be mounted respectively one piece of graphite heat sink on PCBA and the back cover to achieve a better cooling effect.
- The current selections of heat dissipation material are various, and it is recommended to compare different materials to find suitable heat dissipation method.

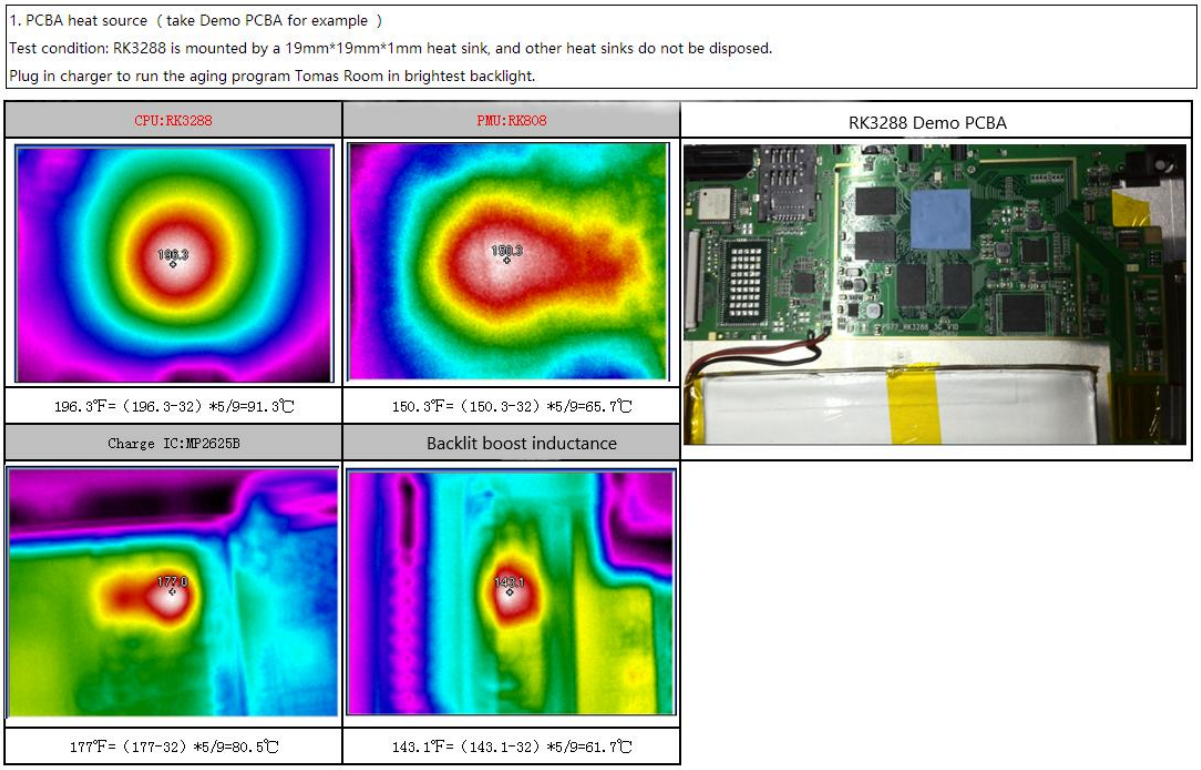


Figure 4-2

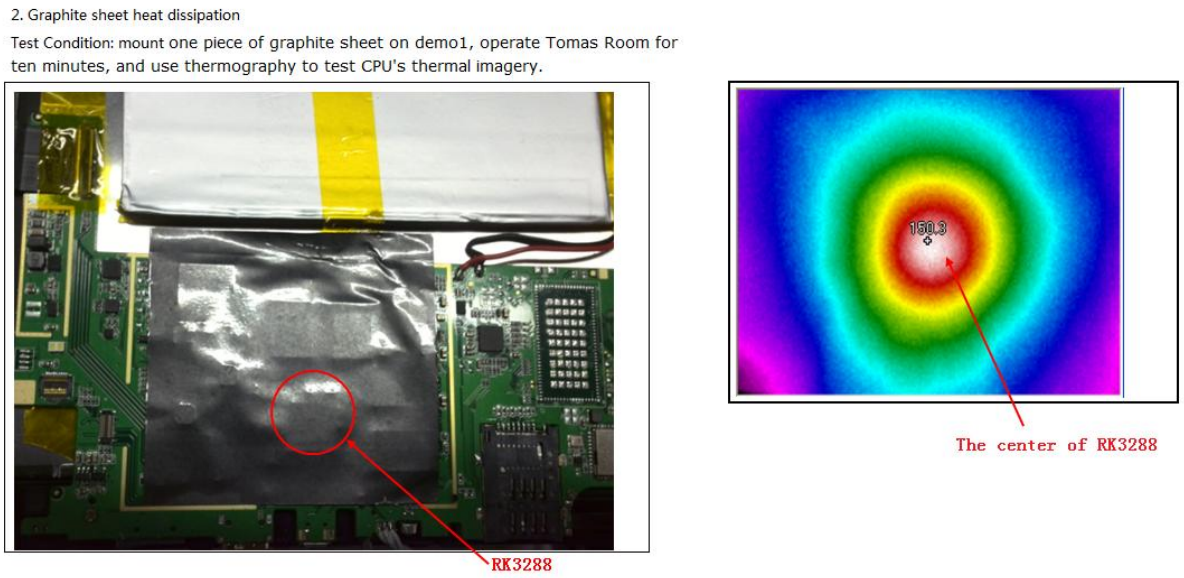


Figure 4-3

3. Imaging picture that Single-layer graphite sheet on PCBA
Test Condition: Mount one piece of graphite sheet on demo1 and demo2, the rear cover does not be disposed. The following is the imaging picture of the cover after operating Tomas Room for 10 mins.

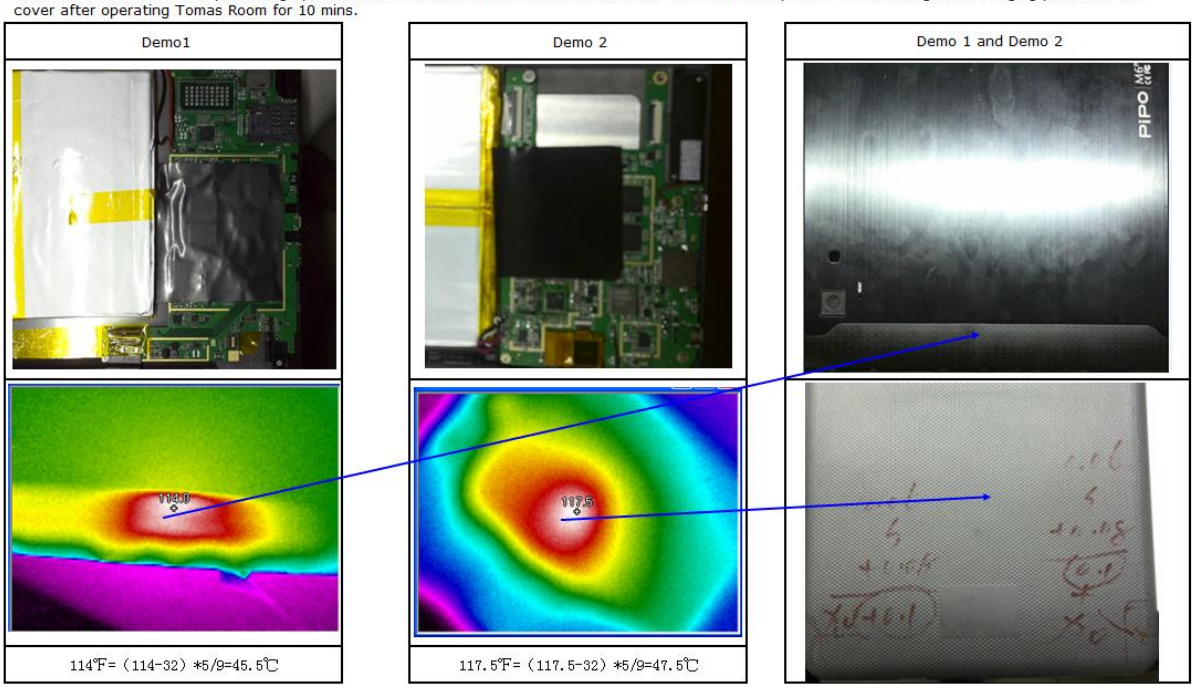


Figure 4-4

4. Imaging picture that PCBA is mounted by a thin graphite sheet, and the rear cover is mounted by a thick graphite sheet
Test condition: PCBAs of domo1 and demo2 are respectively mounted by a graphite sheet, and the rear cover corresponding to the center of CPU is mounted by a thick graphite sheet .The following is the imaging picture of the cover after operating Tomas Room for 10mins

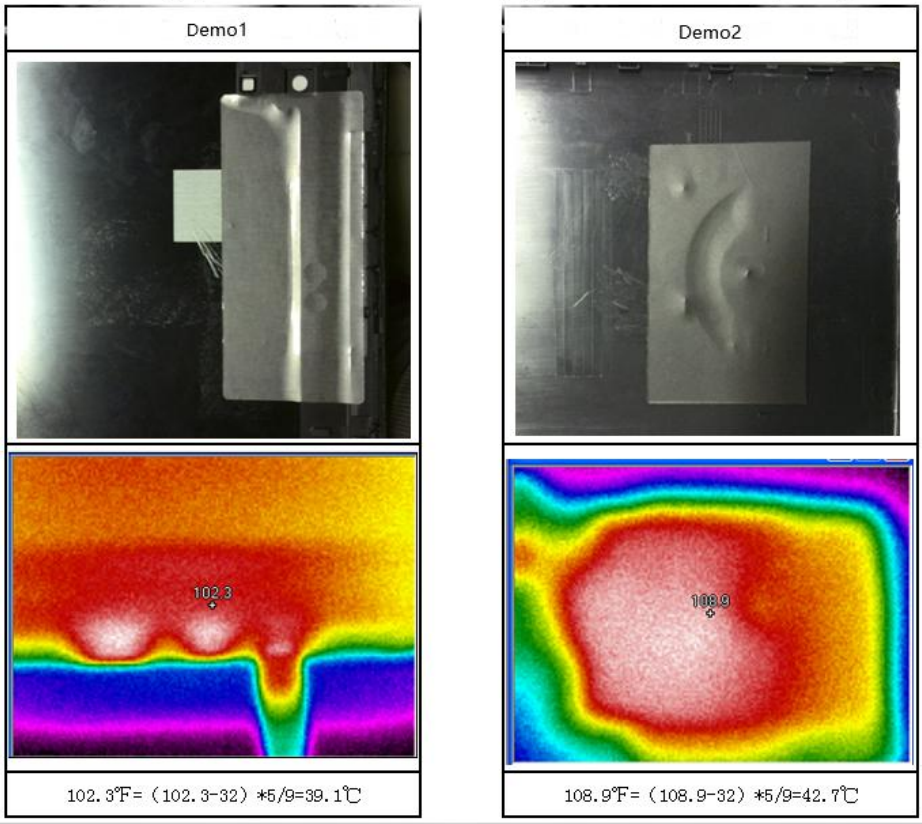


Figure 4-5

Chapter 5 Power

5.1 Schematic

- VDD_CPU and VDD_GPU are power supply for SOC, and the peak current can up to 4.4A/3.6A(CPU@1.6GHz,GPU@400MHz), therefore please do not delete the capacitors in the reference design (VDD_CPU need 154uF capacitors, VDD_GPU need 66uF capacitors), the large capacitor should be placed close to the back of SOC to ensure the power ripple to be controlled within 100mV, shown as Figure 5-1.

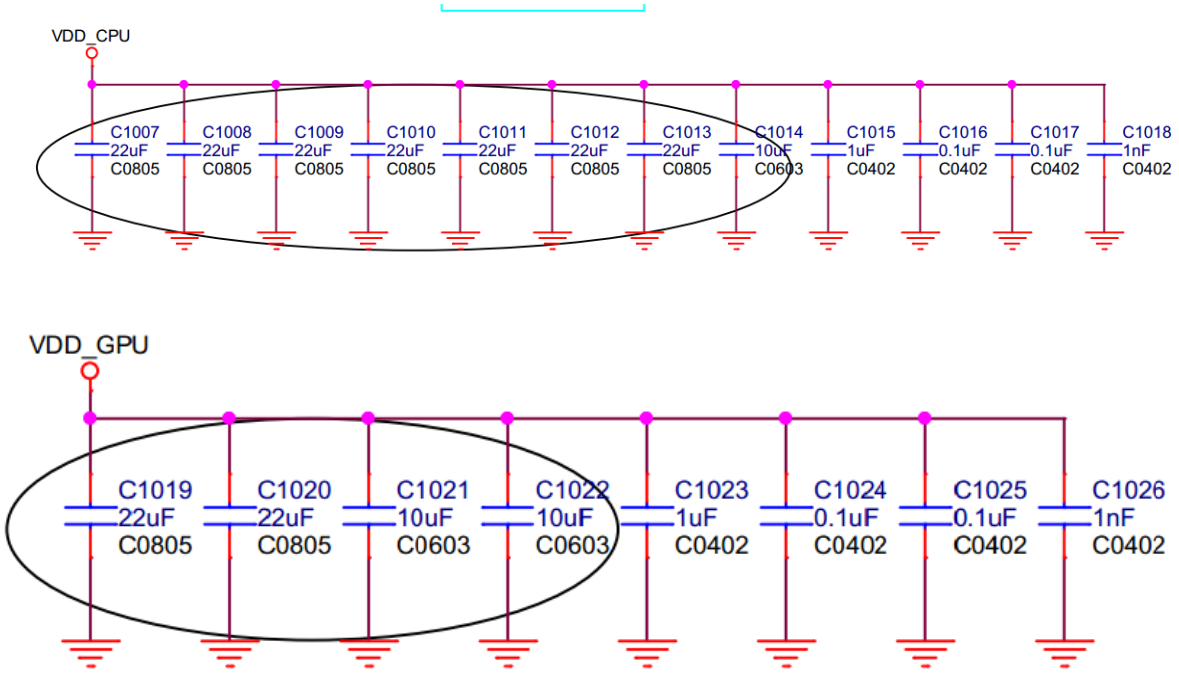


Figure 5-1

- CPU_VDD_COM and GPU_VDD_COM (Figure 5-2) are the power supply feedback pins for CPU and GPU of SOC. They should be connected to FB ports of power output DC/DC, which can compensate the loss of impedance from PCB power traces, and improve the real-time of dynamic adjustment of power supply.

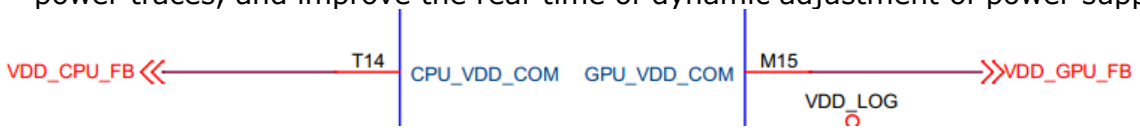
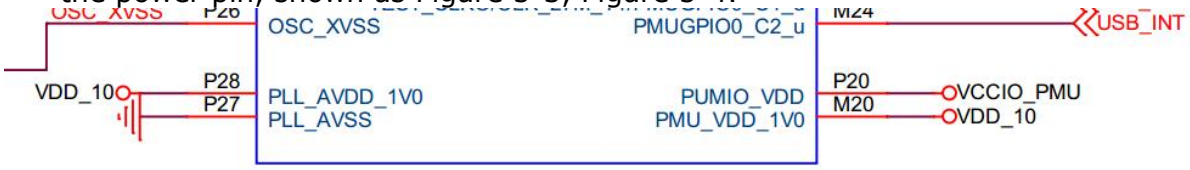
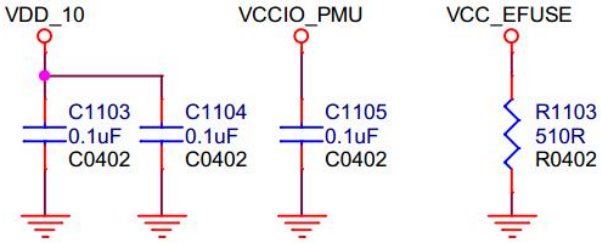


Figure 5-2

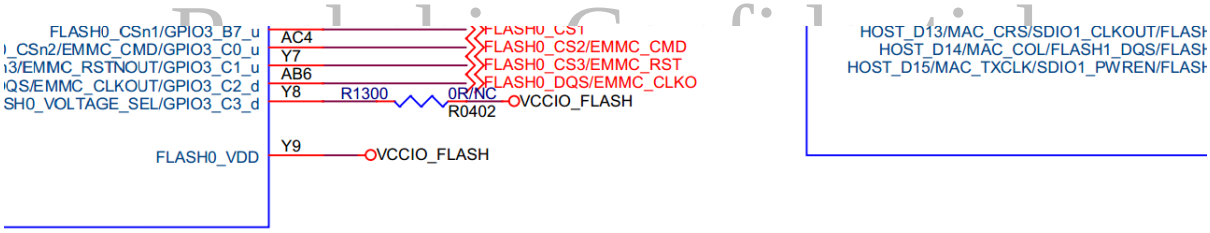
- 100uF coupling capacitors in the schematic design should be placed close to the power pin, shown as Figure 5-3, Figure 5-4.

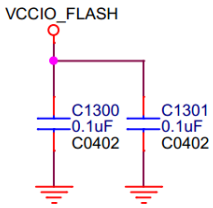




Note: All the capacitor should be place close to the power pin of RK3288。

Figure 5-3





Note: All the capacitor should be place close to the power pin of RK3288。

Figure 5-4

5.2 PCB Layout

The design of power supply is crucial and influences directly the performance and stability of product, please design according to the requirements of Layout released by Rockchip.

To ensure large-area power copper from power output to power pins corresponding to SOC can improve the load-current capacity and reduce the trace impedance, shown as Figure 5-5.

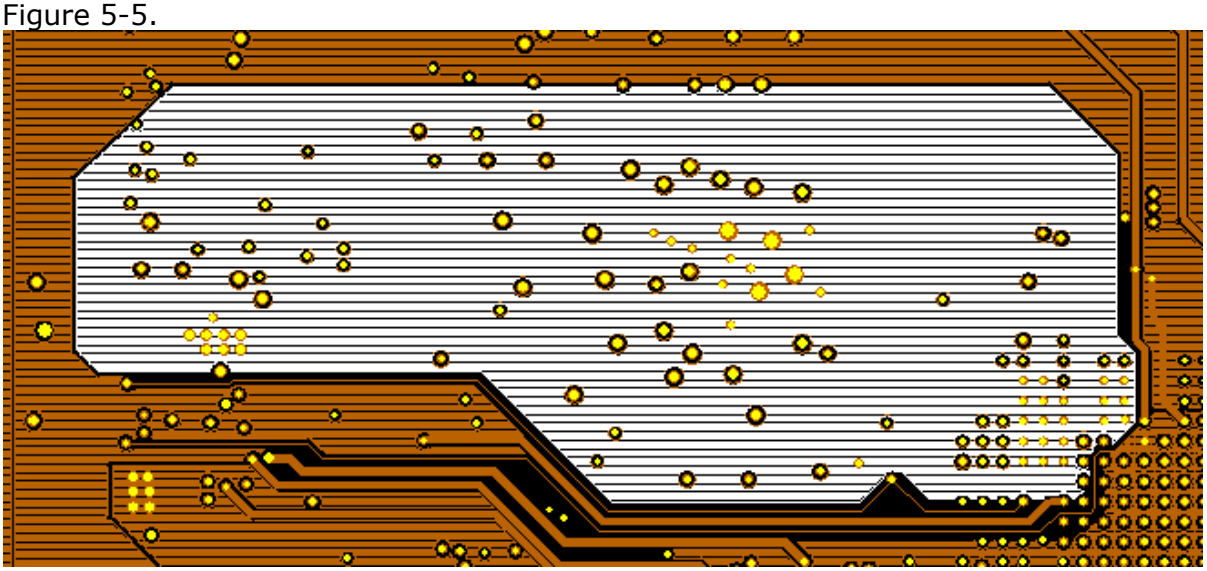


Figure 5-5

The connections of the power swap layer need more vias to improve the load-current capacity and reduce the trace impedance (the specific number can be calculated referring to the tips), shown as Figure 5-6.

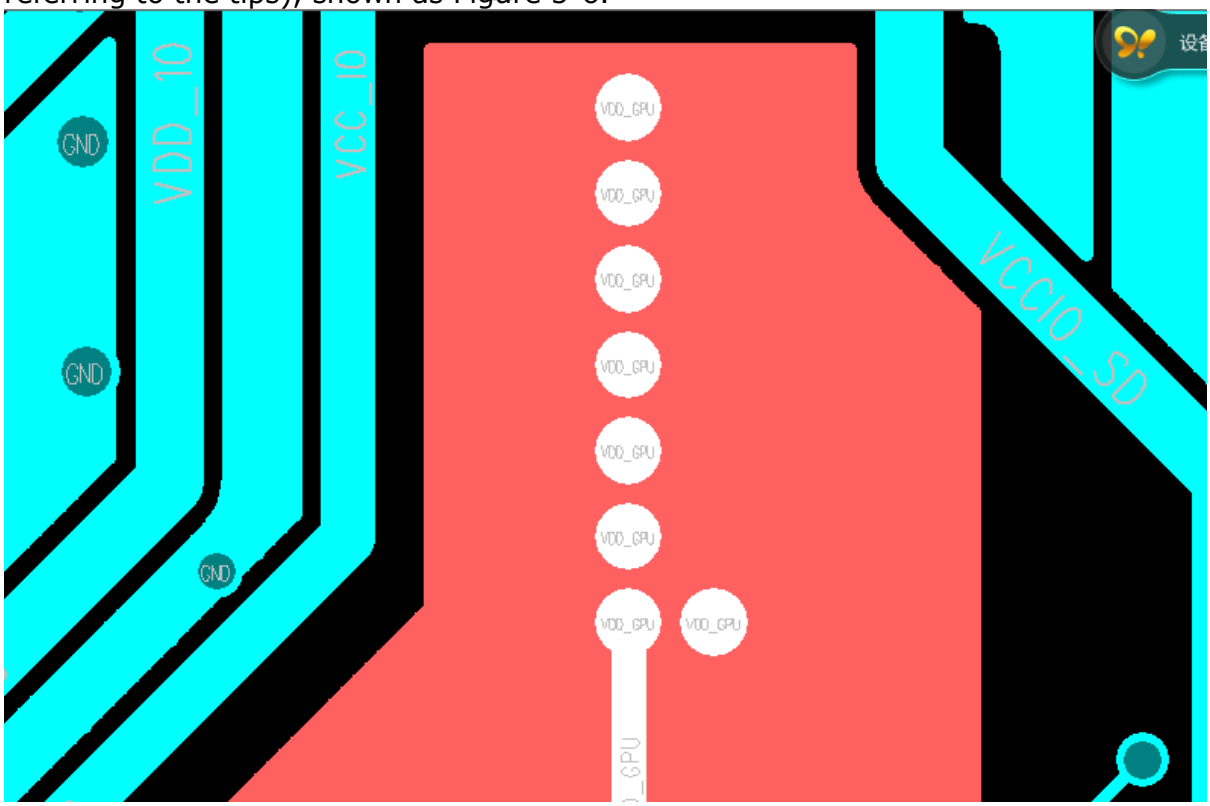


Figure 5-6

The feedback compensation design of CPU_VDD_COM and GPU_VDD_COM can make up for the voltage loss of traces and improve the dynamic adjustment of power supply, shown as Figure 5-7. The traces lighted in the figure is the VDD_GPU feedback compensation trace, on the other side of this trace connects to the FB port of power output DC/DC. The traces need parallel layout with power layer and cannot be disturbed by data lines.

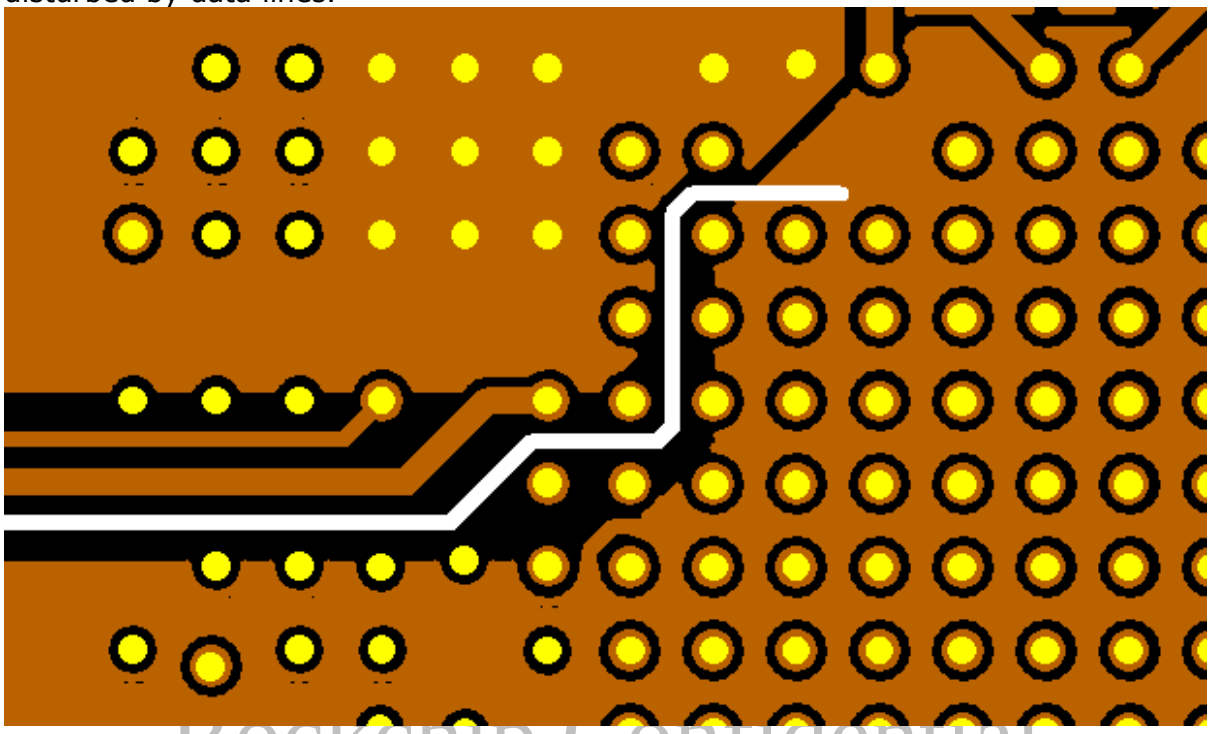


Figure 5-7

The power load ends of VDD_CPU, VDD_GPU, VDD_LOG and VCC_DDR should be placed the large capacitors. If conditions permit, the back of SOC of VDD_CPU and VDD_GPU is placed respectively above 40uF large capacitors, VDD_LOG and VCC_DDR also need to be placed more than 10uF capacitors to improve the quality of power supply and enhance product performance to ensure the stability of products, shown as Figure 5-8.

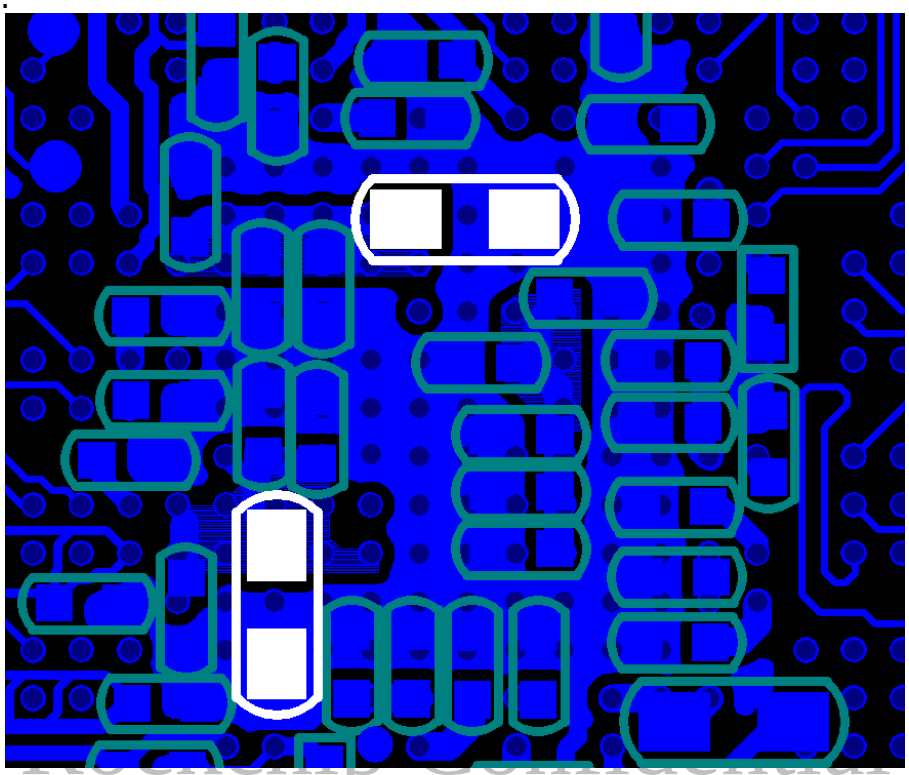


Figure 5-8

GND vias under the SOC should be punched sufficiently, homogeneously and be cross-linked to improve the quality of power supply, heat dispersion and system stability. The dimension of vias in the bottom of SOC are 0.2mm/0.35mm (inner/outer diameter), shown as Figure 5-9.

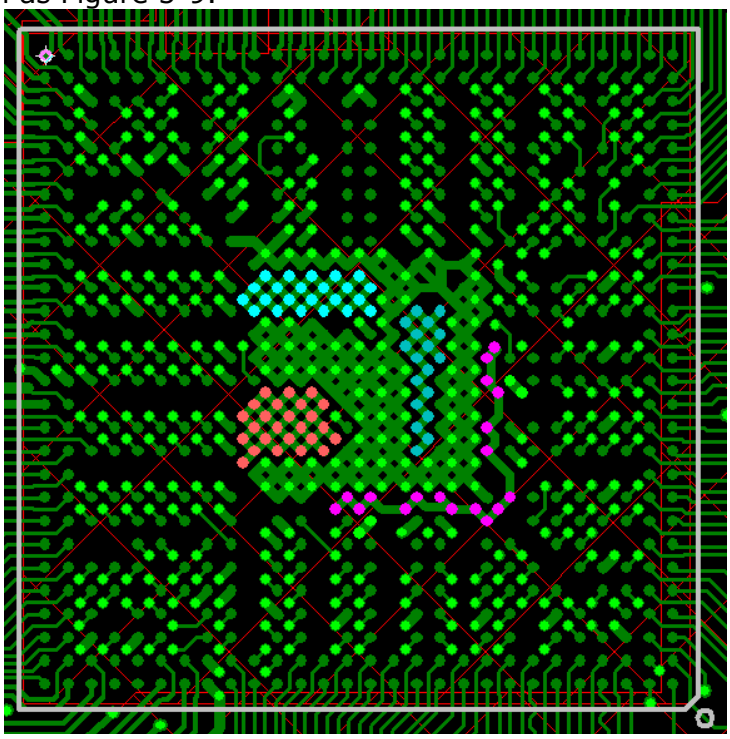


Figure 5-9

Tips:

- **How to set the width of power copper:**

The formula for the maximum allowable current referring to the width of PCB:

$$I = KT^{0.44} A^{0.75}$$

K in the formula is the correction coefficient, and the value of the copper in the outer layer usually is 0.045, while the value of the copper in the inner layer is 0.024; T is the maximum allowable temperature in °C (Celsius); A is the sectional area of copper in sq.mil (not sq.mm); I is the maximum allowable current in A (Ampere).

Taking VDD_CPU power supply of RK3288 as an example, and the peak current is up to 5A. The power supply is assumed in the inner layer, the thickness is 0.8mil (0.5oZ), and the maximum allowable temperature rise is 10°C, then the PCB traces need 312.5mil. If the temperature rise need to be further lower, the width of copper must be wider, thus, if having enough PCB space, it is recommended to use wider copper to lower temperature rise.

- **How to set the vias quantity of the power swap layer:**

Above-mentioned formula can also be used to calculate the magnitude of current in one via. The formula to calculate the width of copper of via is L=πR, R here means the radius of via.

Taking 0.2mm diameter of via as an example, the thickness of copper is 0.8mil(0.5oZ), The maximum allowable temperature rise is 10°C, then one via can pass 420mA current, and to pass 5A current needs at least 13 vias of 0.2mm diameter. When the areas are finite, increasing the diameter of power via can reduce the amount of vias.

5.3 SYR827, SYR828 PCB Layout guide

The definition of SYR827, SYR828 pin is shown as Figure 5-10.

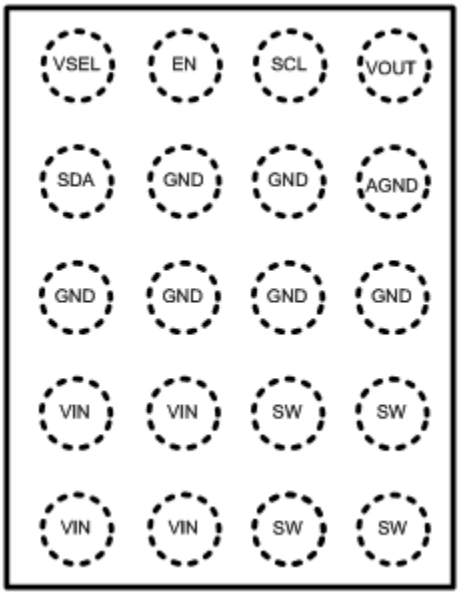


Figure 5-1

Place the input capacitors Cin and the output capacitors Cout among of Vin pin, Vout pin and GND, and reduce the loop areas among Vin pin, Vout pin and GND as more as possible to decrease the amplitude of the power ripple and improve the reliability of the chip, shown as Figure 5-11.

The inner of IC PCB cannot be filled with cooper when mounted, otherwise, IC can be moved easily in SMT, so the trace connection is the only way. The chip should be placed close to GND vias (to ensure the quantity above 10), shown as Figure 5-11.

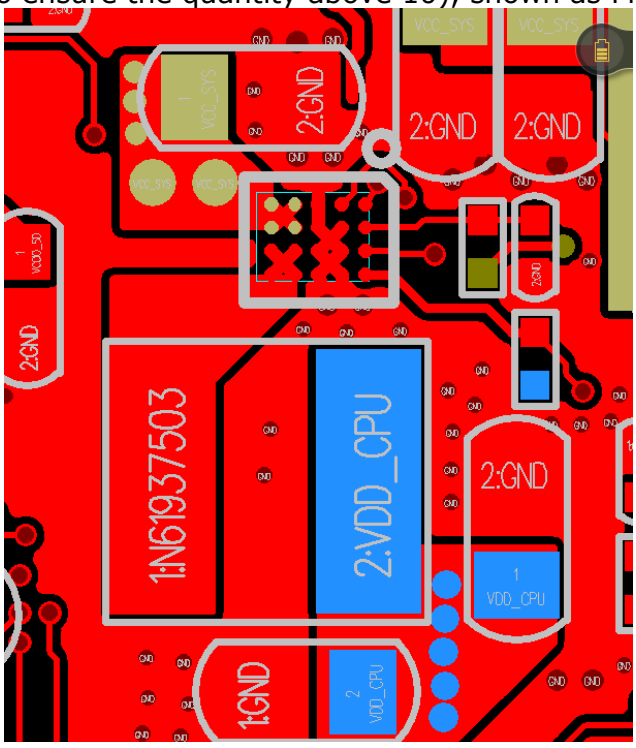


Figure 5-11

The inductance reference value of SYR82X DCDC: the sense quantity is 0.22uH, the saturation current is more than 5A, and the diameter resistance is less than 20mR; To improve the quality of power output, it is recommended to value the range between 0.22uH to 0.24uH (Using 0.22uH inductance, the power output ripple is less about 20mV compared to 0.33uH inductance).

SYR827 and SYR828 correspond respectively to VDD_CPU and VDD_GPU, which have different I2C addresses, same appearance, and the slight different top marking. The factory is easy to mount in the wrong place to cause the machine crash that is very difficult to rework (the success rate of rework is about 50%). Customers should pay more attention to the locations of materials and the wrong welding placements. The appearance identification is shown as Figure 5-12, Figure 5-13.

Figure 5-12(Spec: SYR827. Correspond to VDD_CPU power supply)

Figure 5-13(Spec: SYR828. Correspond to VDD_GPU power supply)

5.4 PMIC RC5T620

It is recommended to use the RC5T620 in the single battery supply that the cost is relative low, but must try to avoid using in the system that the maximum current exceeds 3.5A (Such as the 9.7-inch eDP display solution. In the single battery solution: battery internal resistance is 70mR, coulometer sampling resistor is 20mR, and path management resistance is 60mR. All told are very easy to surpass 150mR, and the large pressure drop loss, 0.525V (150mR*3.5A) on the transmission will reduce the efficiency). Therefore, try to use full electric voltage 4.35V, internal resistance less than 70mR and 90 percent of battery over 3.5V.

To ensure input/output capacitors close to GND as much as possible, shown as Figure 5-14, the earth terminal of input/output capacitors should be punched the corresponding amount of vias to GND according to the supply current, shown as Figure 5-15.

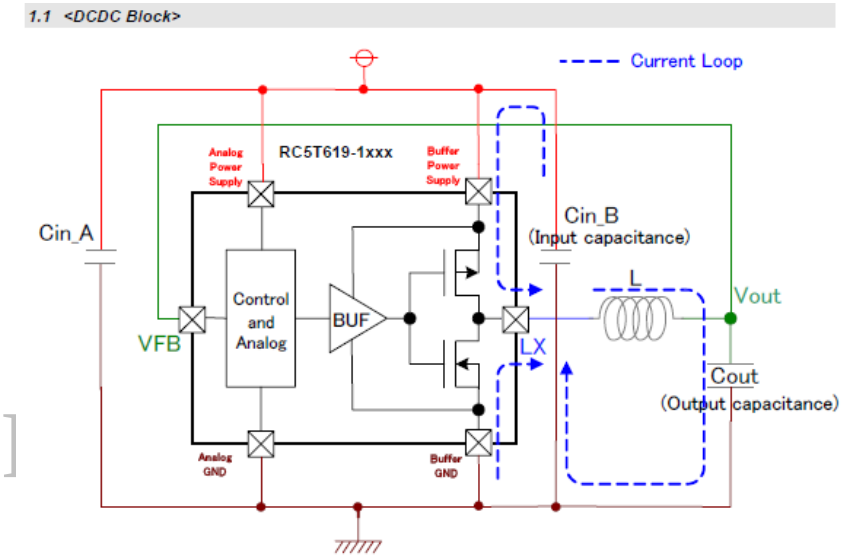


Fig. 1-1: Simplified Schematic for DCDC1, DCDC2, DCDC3, DCDC4 and DCDC5

Figure 5-14

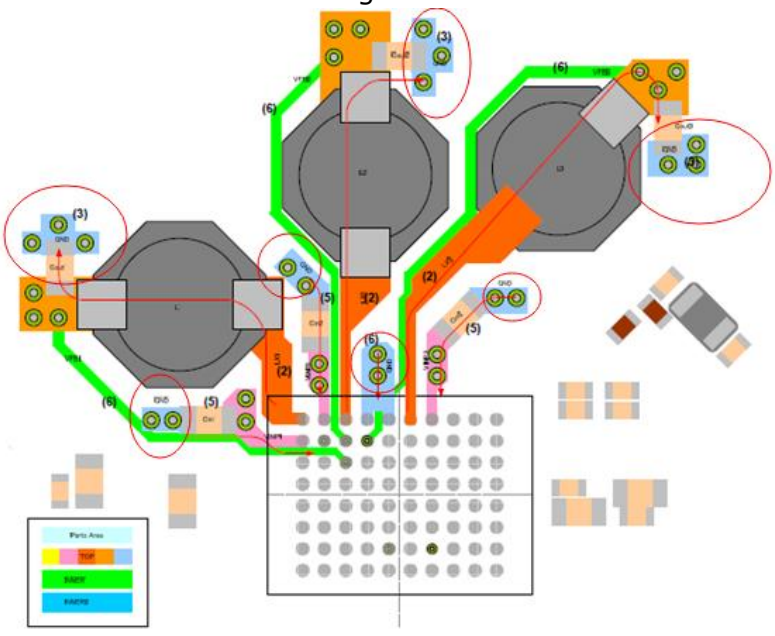


Figure 5-15

There are two sampling resistances in RC5T620: one is charging current sampling current as shown in Figure 5-16. It needs to differential traces to the C4 pad and C5 pads from the both ends of R2166 in PCB Layout, as for the blue line shown in Figure 5-17, please special attention that C5 cannot be short circuit with B5 directly, otherwise, low charging current would appear.

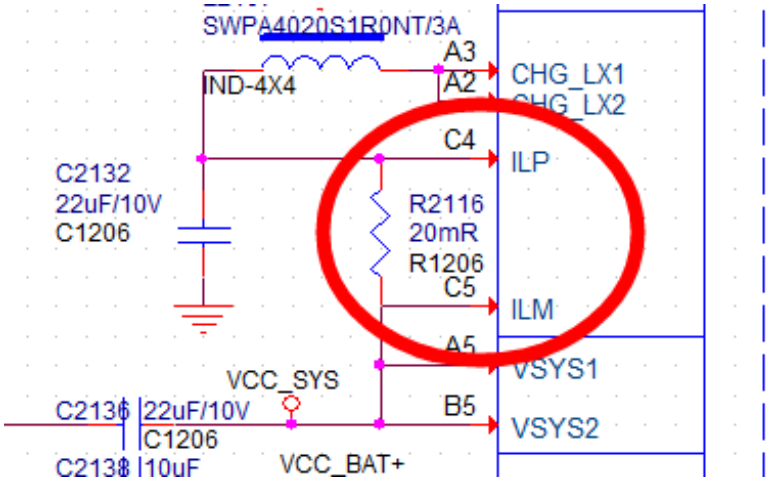


Figure 5-16

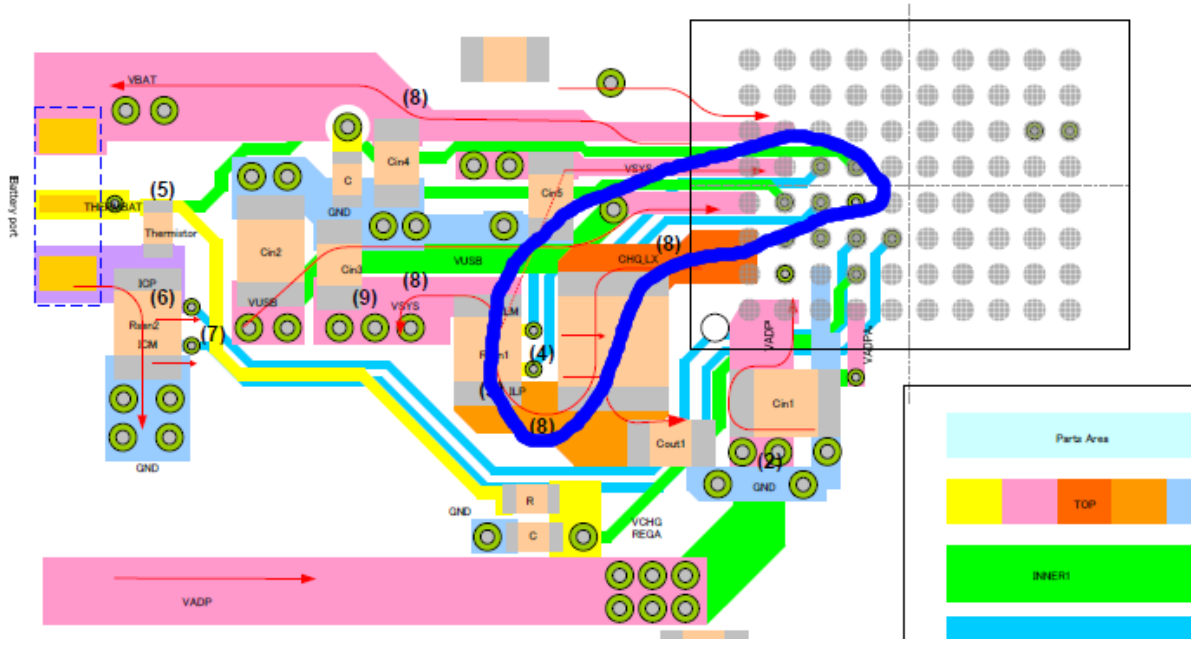


Figure 5-17

Other sampling resistances in battery terminal are shown as Figure 5-18, please place R2120 close to R2119 in Layout, R2120 cannot be connected to GND directly and should separately be traced to R2119 after separating the copper with Keepout, then ICP, ICM traces differentially to E3 and D3 pads, shown as Figure 5-19.

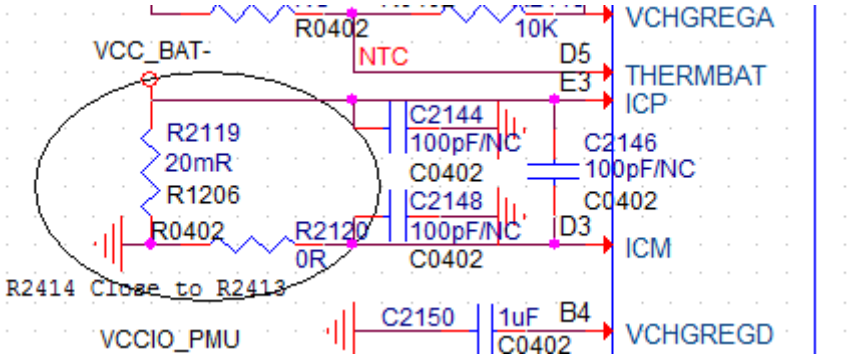


Figure 5-18

R2120 is separately traced to R2119 after separating the copper with Keepout

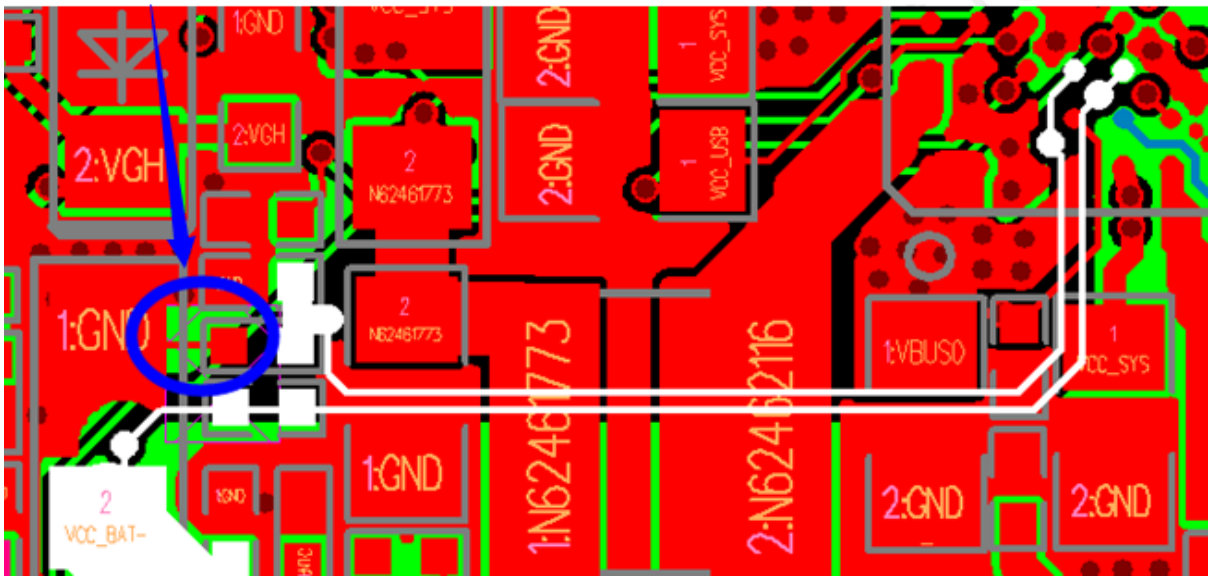


Figure 5-19

32.768KHz should be shielded by GND traces, the second layer refers to the horizon, and try not to be traced with other date lines to avoid disturb the clock, shown as Figure 5-20.

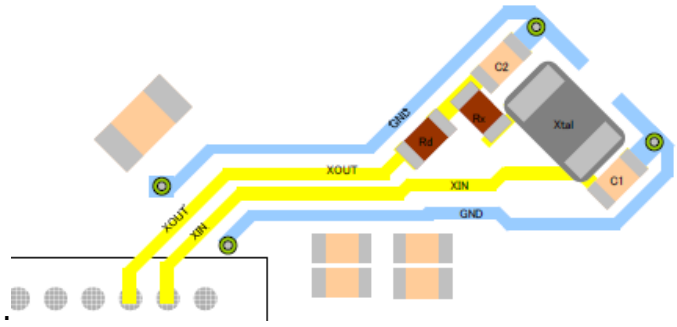


Figure 5-20

RC5T620 has to be short circuit from the USB port to ADP port in the solution of only having USB charging port to reduce the trace loss (The resistance of the internal switch of USB charging port is larger than ADP charging port). (Note: after short circuiting the ADP and USB, ADP will be priority, so the traces from USB port to ADP terminal should be thick.)

5.5 PMIC RK818

RK818 has sampling resistance R2340 in the battery terminal and differential resistance R2342, shown as Figure 5-23. In Layout, please place the second pin of R2342 close to the second pin of R2340, and forbid cooper around R2342, and connect R2340 with single points. Place RK2340 near the battery terminal. SNSP and SNSN order differential traces, shown as Figure 5-24.

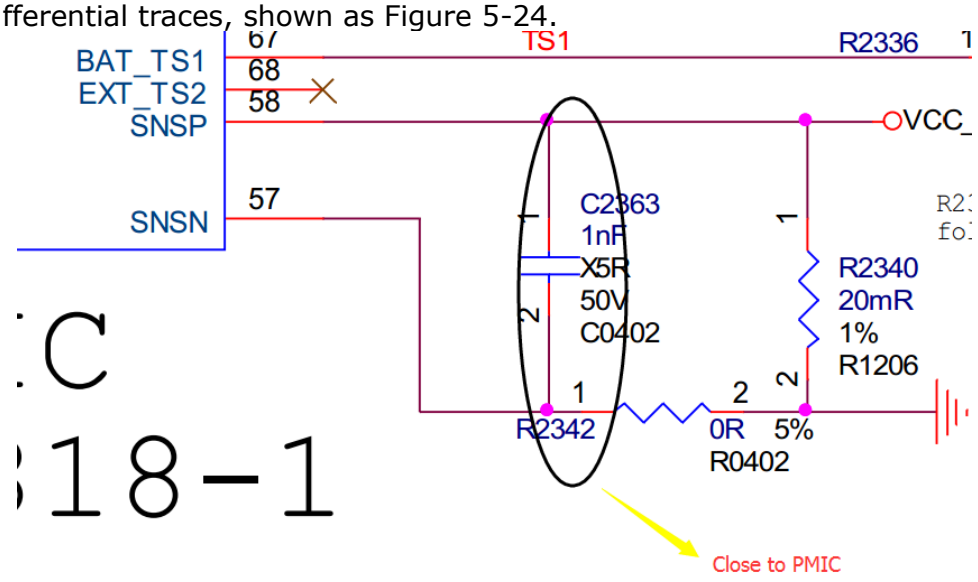


Figure 5-23

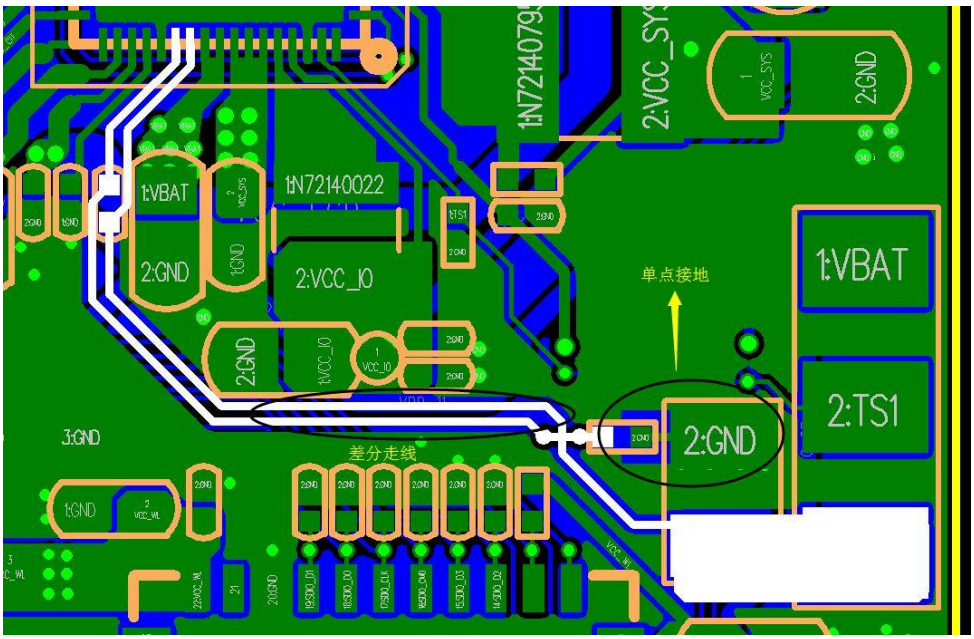


Figure 5-24

To improve the sampling accuracy of the battery, the capacitance C2363 (Figure 5-25) in the feedback circuit need to close to RK818, shown as Figure 5-25.

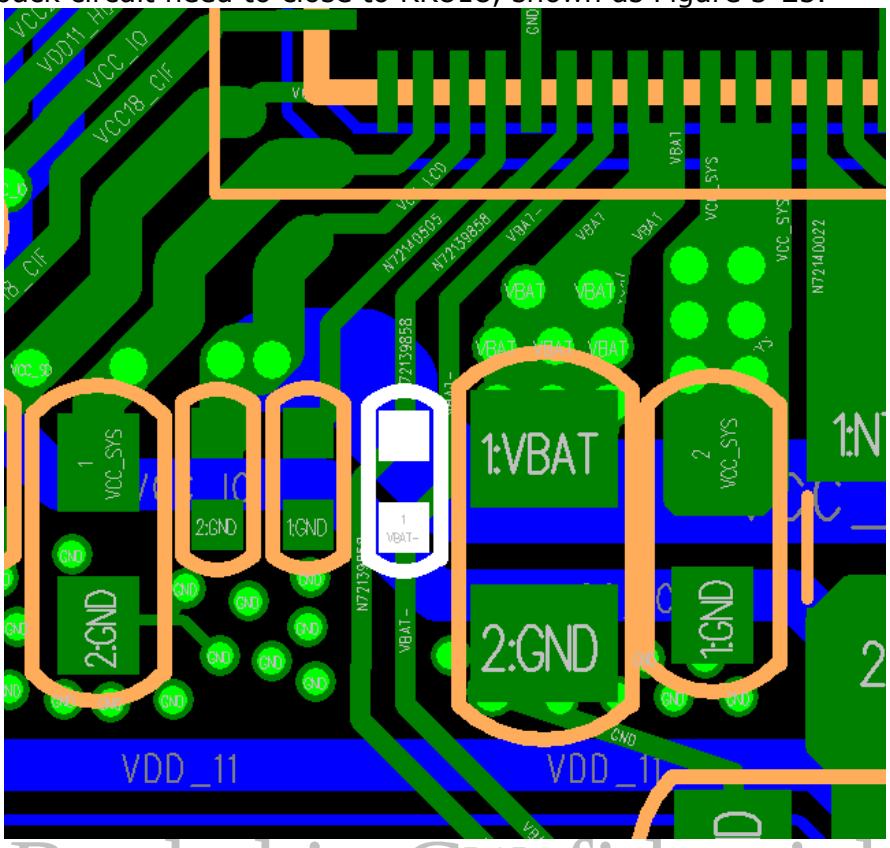


Figure 5-25

To ensure the performance and heat dissipation of the chip, please make sure RK818 has good GND connection, including GND pin connected to ePAD, which should have efficient GND vias, shown as Figure 5-26.

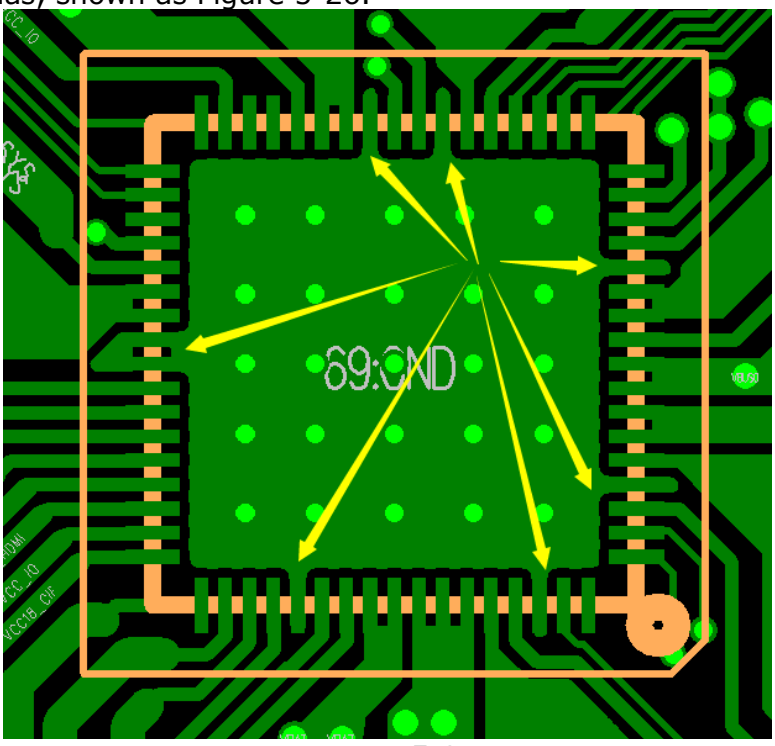


Figure 5-2

The clearance between SW5 and SW6 inductance must remain above 1.6mm, otherwise, the high pressure generated for mutual inductance may result in the damage of RK818; the value of BOOST output capacitance must be above 33uF, shown as Figure 5-27, Figure 5-28.

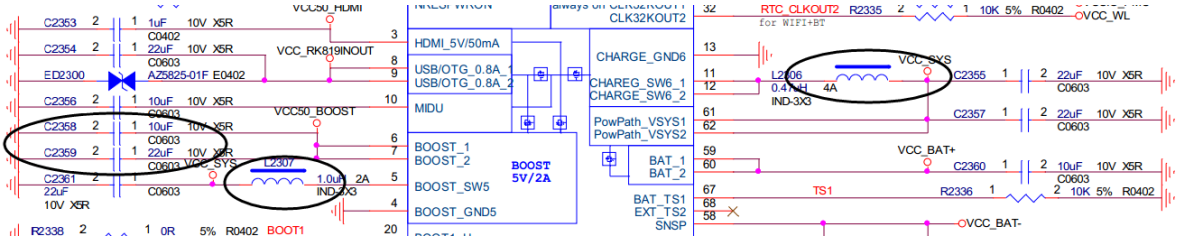


Figure 5-27

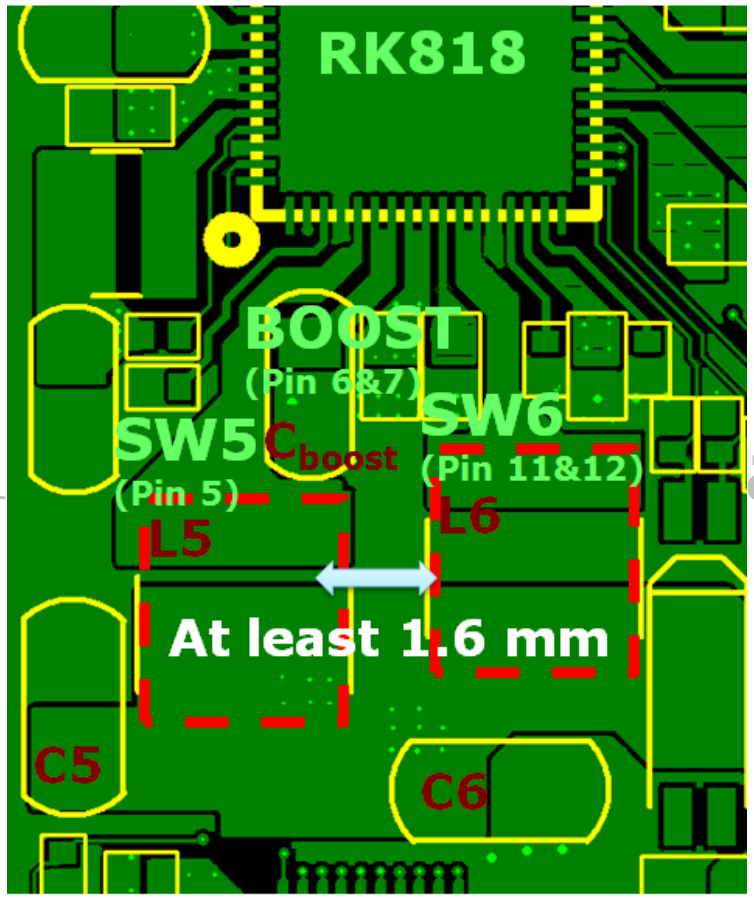


Figure 5-28

Power feedback traces must be traced along with output power plane, otherwise, it may cause power pressure instable for crosstalk, shown as Figure 5-29.

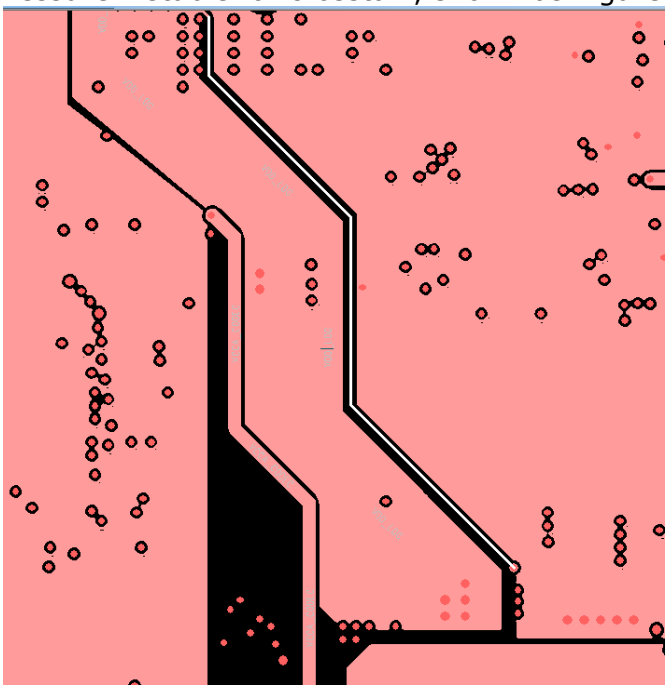


Figure 5-29

All input and output capacitances must close to RK818, and have efficient vias to ensure return current, especially the input/output capacitances of the high-current power supply, shown as Figure 5-29.

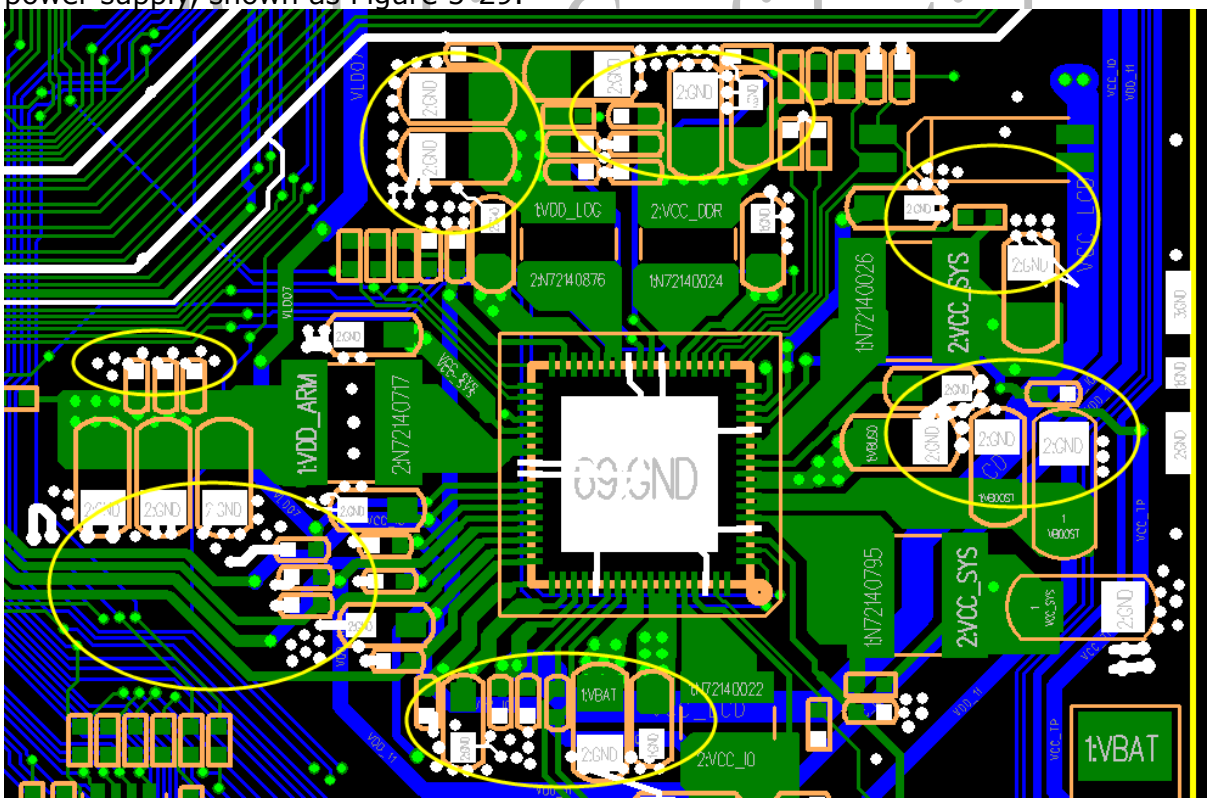


Figure 5-29

Chapter 6 GPIO

6.1 Schematic

In the actual product design, if want to change GPIO haven defined by Rockchip, please notice the level match of IO and the pull up/down characteristics of GPIO, otherwise the function may be abnormal. GPIO pull up/down in RK3288 is configurable and closable after power up, shown as Figure 6-1. The label "_d" in the schematic design package means the internal pull-down, and the label "_u" means the internal pull-up, if modification is needed, please refer to *RK3288 IO LIST V1.0 20140429* released by Rockchip.

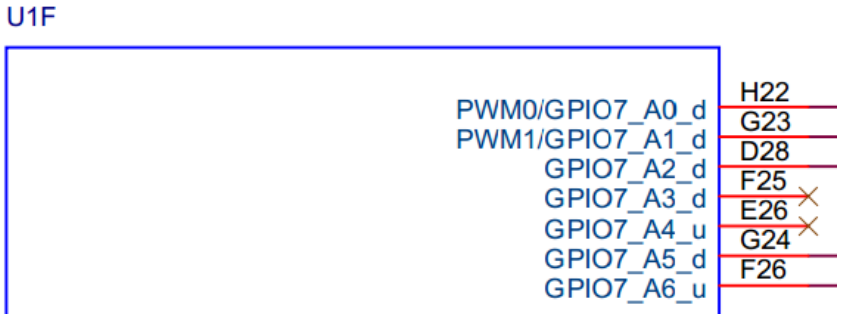


Figure 6-1

In the RK3288 application, BS_JTAG_TRSTn and APIO2_VDD must respectively be connected to GND and battery, shown as Figure 6-2. Otherwise the chip may work abnormally during the period of power up, and the specific performance is the failure of the default pull-up/down in the chip.

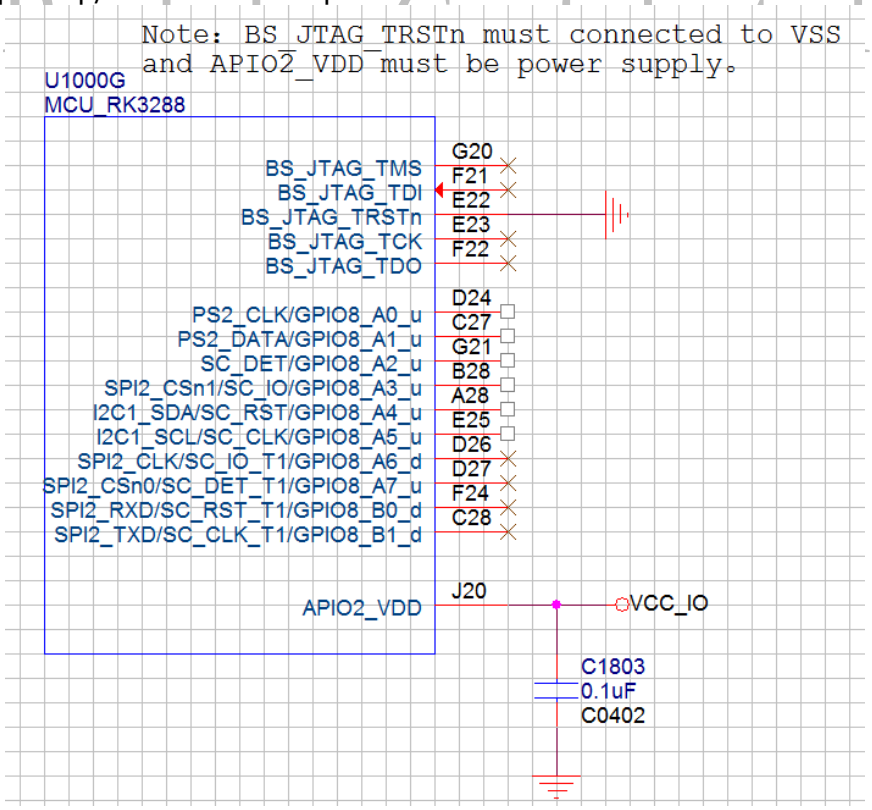


Figure 6-2

In the design of RK3288, all power pins of the function module with independent power supply should be placed in each function module, aiming to distribution as the needs and to the reduction of power dissipation, therefore, in the practical application, available modules except APIO2_VDD can break power supply to reduce the power dissipation, shown as Figure 6-3.

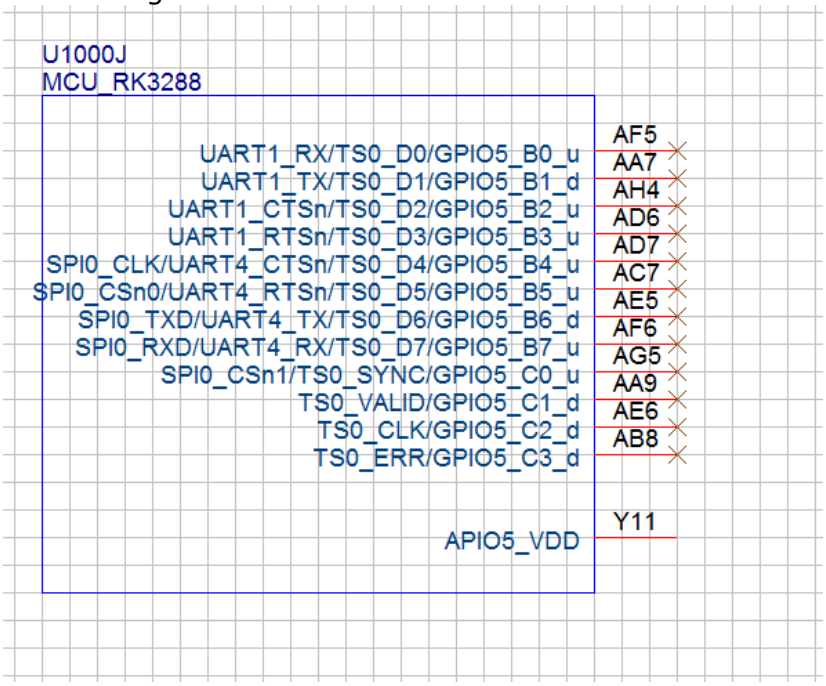


Figure 6-3

Different function modules according to the differences of power supply (1.8V, 2.5V or 3.3V) can be modified by regulator-name in dts file to adjust corresponding intensity of output driving, shown as Figure 6-4. The specific modifications please consult the software engineers of Rockchip.

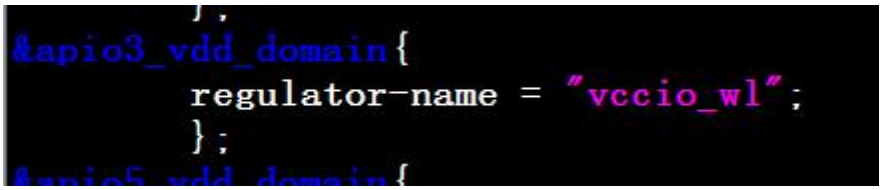


Figure 6-4

Tips:

1. GPIO allocation please design the products according to the IO list allocated in *RK3288_IO_LIST*, which can be used directly without modification to improve the progress and reliability of the product.

2. The IO can be modified by software after the IO pull-up/ down system of RK3288. Please refer to the relevant DATASHEET released by Rockchip.

Chapter 7 CPU&PMU

7.1 Schematic

RK3288 only needs an external 24MHz crystal, shown as Figure 7-1. Crystal Y1100 in the figure needs to use quartz crystal ± with 20ppm frequency deviation and ±30ppm temperature deviation, and the selection of the values of loading capacitors C1101 and C1102 need to refer to the actual value of loading capacitors. 8pF is the corresponding value of crystal chosen by Rockchip, which is not the universal value.

In order to reduce the jitter of crystal and PLL clock and avoid the over-jitter of the clock for poor design of return current, the reference GND of clock signal is OSC_XVSS pin. This design has certain requirements for PCB Layout, and if customers do not need to reserve adjustment, R1102 resistance can be deleted, then connecting OSC_SVSS to GND network.

When RK3288 configure low-power dissipation mode, switching the internal clock source to the external signal of 32.768 KHz, which can be receipted from PMIC or external RTC clock source through reducing the work frequency so as to decrease system dissipation.

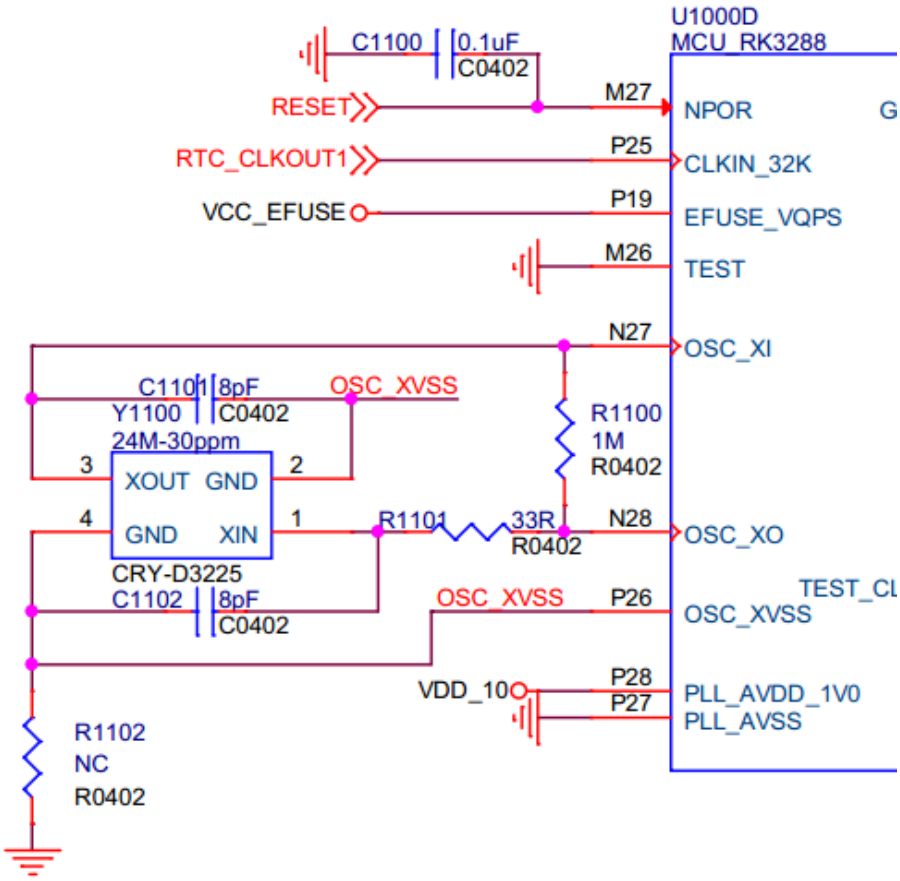


Figure 7-1

7.2 PCB Layout

The bottom, surface and second layer of 24MHz crystal prohibit other network traces. Please place crystal close to CPU when using OSC_XVSS as clock GND, and OSC_XVSS needs to be as the reference plane of crystal traces, shown as Figure 7-2.

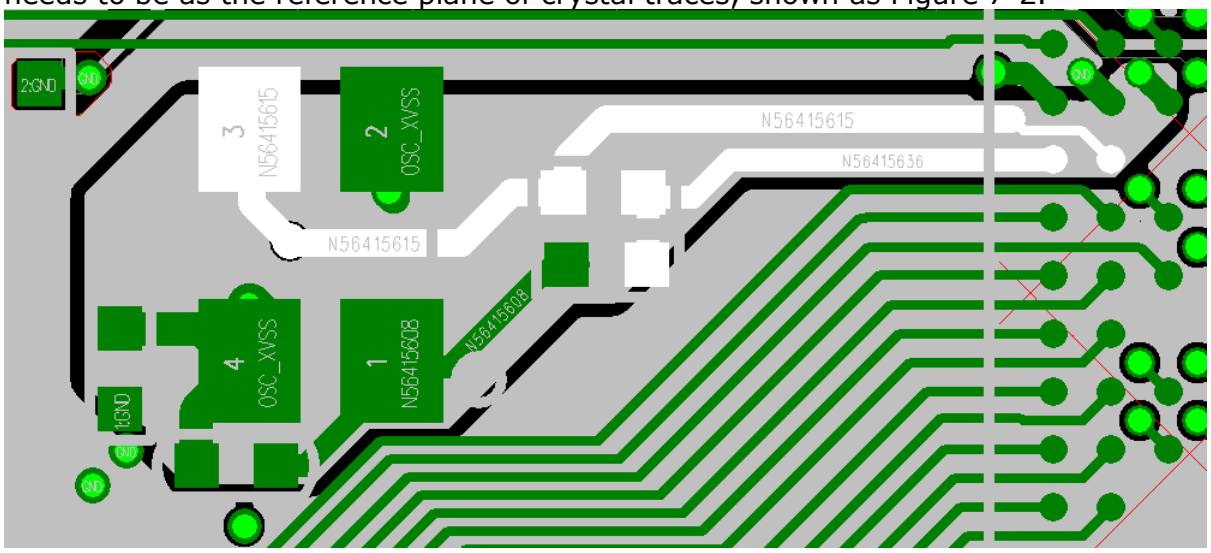


Figure 7-2

Please place crystal close to CPU when using GND as clock GND, and punch more vias on crystal pins and loading capacitors, shown as Figure 7-3.

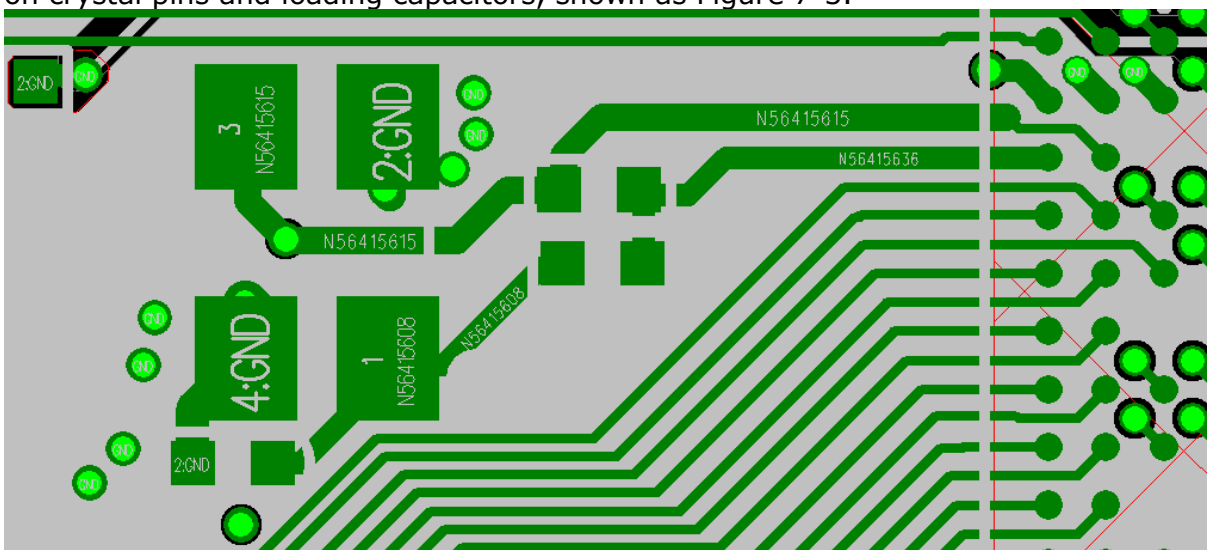


Figure 7-3

Chapter 8 DDR Controller & DRAM

8.1 Schematic

- RK3288 has 32bits DDR controller with two channels, which has the corresponding operation, and taking DDRO channel as an example to illustrate the grouping requirements of following signals:
  - 4 groups of cable (DATA0—DATA31), 4 DATA MASKS (DQM0--DQM3), 4 pairs of DATA STROBES differential traces (DQS0P/ DQS0M—DQS3P/ DQS3M), and these 36 traces and 4 pairs of differential traces are divided into 4 groups:

GROUP A: (DATA0—DATA7, DQM0, DQS0P/ DQS0M)
GROUP B: (DATA8—DATA15, DQM1, DQS1P/ DQS1M)
GROUP C: (DATA16—DATA23, DQM2, DQS2P/ DQS2M)
GROUP D: (DATA24—DATA31, DQM3, DQS3P/ DQS3M)

  - The rest of signal traces are divided into three types:

GROUP E: Address: ADDR0—ADDR14 have totally 15 address wires.
GROUP G: Control: including WE, CAS, RAS, CS0, CS1, CKE0, CKE1, ODT0, ODT1, BA0, BA1, BA2 etc. controlling signals.
GROUP F: Clock: CLK, CLKn differential pairs.

Address, Control and CLK classified as a group is for Address, Control output by DDR controller on the failing edge of CLK, and the DDR particle latches the condition of Address and Control bus on the rising edge of CLK, therefore, strictly controlling the sequential relationship between CLK and Address/Command, Control to ensure DDR particle to obtain efficient and best setting/holding time.

- No matter using DDR3, LPDDR2 or LPDDR3 is not allowed to exchange the Address traces and Control traces, which is GROUP E and GROUP G.
- When the data lines are exchanged among Groups, 4 DATA MASKS (DQM0--DQM3) and 4 pairs of DATA STROBES differential pairs (DQS0P/ DQS0M—DQS3P/ DQS3M) are also exchanged simultaneously, shown as Figure 8-1.

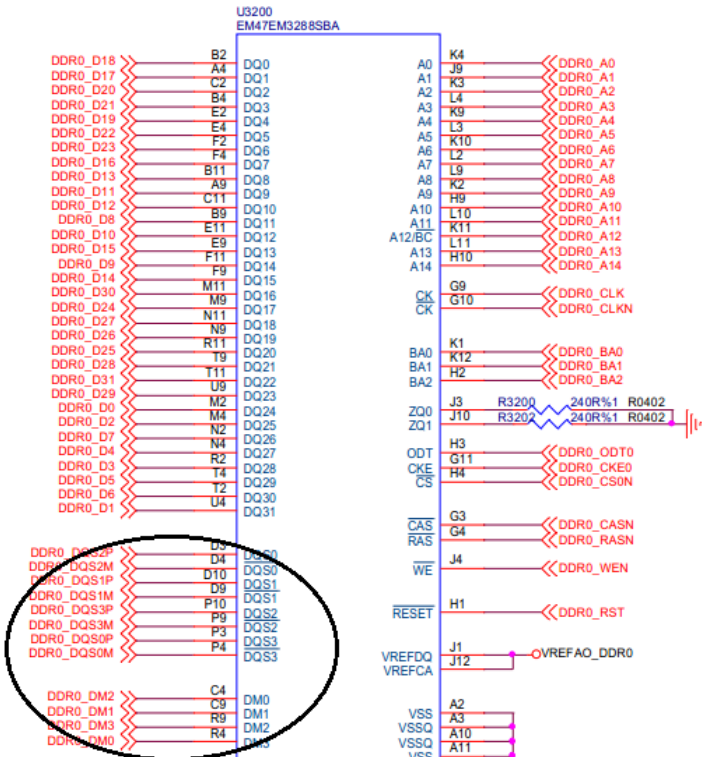


Figure 8-1

- If using DDR3, all date lines (GROUP A, B, C, D) can be exchanged in group (for example, exchange the order in DDR0_D8~D15), or among groups (for example, exchange GROUP A to GROUP D). Exchanges all depend on practical demands, shown as Figure 8-2.

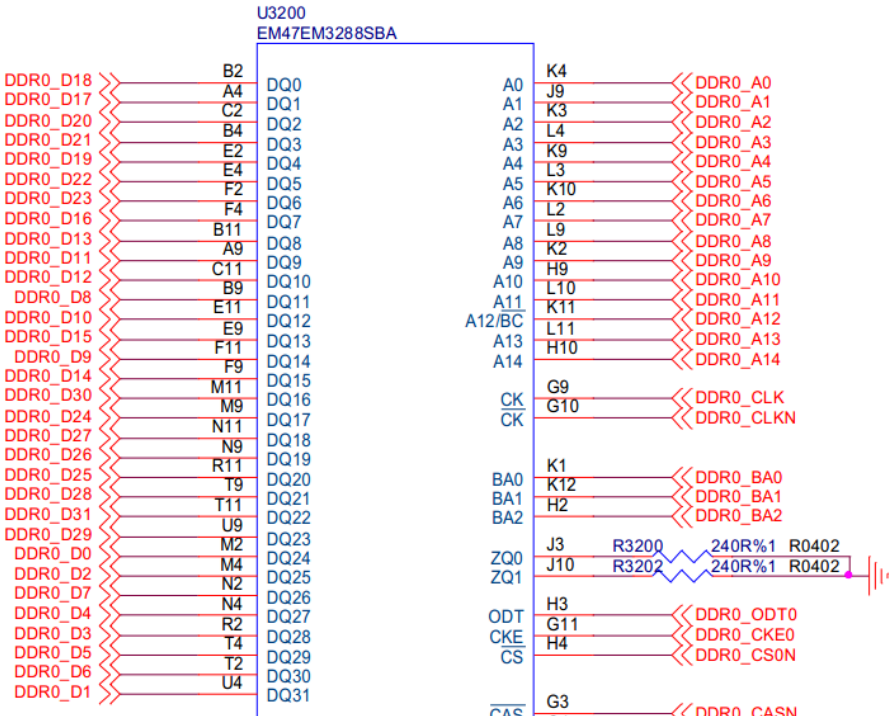


Figure 8-2

- If using LPDDR2/3, GROUP A of channel 0 cannot be exchanged in group and among groups, which require one-to-one correspondence to D0~D7 of A or B channels; Other date lines (GROUP B, C, D) can be exchanged in group (for example, exchange the order in DDR0_D8~D15), or among groups (for example, exchange GROUP B to GROUP C); All GROUPs of channel 1 can be exchanged in group or among groups according to the practical demands, shown as Figure 8-3.

Figure 8-3

- DDR_RETLE is the retention latch enable pin of DDR controller, which controls DDR PHY into refresh mode to reduce power dissipation, and the operation level of

this pin should be consistent with VCC_DDR. Using divider resistance R1204 (120K), R1206 (120K) under DDR3 mode to keep level match (Figure 8-4). Please modify the divider resistance value as R1204 (100K), R1206 (82K).

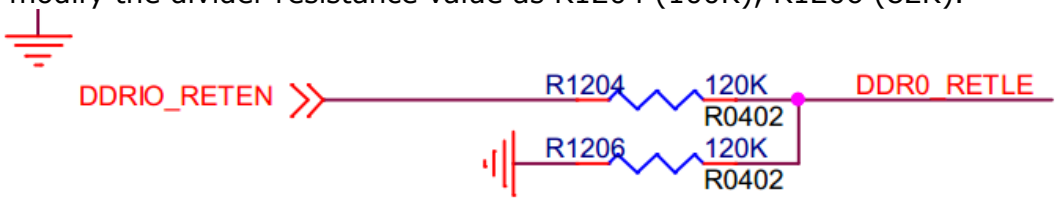


Figure 8-4

- Please ensure the reference power divider resistance to use the resistance of 1% accuracy. VREF_DDR power supply is closable during hibernation, and the two divider resistances are 1K; While VREFAO_DDR power supply cannot be closed during hibernation, thus using 10K divider resistance to reduce power dissipation, and to make sure the following features of battery. The resistance should be connected respectively 0.1uF capacitor in parallel, shown as capacitors C1208 and C1210 in Figure 8-5.

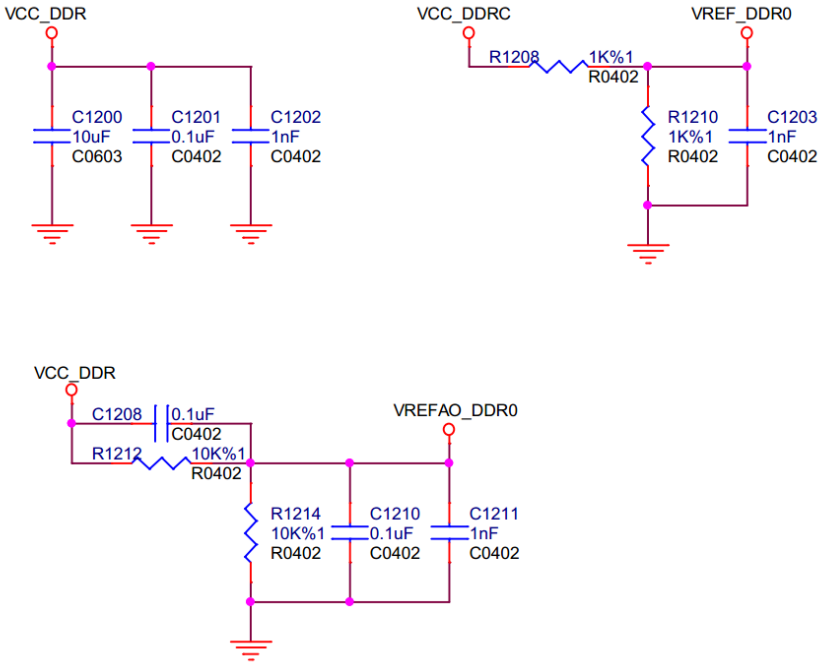


Figure 8-5

- As for branched DDR topological structure, like DDR3, 0402 footprint resistor should be reserved between DDR_CLK and DDR_CLKn, and try to close to the branch point of DDR clock trace in Layout, which can be simple processed at the problem of EMI.

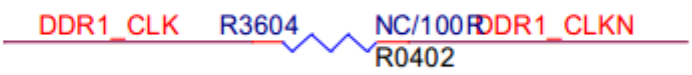


Figure 8-6

- VCC_DDRC power supply is controlled by NMOS Q3200, and turning off the VDDQ power supply to reduce system power dissipation, shown as Figure 8-7. In

LPDDR2/3 mode, adding an NMOS Q3300 to avoid VCC_DDRC UVP (1.2V) leading to connection inadequacy, shown as Figure 8-8.

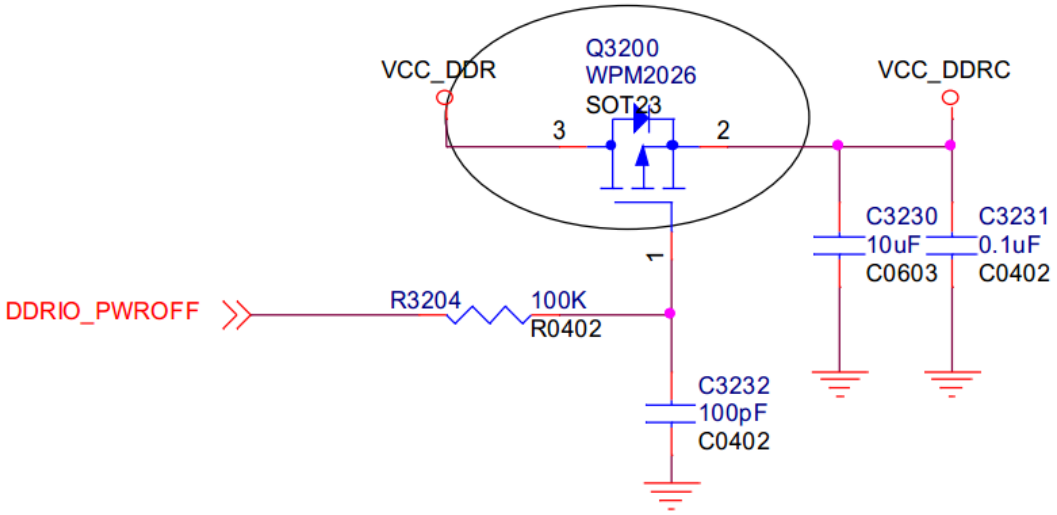


Figure 8-7

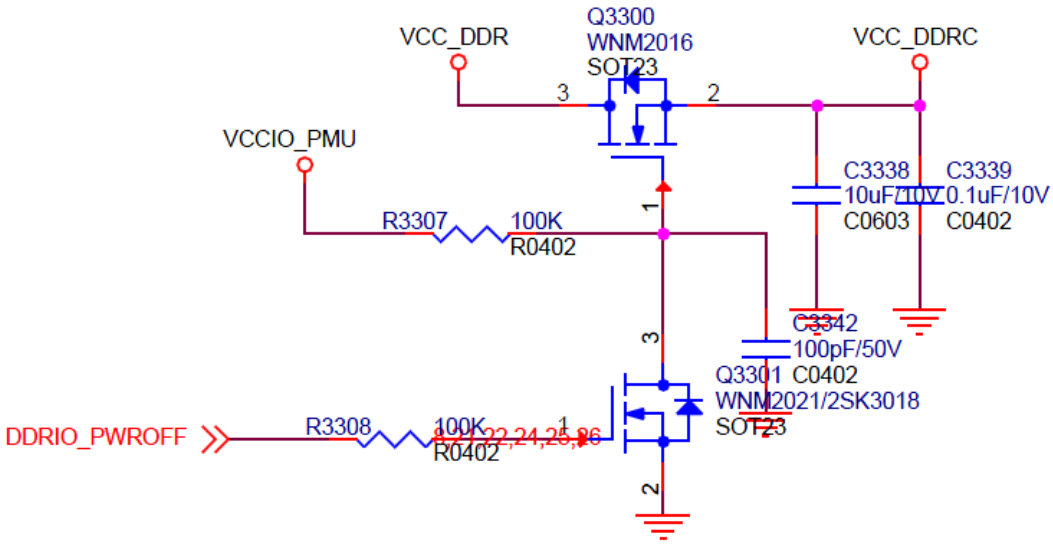


Figure 8-8

8.2 PCB Layout (DDR0 channel, DDR1 channel)

To ensure the good performance and compatibility of DDR, please operate in strict according to the following requirements, otherwise, the performance and stability of product may be degraded, even in severe case, the system may not operate properly.

✧ Clearance

➢ The clearance between the different signal traces in the same group should be above 3W.

➢ The clearance between the two adjacent signal traces in different groups should be above 3W.

➢ For the ball distance of RK3288 is 25.59mils, the clearance between the two adjacent signal traces in the same group should be 12.795mils, which is the half distance of the center distance of pad. And 3W rule is conformed as long as the traces fan-out from SOC parallelly and equidistantly.

✧ Signal trace length requirements

The trace length errors between DQSnP/DQSnM of GROUP A ~D are controlled within 5mils; the differential internal signals skew between the data line DATAn of each GROUP and DQMn group are controlled within 50mils; The date between groups have only to within 120mils.

The trace length errors between GROUP E and GROUP G are controlled within 100mil.

The trace length errors of differential pairs of CLK, CLKn in GROUP F are controlled within 5mil.

Making length difference between CLK, CLKn in GROUP F and DQSnP/DQSnM in GROUP A~D satisfy tDQSS timing parameter can refer to the following design rules(advices):

- DDR1600: Length (CLK) –Length (DQSn) <900mils
- DDR1333: Length (CLK) –Length (DQSn) <1200mils
- DDR1066: Length (CLK) –Length (DQSn) <1700mils
- DDR800: Length (CLK) –Length (DQSn) <2600mils

✧ Other Traces Notes

➢ DQS signal trace should be traced in the middle of DQ signal trace of intergroup.

➢ DQS does not adjoin to the clock.

➢ Center-to-center spacing between serpentine curves should comply with 3W rule, and the amplitude of serpentine curve should be controlled within 180mils, otherwise, the quality of signals would be destroyed resulting in the transmission delay lower than the expectation.

➢ The signal trace of DDR3 must have a complete reference surface to ensure the minimum of backflow impedance of the signal circuit and the continuity of the impedance.

➢ Prohibit all signal traces of DDR3 to cross different power plane.

➢ Prohibit other types of signal lines to cross the area of DDR traces.

➢ Each VCC_DDR pin of RK3288 and DDR particle tries to be placed a decoupling capacitors on the back of chip, and the vias should be placed next to pins to avoid increasing inductance of traces.

✧ Disposal of VREF

➢ VREF of SOC and DDR3 should be divided and obtain respectively partial pressure from VDDQ. VREF tries to close to the chip, while VREF traces should be as short as possible and be divided with any other data lines to ensure without

interference (pay more attention to the crosstalk between adjoining layers), and good tacking characteristic compared to VDDQ, and ensure the voltage values of VREF to change with VDDQ when the noise and the temperature is changing.

- VREF only needs to provide rather small current (the input current is about 3mA), every VREF pin should be close to 1nF bypass capacitor (the amount of each capacitors should be not more than 5 to degrade the supply power tacking characteristic), and the trace width had better no less than 10mils.

✧ Impedance requirements .

- The width of single trace is 4mils, the impedance control is 55ohm±10%
- The width of differential pairs is 4mils, the impedance control is 100ohm±10%
- The variation range of permittivity of the PCB packing material is 4.0~4.5, and the value floats with the factors like frequency, temperature etc. FR-4 is the typical dielectric material, and the average permittivity is 4.2 in 100MHz; it is recommended to use FR-4 as the PBC packing material.
- Ensure the integrity of copper.
- The integrity of copper in the part of DDR will directly influence the performance and compatibility of DDR. Design as follows can achieve the effect shown as Figure 8-9.

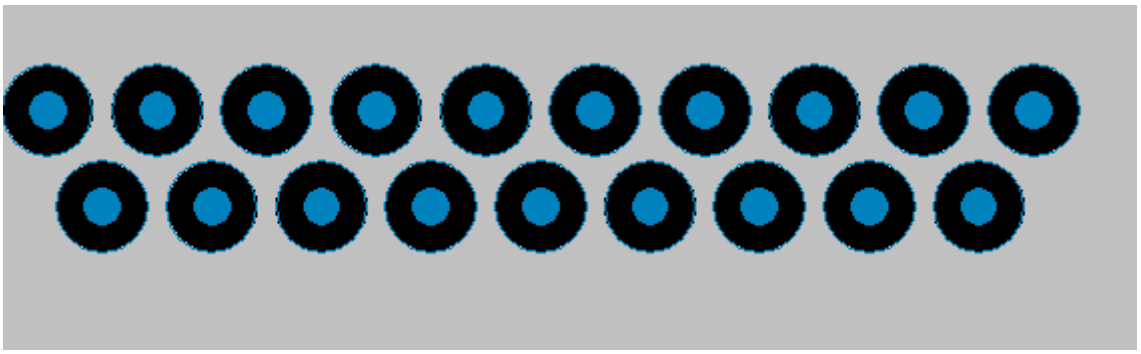


Figure 8-9

- Ensure the vias of signal traces in swapping layer to distribute homogeneously and the clearance between two vias is greater than or equal to 32mils.
- Use 0.2mm diameter, 0.4mm via of the hole plate.
- Set copper layer attribute as split/mixed plane.
- Set the clearance between via and copper as 5.5mils.
- Set the width of copper as 4mils.

Note: Please refer to DDR core template PCB document and corresponding design specification document.

Chapter 9 Flash control & Memory

9.1 Schematic

RK3288 supports FLASH like Nand Flash, eMMC, tSD. When using Nand Flash, tSD Flash, controller and VCC_FLASH device are 3.3V (R1300 in Figure 9-1 is NC). However, VCC_FLASH of controller and FLASH particle may be 1.8V (above eMMC4.1) or 3.3V in different versions. Please adjust according to Datasheet and modify the state of pull/down of FLASH0_VOLTAGE_SEL, shown as Figure 9-1.

Tips

- **Advise VCC_FLASH to use 1.8V power supply to stabile high-speed when using eMMC;**
- **FLASH 1 channel does not support eMMC Flash;**
- **Boot is guided by FLASH 0 channel by default, which cannot be modified;**

Table 9-1

FLASH0_VOLTAGE_SEL (Internal pull-down by default)	1.8V	3.3V
	VCC_FLASH	GND(default)

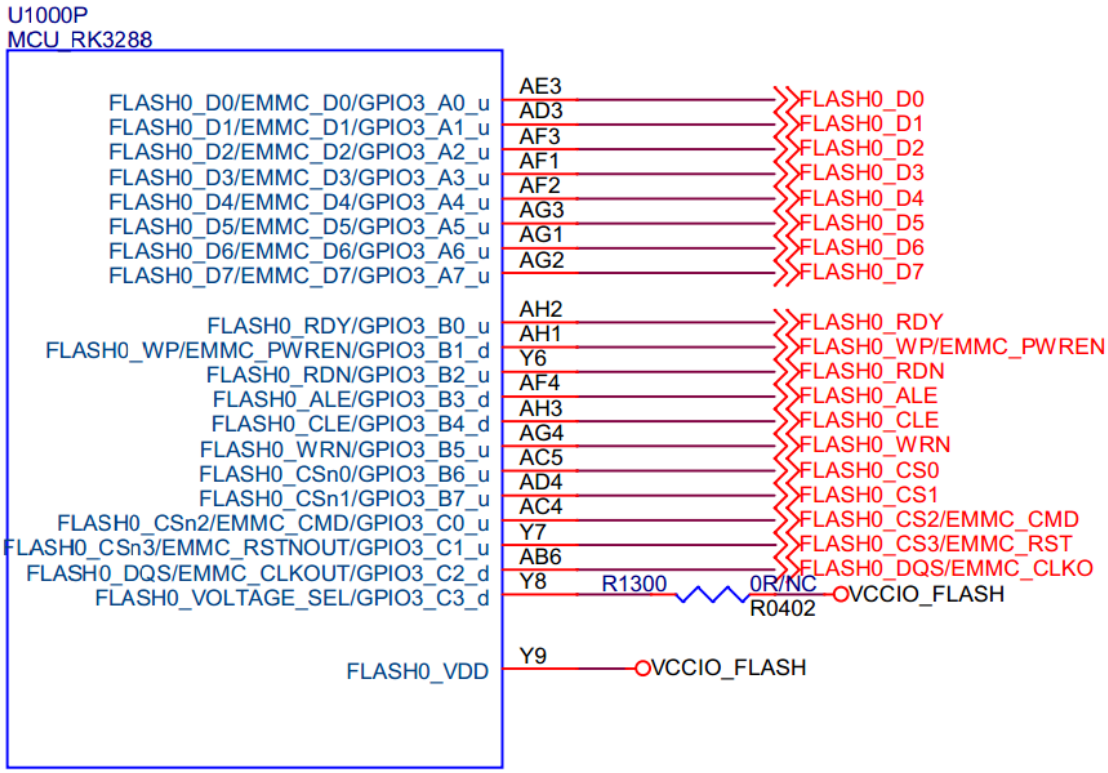


Figure 9-1

When using Nand Flash, the schematic diagram is shown as Figure 9-2. When using Nand Flash of DDR mode of Toshiba and Sandisk, VCCQ1 and VCCQ4 should be connected to VCC_IO power supply, which means R4001, R4003, R4004, R4005 should be mounted with 0R resistance.

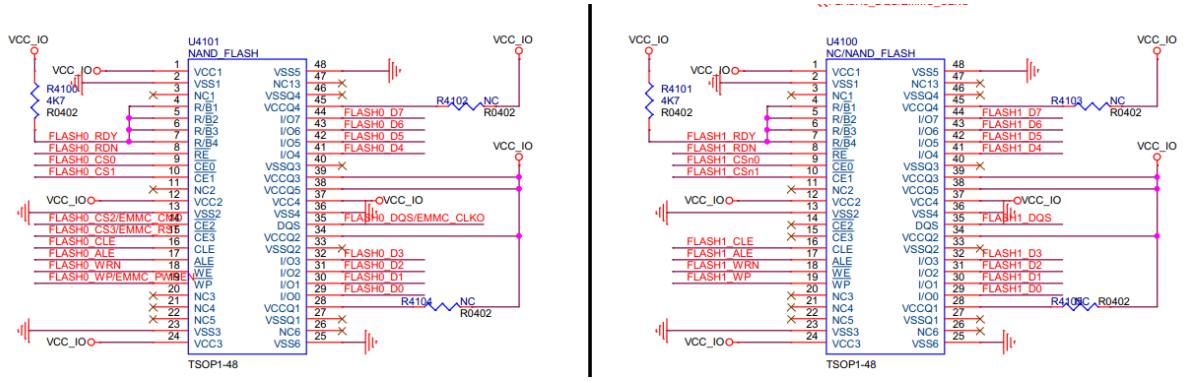


Figure 9-2

When using eMMC Flash, the schematic diagram is shown as Figure 9-3. Signal eMMC-DATA/CMD pull-up resistances use 10K and connect to the power supply VCC_FLASH, and eMMC-CLK do not need to pull-up.

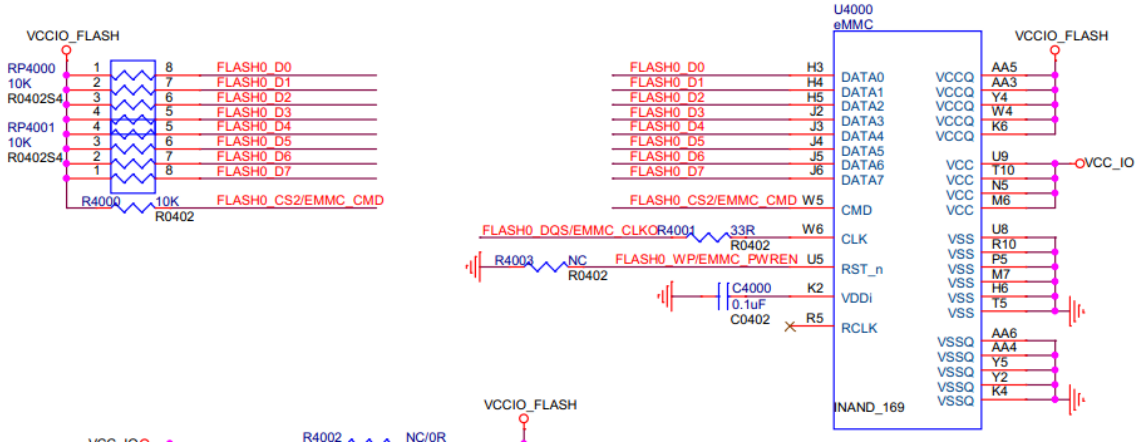


Figure 9-3

eMMC is set 1.8V LDO power supply by default, shown as Figure 9-4, eMMC4.1 is compatible, and the range of candidate materials are wider.

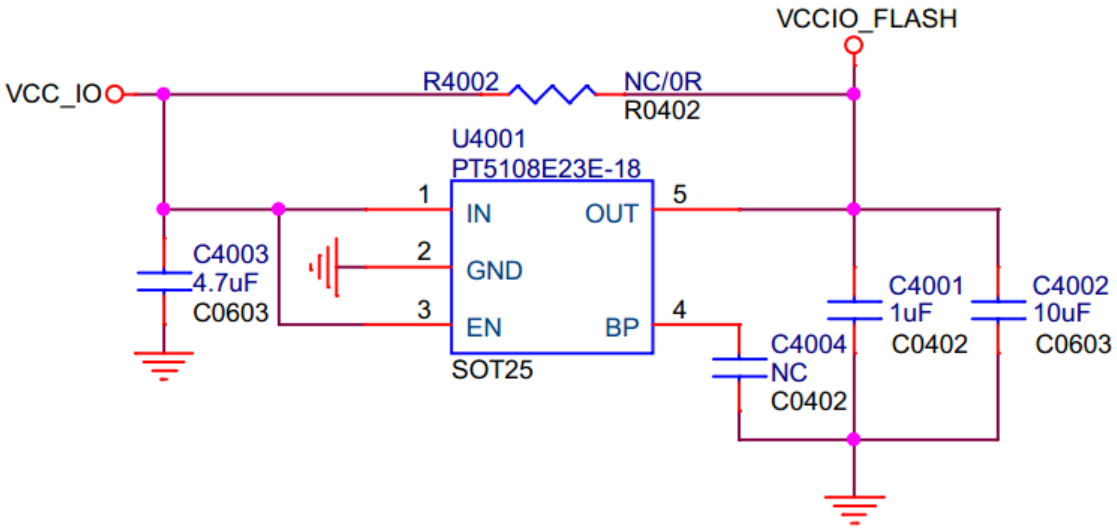


Figure 9-4

In order to facilitate enter Maskrom mode in development stage (require to update LOADER), FLASH_CLE needs to reserve a test point when using Nand Flash, while when using eMMC Flash, the test point needs to be reserved by EMMC_CLKO, shown as Figure 9-5, Figure 9-6.

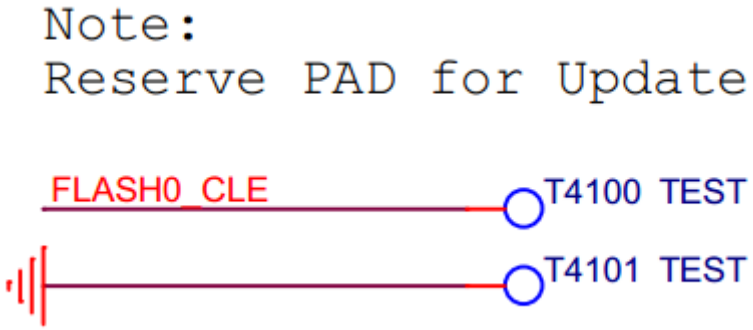


Figure 9-5

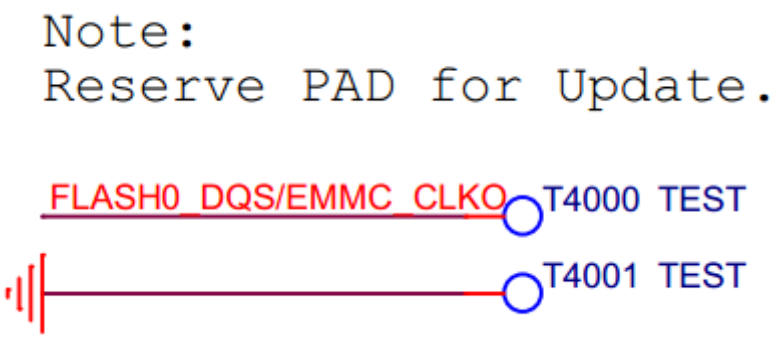


Figure 9-6

9.2 PCB Layout

Nand Flash and eMMC Flash can achieve the material exchange through double Layout, which is shown as Figure 8-7. When coppering below eMMC, the part of pad needs to add one area with cutting out copper to avoid the nonuniform distribution of copper foil to influence heat dissipation and resulting in pseudo soldering.

The group traces of eMMC Flash should be shielded by GND traces, and the skew of any two signals in the signal group should be controlled within 400mil, otherwise, the frequency in high speed mode would not meet to the standard. The PCB Layout length of eMMC try to limit in 12.4inch. It is recommended to use drive strength and Timing Tuning adaptive algorithms to promote the stability and compatibility of eMMC.

Attention that the power supply ripple cannot be above 80mV in Flash, therefore, the traces of power supply should keep away from the high way. The data lines of Flash cannot close to high-current signals of large ripple like Vbus, Vdc, VCC_SYS.

The test points of firmware upgrade mode are recommended to close to Flash, and be placed on the device placement layer (not adjoin to the side of LCM) to facilitate upgrade, shown as Figure 9-7.

Layout follows the Figure 9-8, the signal traces can pass by eMMC unused pins. The way can reduce PCB spacing requirement.

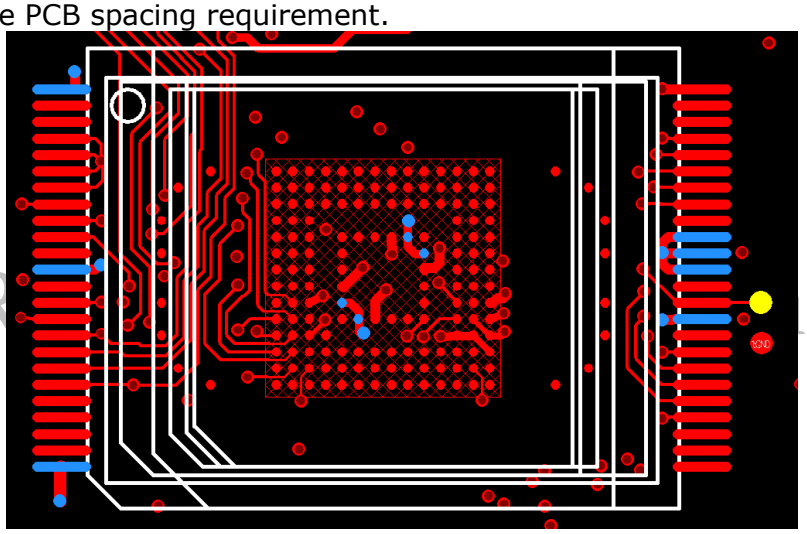


Figure 9-7

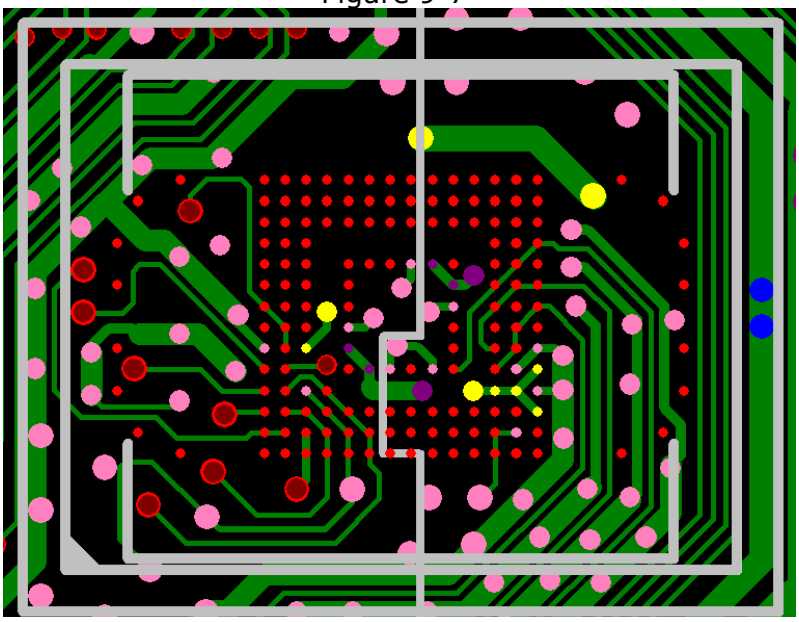


Figure 9-8

Chapter 10 TF Card

10.1 Schematic

Memory card adopted by the reference Rochchip's drawing published is TF card, if needed to change into SD card, please pay attention to the deck package.
The circuits of TF are compatible of SD 2.0/3.0, and VCCIO_SD power supply of module is adjustable and the defaults of power supply is 3.3V, while VCC_SD power supply of TF card is 3.3V. When inserting SD 2.0 memory card, VCCIO_SD and VCC_SD are both 3.3V. When inserting SD 3.0 memory card, SOC identifies as SD 3.0 device and adjusts VCC_SD as 1.8V to meet the demands of SDHC signal; meanwhile VCC_SD of TF card generates 1.8V power supply through internal LDO.
When using SD 3.0 memory card, it is recommended to add pull-up resistances R8107-R8112 pulling-up to the power supply VCCIO_SD to promote the stability of date, shown as Figure 10-1.
If need to support SD 3.0 memory card, ESD devices please choose the junction capacity lower than 10pF, shown as Figure 10-1.

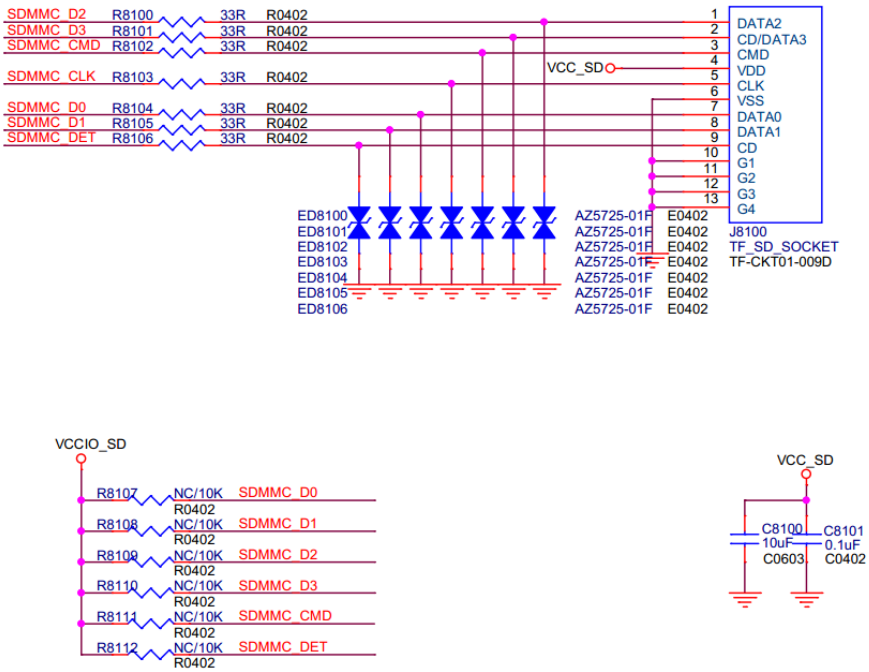


Figure 10-1

10.2 PCB Layout

The capacitors of TF deck VCC_SD, C8100, C8101, should be close to deck pin in Layout.
Try to trace away from other high-frequency signals and shield the group traces by GND traces. If having rich space, CLK is recommended to be shielded separately by GND traces.
TF card traces require the skew of any two signals in the signal group should be controlled within 400mil, otherwise the signal in high speed mode would not meet to the standard.

Try to limit the length of PCB Layout of TF Card in 12.4inch in RK3288 board. It is recommended the

customers to use drive strength and Timing Tuning adaptive algorithms to promote the stability and compatibility of SDIO.

Chapter 11 USB & HSIC

11.1 Schematic

RK3288 has three USB interfaces, one of them is USB OTG, and the other two are USB HOST, shown as Figure 11-1.

- USB OTG interface can configure for Host or Device function through detecting the signals of USB_VBUS and USB_ID, and support the specification of USB2.0/1.1.
- USB HOST interface can be regarded as HOST interface external device, in which HOST1 only supports the specification of USB 2.0, while HIST2 can support the specification of USB 2.0./1.1. The application of BOX solution gives priority to use the HOST2 interface.

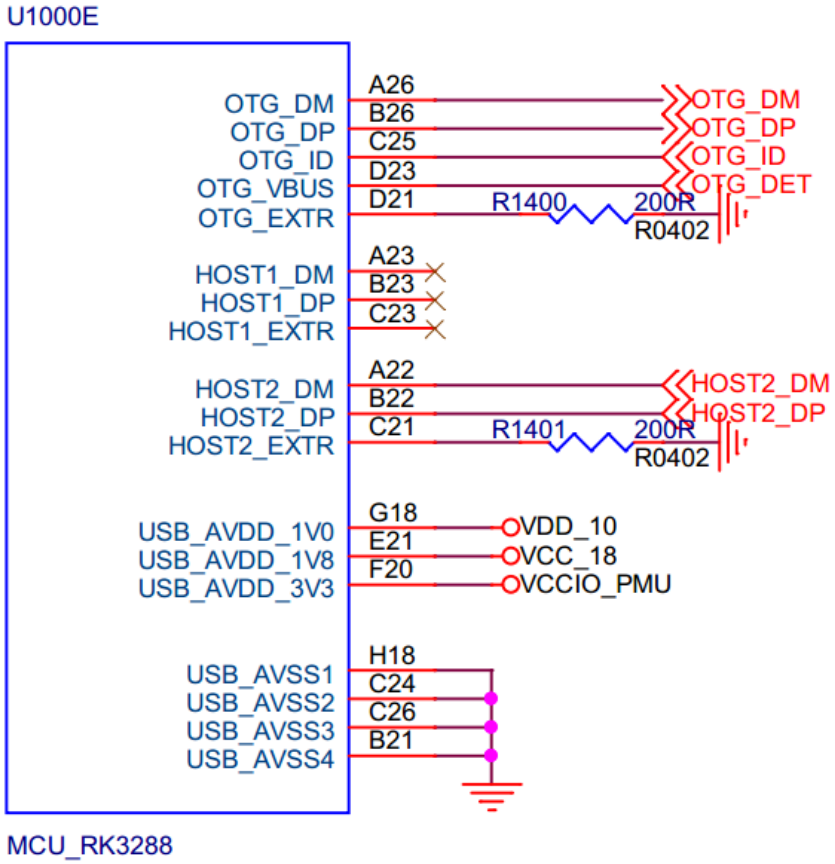


Figure 11-1

The reference resistances of USB controller, R1400, R1401, please select the resistances of 1% accuracy which relates to the USB eye diagram.

The transmission rate of USB is up to 480Mbps, therefore the differential signals are very sensitive to the parasitic capacitance in the traces. Thus, to choose the ESD protection device with low junction capacitance which should less than 1pF.

In order to suppress EMI, it can be considered to reserve the common mode choke on the signal traces, and the resistance or common mode choke is chosen according to the actual situation in the debugging process, shown as Figure 11-2.

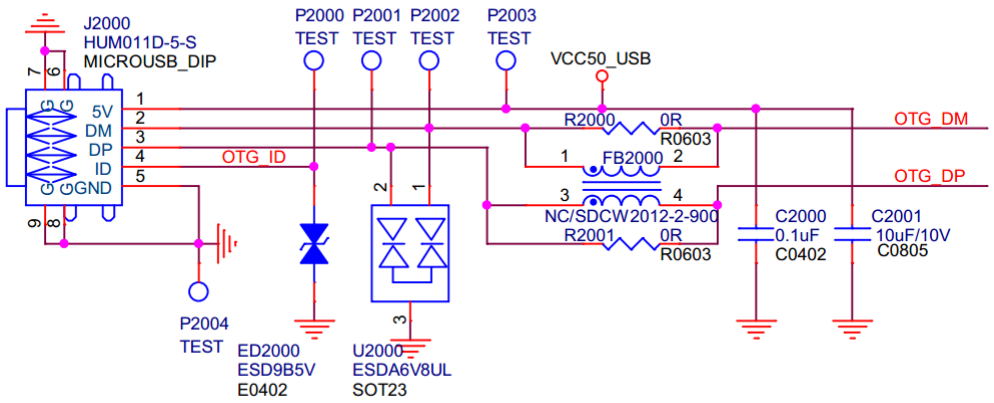


Figure 11-2

11.2 PCB Layout

The following is the USB PCB Layout notices:

- USB interface should be placed close to the chip as much as possible to shorten the trace distances.
- The USB signal traces must strictly follow the requirements of differential pair rules. Using arc or obtuse angle at the corners of traces as much as possible, right-angle or acute angle is unallowable, and the impedance requirement Z=90±10ohm, shown as Figure 11-3;

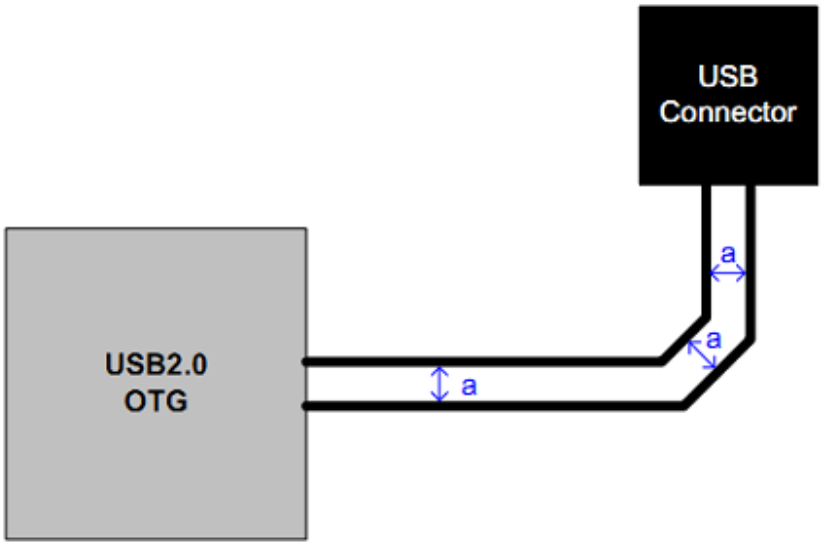


Figure 11-3

-
-
-
-
-
- In order to suppress EMI, the USB signal traces is recommended to be placed in the inner layer and ensure that the reference plane is continuous and complete, otherwise, it will cause discontinuities in the trace impedance and increase the external noise on them, shown as Figure 11-4. If tracing on the PCB surface, please shield by GND traces, shown as Figure 11-5.

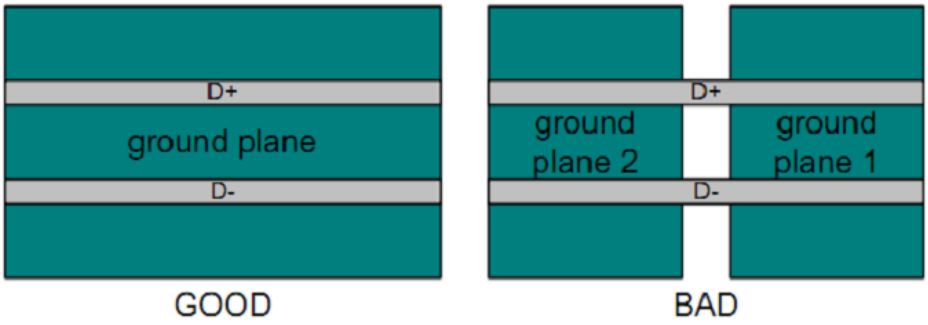


Figure 11-4

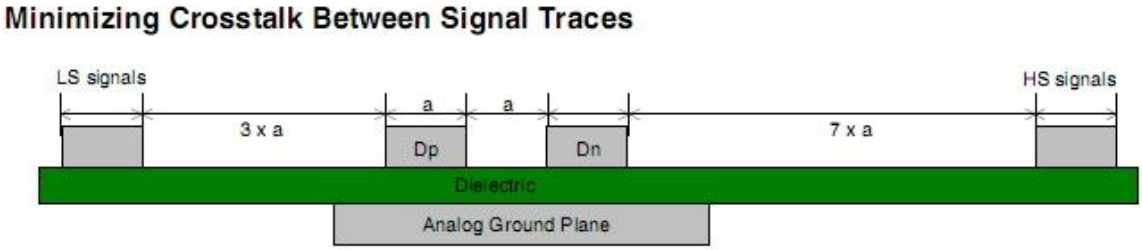


Figure 11-5 USB Layout

- Try to reduce vias between different layers in layout, otherwise, that would cause the discontinuous trace impedance.
- The power current of USB 2.0 specification is 500mA, but the VBUS traces had better withstand 1A current to avoid overcurrent. If under the situation of charging by USB, the VBUS traces should withstand 2.5A current.
- ESD protection device, common mode choke and large capacitance should be placed close to USB interface as much as possible, shown as Figure 11-6, Figure 11-7.

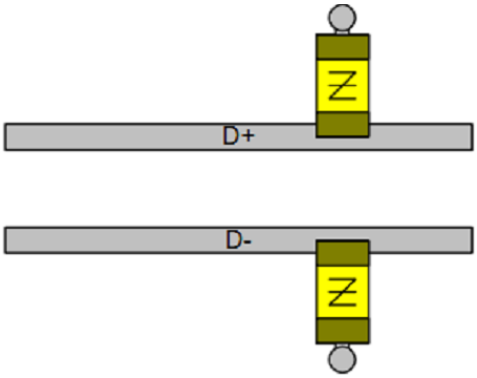


Figure 11-6

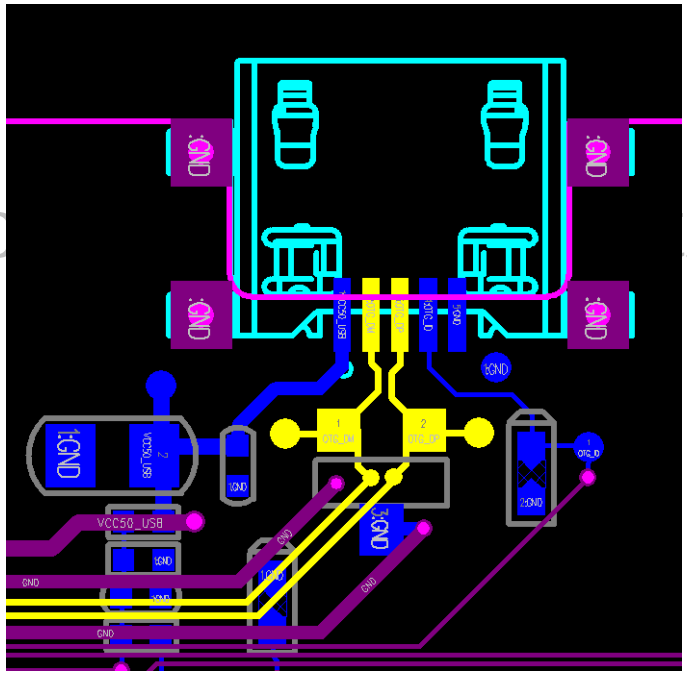


Figure 11-7

Chapter 12 SADC & Key

12.1 Schematic

RK3288 adopts ADC_IN1 of SARADC as scanning channel of key value, and it can multiplex with RECOVER mode (not update LOADER), shown as Figure 12-1. In the premise of having firmware in the system, pressing SW1500 at startup to keep ADC_IN1 on 0V Level (the maximum cannot over 100mV), then RK3288 enters Rockusb mode. When PC identifies the USB, releasing key press to make ADC_IN1 return to high-level (1.8V), which can enter the firmware programmer.

The sample range of SARADC is 0-1.8V in RK3288, and the sampling precision is 10bits.

The key array can increase or decrease key and adjust the ratio of the divider resistances to adjust the input key value, realizing the multi-key input to meet the demand of customers. It is recommended that the voltage difference of any two key value must be greater than 250mV.

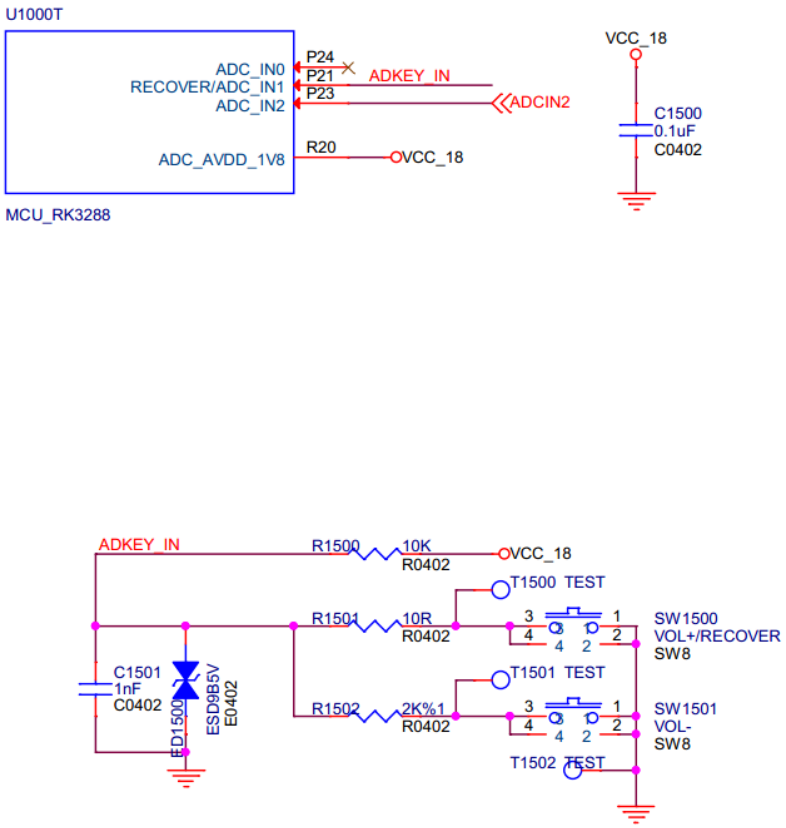


Figure 12-1

Tips:

- **The entry method of the recover mode cannot be modified by oneself.**
- **If the key is unnecessary in design, the pull-up resistance R1500 of ADC_IN1 must be reserved.**

12.2 PCB Layout

The following is the notices of Key PCB Layout:

- Please place ESD protective part close to the key to play the roles of ESD protection, shown as Figure 12-2;
- Please place the elimination buffeting of keystroke capacitor C1501 close to the chip;
- Isolate ADKEY_IN traces and other signal traces by GND traces to avoid crosstalk between signals resulting in misjudgments.

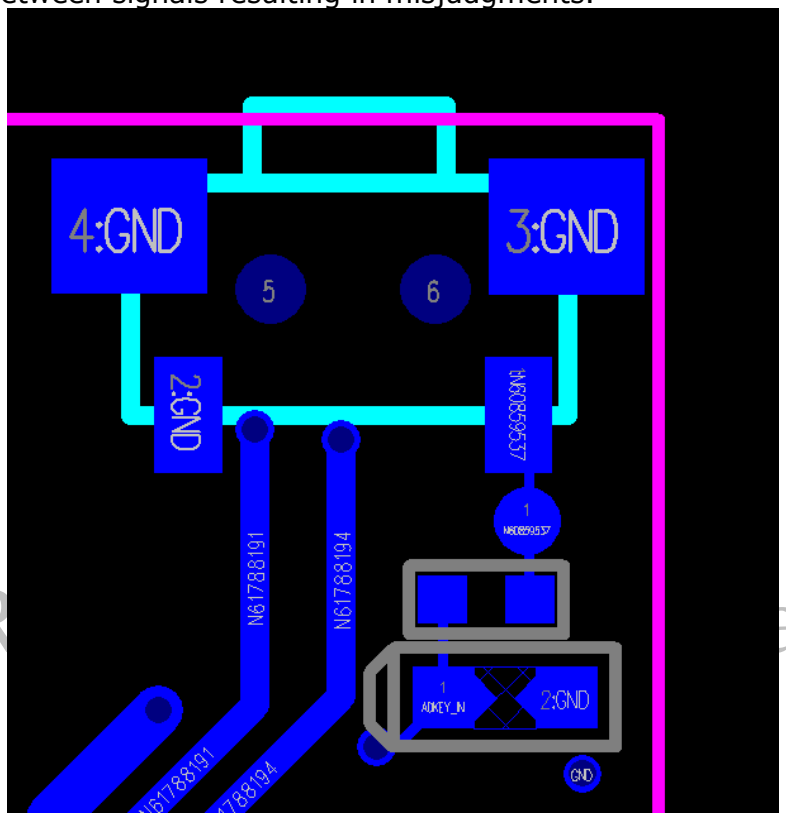


Figure 12-2

Chapter 13 DVP Interface & Camera

13.1 Schematic

DVP digital power domain is DVPIO_VDD power supply, and in the actual product designs, according to the actual demands of IO power of Camera (1.8V or 2.8V), choosing the corresponding power supply, meanwhile the I2C pull-up level must be consistent with it, otherwise, the Camera would work abnormally or incapably, shown as Figure 13-1.

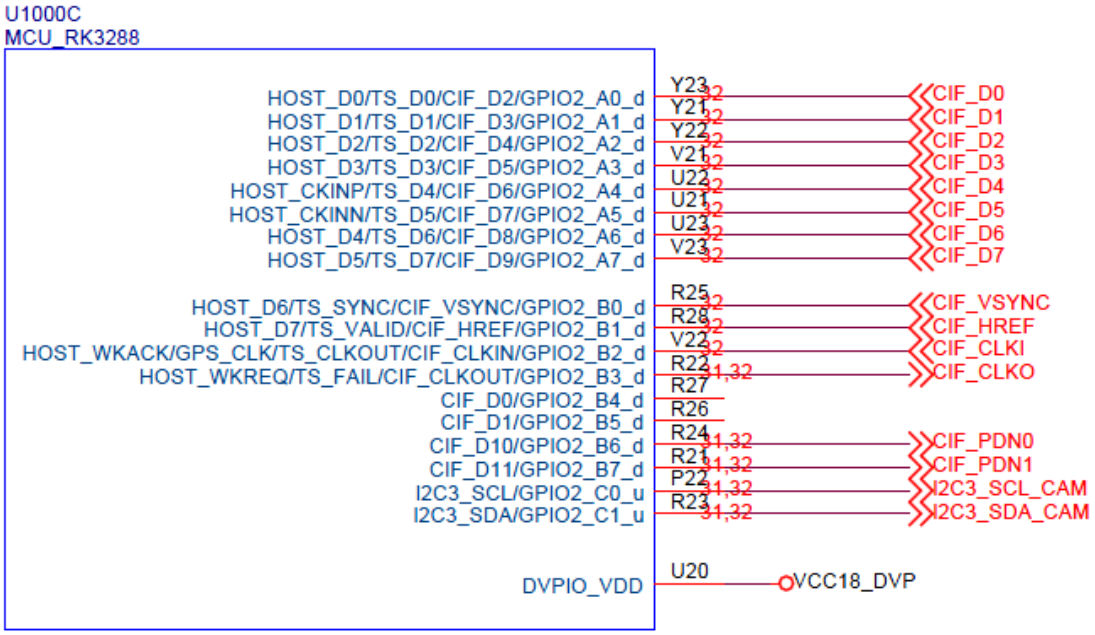


Figure 13-1

In order to avoid the over-length of Camera traces in the actual products to cause timing problems and abnormal data collection, therefore, RC delay circuit shown in Figure 13-2 needs to be added. Notice that the flow direction of clock signals and the corresponding parts should be placed close to signal output terminal.

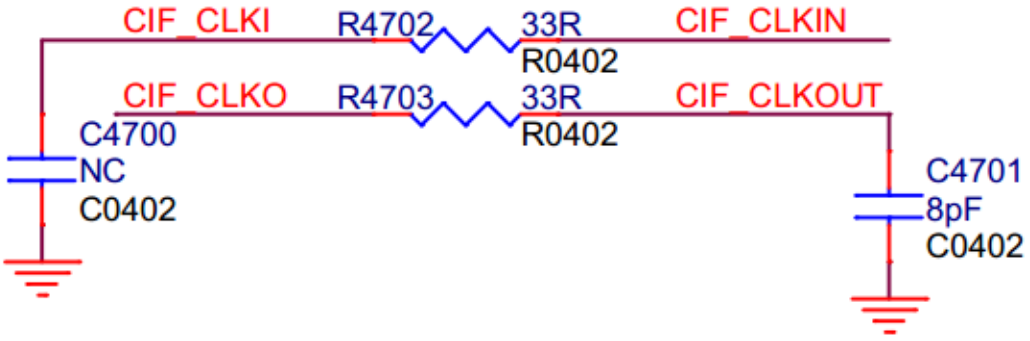


Figure 13-2

Notice when using DVP SOC Camera Sensor:

- Recommended to connect YUV data bit0-bit7 of Sensor output to bit2-bit9 of RK3288 DVP interface.
- Recommended to adopt RAW Sensor output mode when not requiring the front and rear cameras to work simultaneously.
- Only one of the two DVP SOC Sensors is RAW Sensor and one of them must be MIPI Sensor when requiring the front and rear cameras to work simultaneously for RK3288 having only one ISP processor.

RK3288 support double MIPI Sensor input, please notice the following when using MIPI Camera Sensor:

- Preferred use MIPI_ RX (MIPI PHY0) to connect MIPI Camera module.
- When using Dual MIPI LCM, using MIPI_TX_RX (MIPI PHY1) to connect MIPI Camera module is available.
- If MIPI Lanes of Sensor number≥ MIPI Lanes number supported by PHY, this sensor can be connected to corresponding MIPI PHY, but the number of Lanes used actually is based on the number of Lanes that PHY actually support.

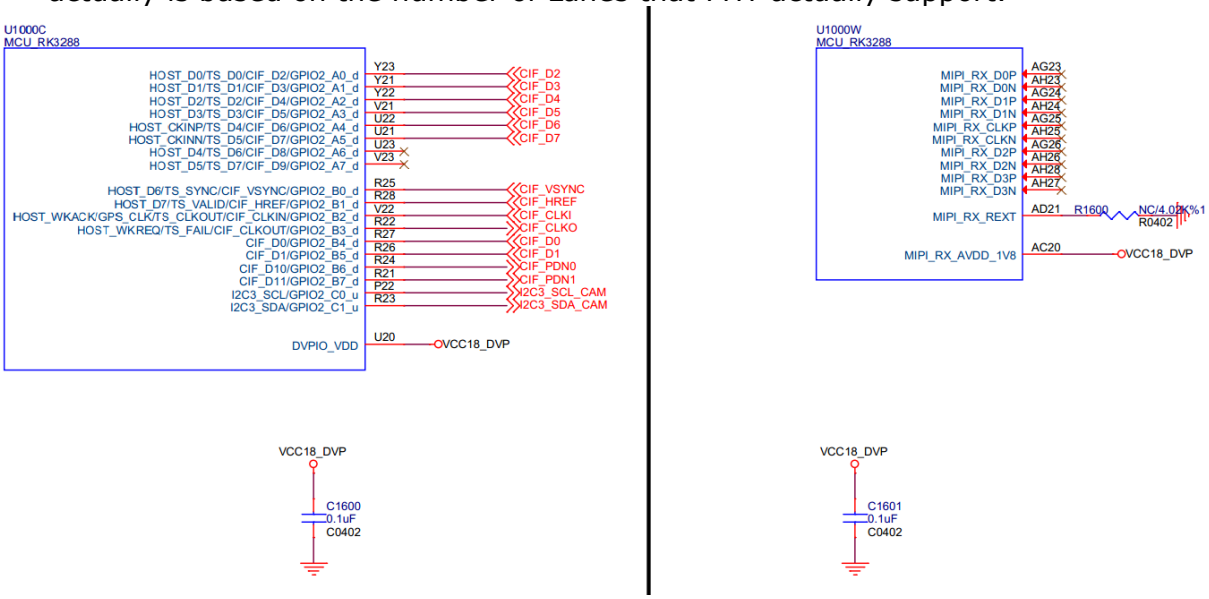


Figure 13-3

Tips:

- **MIPI 1Lane and 2Lane mode directly influence the preview fps of Camera and the speed of taking photos.**
- **Refer to the identification list *RK_Camera_Verification_List.xlsx* in advance, to affirm whether the debug has been passed when using MIPI Camera Sensor.**

13.2 PCB Layout

The following is the notices of DVP PCB Layout:

- Place MIPI Sensor connection close to the chip as much as possible to shorten the trace distances.
- The MIPI Sensor signal traces must strictly follow the requirements of differential pair rules, the skew of the two differential internal signals are controlled within 10mil and the skew between differential external signals are controlled within 30mil. Use arc or obtuse angle at the corners of traces as much as possible, right-angle or acute angle is unallowable, and the impedance requirement Z=100±10ohm.
- In order to suppress EMI, the MIPI Sensor signal traces is recommended to be placed in the inner layer and ensure that the reference plane is continuous and complete, otherwise, it will cause the discontinuous traces impedance and increase the external noise on them. If tracing on the PCB surface, please shield by GND traces.
- Try to reduce vias between different layers in layout, otherwise, that would cause the discontinuous trace impedance.
- The clock traces like MIPI_MCLK, CIF_CLKI, CIF_CLKO and so on are recommended to shield solely by GND traces avoiding other high ways.
- The data traces CIF_D2-D9 of DVP Sensor signals is recommended to shield by GND traces.

Chapter 14 Display Interface

14.1 Schematic

- RK3288 supports various video output modes like Parallel RGB, LVDS, MIPI, eDP, HDMI etc. The reference resistances of MIPI, LVDS, HDMI PHY please choose 1% accuracy and eDP is unnecessary to connect the external reference resistance, shown as Figure 14-1 to Figure 14-5.

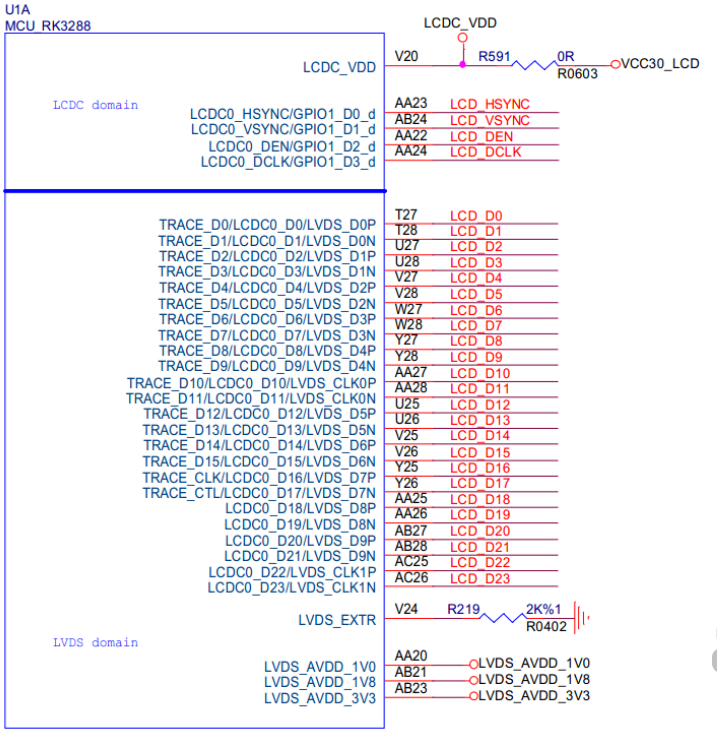


Figure 14-1

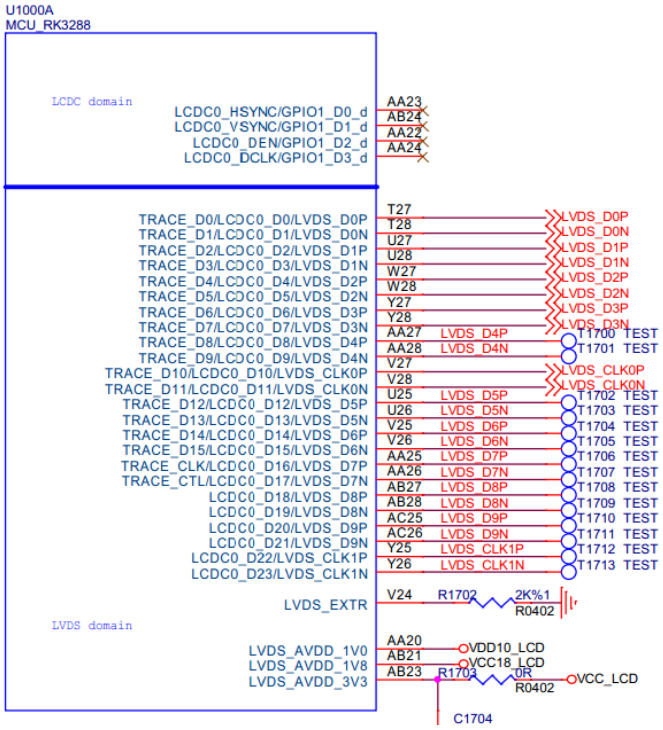


Figure 14-2

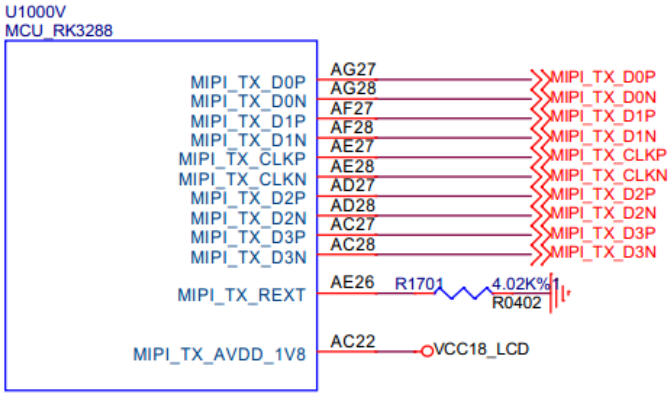


Figure 14-3

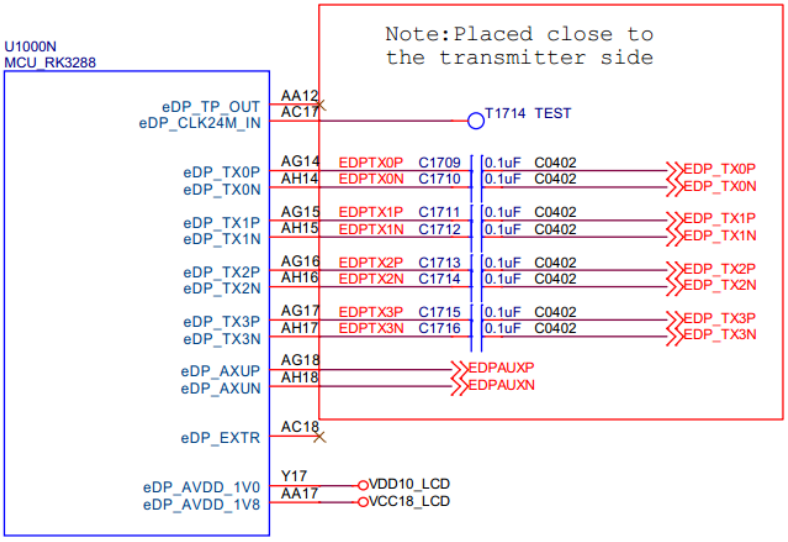


Figure 14-4

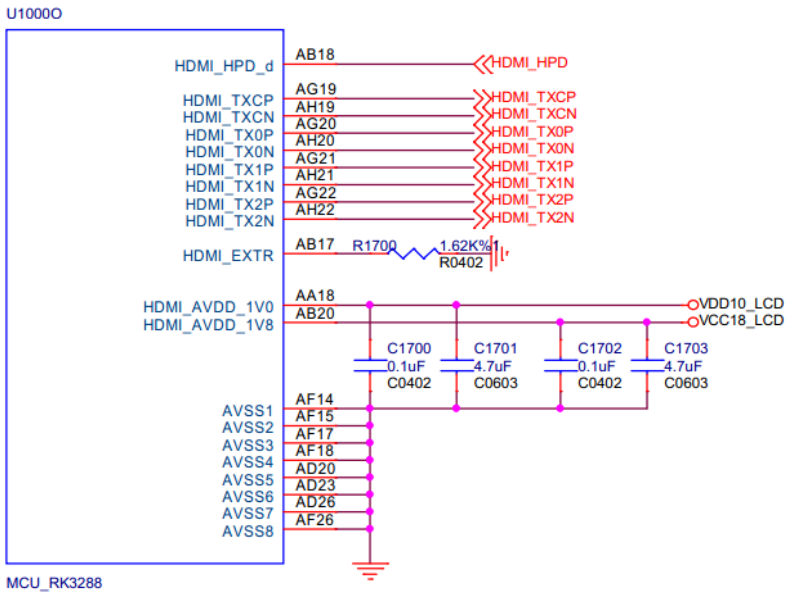


Figure 14-5

- MIPI_TX_AVDD_1V8 and MIPI_TX/RX_AVDD_1V8 are the power supply in the same group in the chip, so they must use the same power supply.
- When using LVDS and RGB functions, LVDS_AVDD_1V0, LVDS_AVDD_1V8 and LVDS_AVDD_3V3 are all requiring power supply, while the power supply is not needed when no using, shown as Figure 14-6.

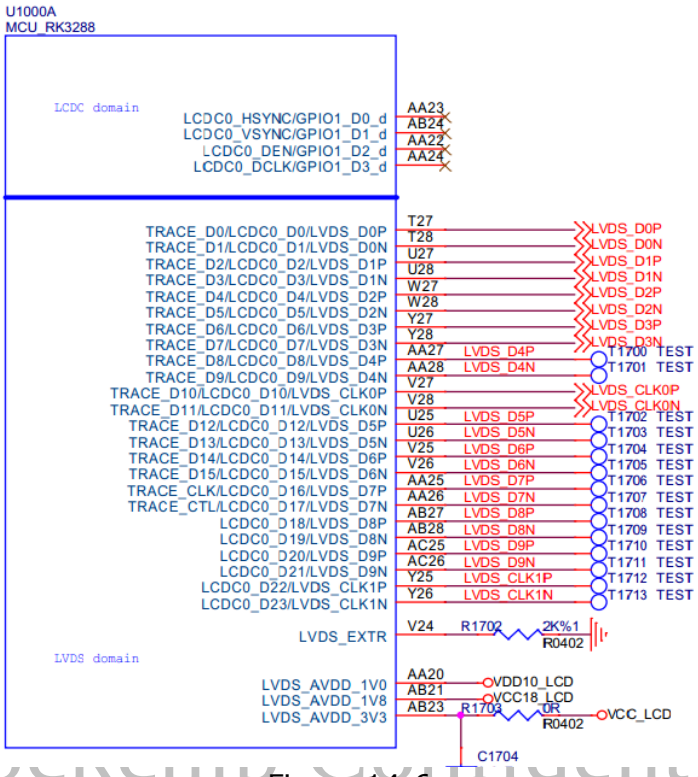


Figure 14-6

- In RK3288, place the power supply pins into each module in the display modules of independent power supply, and unavailable modules can break power supply to reduce the power dissipation, shown as Figure 14-7 and Figure 14-8.

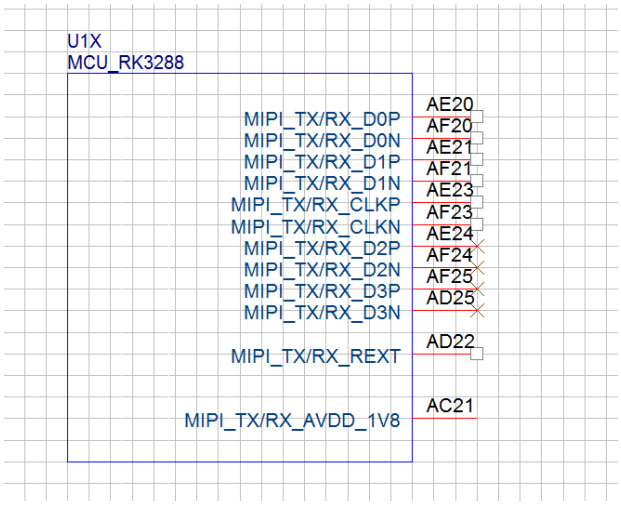


Figure 14-7

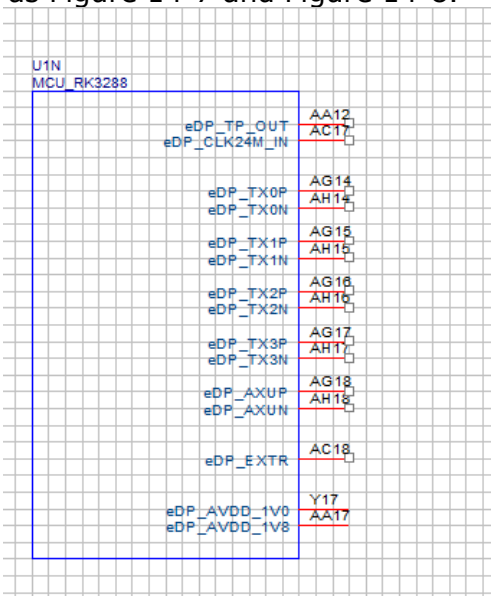


Figure 14-8

-

- Please ensure LCDC_VDD power supply work normally when designing, otherwise, the display would abnormal, shown as Pin V20 in the Figure 14-9.

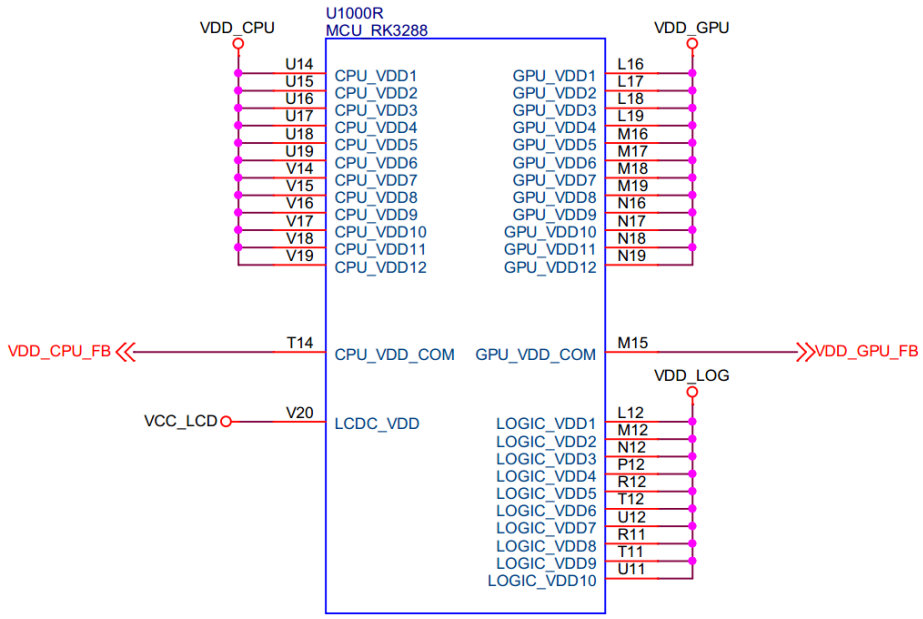


Figure 14-9

- Please place the power decoupling capacitors for each module close to the pins as much as possible, shown as Figure 14-10;

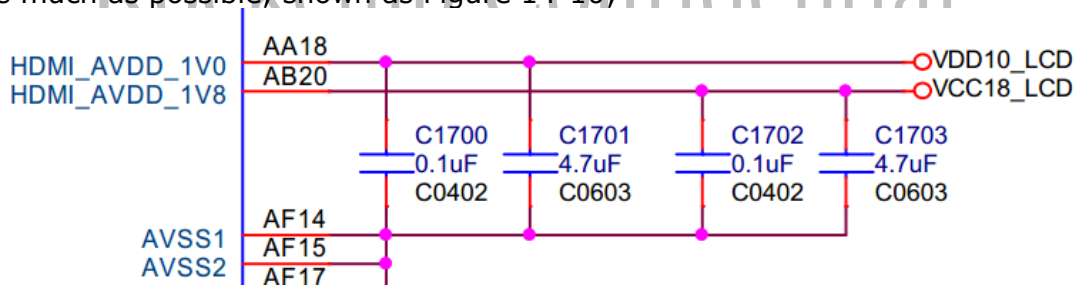


Figure 14-10

- The high-speed differential signals are very sensitive to the parasitic capacitance on the traces, thus, to choose the ESD protection device with low junction capacitance which should in compliance with requirements.

14.2 PCB Layout

- Place signal connector close to the chip as much as possible to shorten the trace distances.
- The signal traces of MIPI, eDP and HDMI must strictly follow the requirements of differential pair rules, the skew of the two differential internal signals are controlled within 10mil and the skew between differential external signals are controlled within 30mil. Use arc or obtuse angle at the corners of traces as much as possible, right-angle or acute angle is unallowable, and the impedance requirement Z=100±10ohm.
- The LVDS signal traces must strictly follow the requirements of differential pair rules, the skew of the two differential internal signals are controlled within 10mil and the skew between differential external signals are controlled within 30mil. Use arc or obtuse angle at the corners of traces as much as possible, right-angle or acute angle is unallowable, and the impedance requirement Z=100±10ohm.
- Try to control the total length of MIPI nets (including the length of PCB Layout, FPC cable and PCB receiving terminal) within 10inch, which the maximum had better no more than 15inch. Otherwise, the quality of signal on RK3288 board would be affected.
- Try to control the length of PCB Layout of eDP net within 10inch under the rate of 2.7Gbps in RK3288 board, and if demanding the signal of the rate of 5.4Gbps, the maximum trace length of PCB is recommended to be 5inch.
- Require the length of PCB Layout of HDMI net less than 5inch and had better within 3inch in RK3288 board. If the impedance continuity of the swap layer cannot be avoided, the impedance change is recommended to be controlled within 10% and place nearby GND vias in each differential pair of the swap layer to swap layer of signal reflow.

- In order to suppress EMI, the high-speed signal traces like eDP, MIPI, HDMI is recommended to be placed in the inner layer and ensure that the reference plane is continuous and complete, otherwise, it will cause the discontinuous trace impedance and increase the external noise on them. If tracing on the PCB surface, please shield by GND traces.
- Try to reduce vias between different layers in high-speed signal layout like eDP, MIPI, HDMI, otherwise, that would cause the discontinuous trace impedance.

- Place ESD devices close to HDMI outlet, shown as Figure 14-11;

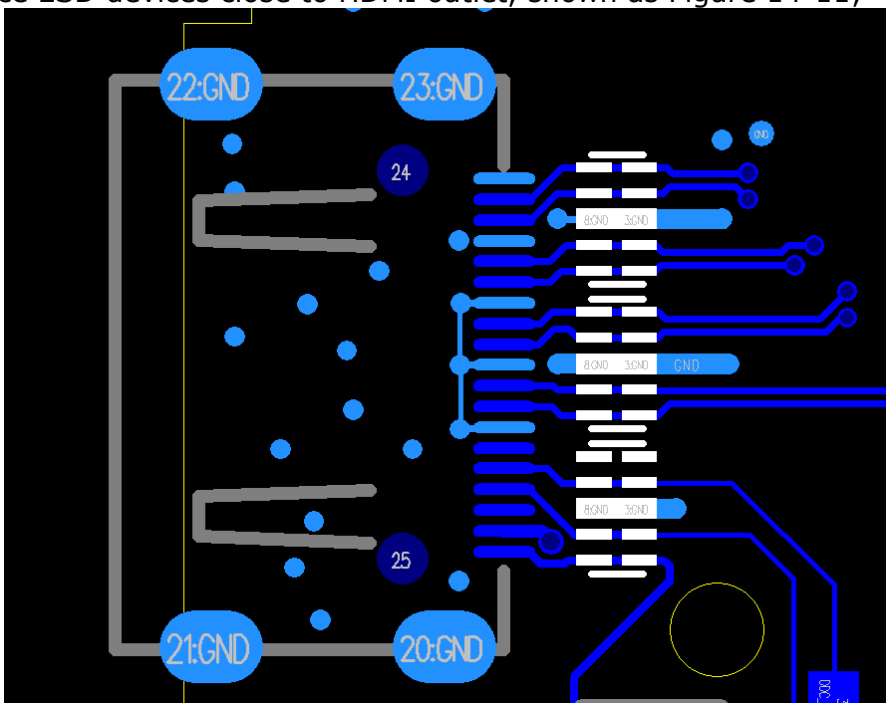


Figure 14-11

- The output coupling capacitors of eDP data channels should close to the chip terminal, shown as Figure 14-2;

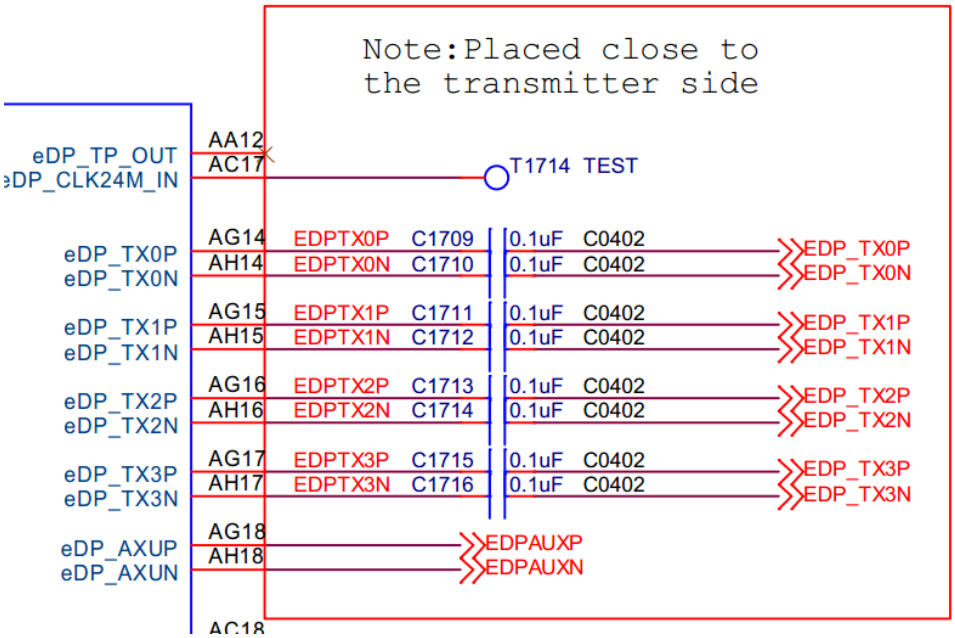


Figure 14-12

Chapter 15 LCM

15.1 Schematic

The power dissipation of eDP screen is high, please choose backlight driver IC of high-current, shown as Figure 15-1.
Using the power supply solution of dual-section battery and mount R5002 when adopting 9.7-inch screen; Using single-section battery and mount R5003 when 7.85-inch screen.

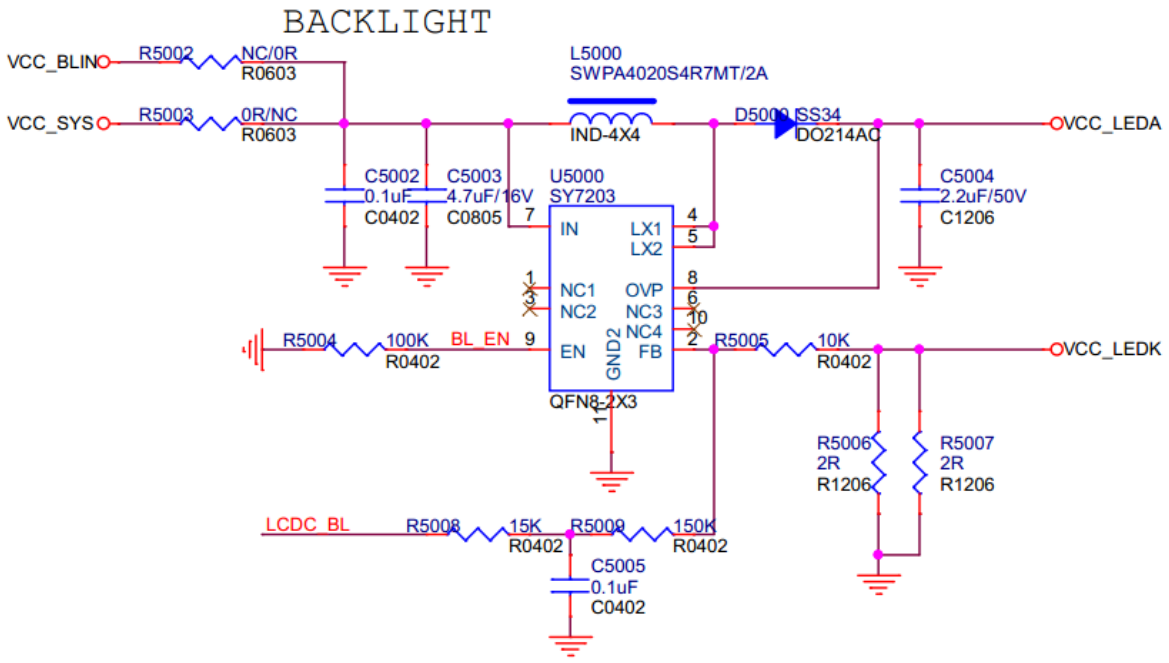


Figure 15-1

eDP screen AUXN, the pull-up/down resistance of AUXP auxiliary channel R5000, R5001 and the coupling capacitor C5000, C5001 should be placed close to screen socket, shown as Figure 15-2.

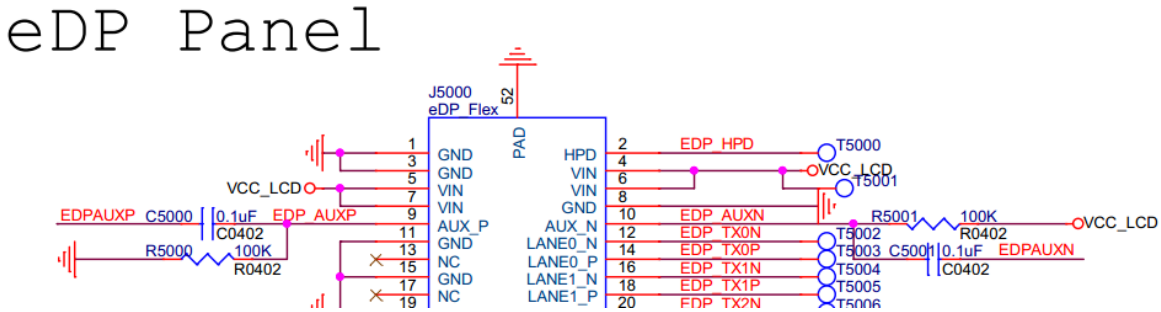


Figure 15-2

Please connect to MIPI_TX channel when using single MIPI screen, and MIPI_TX/RX cannot as default output channel.

Please do not connect the traces reversely when using double screen that MIPI_TX is Left channel and MIPI_TX/RX is Right channel, shown as Figure15-4 and Figure 15-4. If the channel of MIPI screen can be used interchangeably, then this problem is not present, please refer to datasheet of screen.

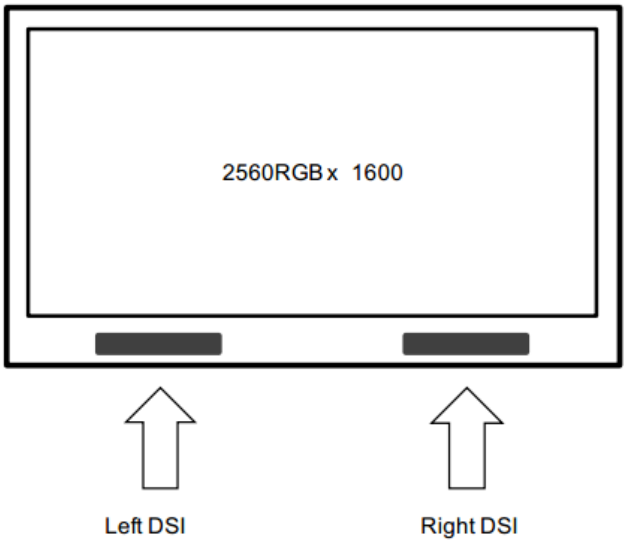


Figure 15-3

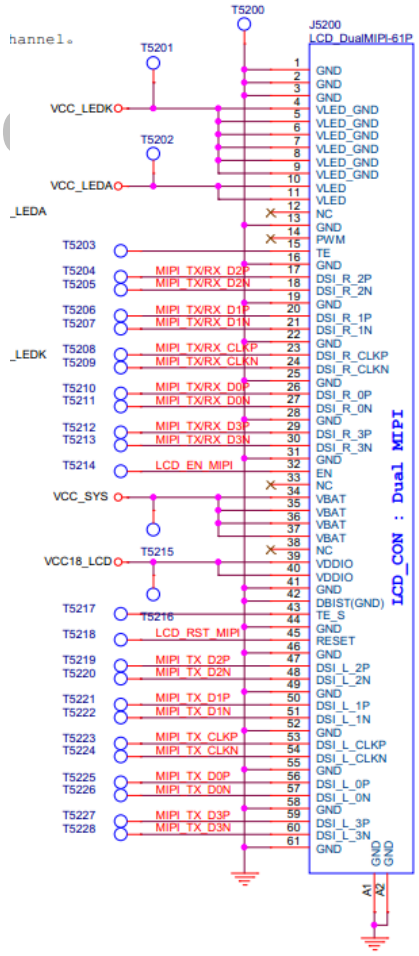


Figure 15-4

When using single LVDS screen, please connect to the low bit output of LVDS channel, which is LVDS_D0~D4, shown as Figure 15-5.
When using double LVDS screen, please connect low bit output of LVDS channel to the odd signal of LVDS and high bit to the even signal, shown as Figure 15-5.

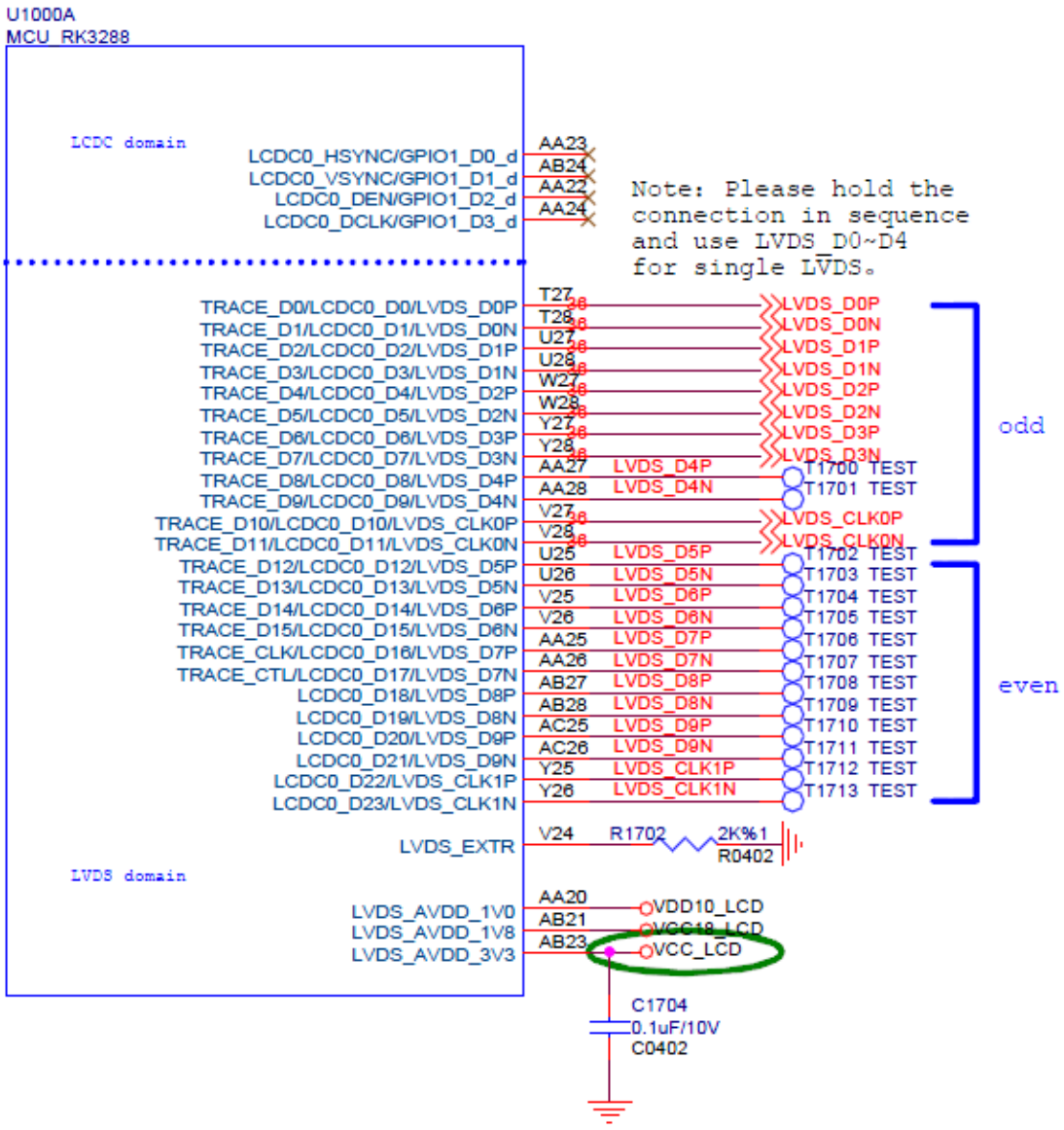


Figure 15-5

The drive circuits of MIPI and LVDS screen reserve CABC control circuit, shown as Figure 15-6. If CABC function is not used, resistance R5107, R5108, R5109, R5110 and the inverter U5101 is not mounted. The backlight voltage regulator circuit shown as Figure 15-7 is controlled by SOC through PWM, the higher the duty cycle of PWM, the lower the brightness of screen. When using CABC function, R5107, R5108 are mounted by 0R resistance, while whether mounting the inverter U5101 and resistances R5109 and R5110 according to the scale of screen.

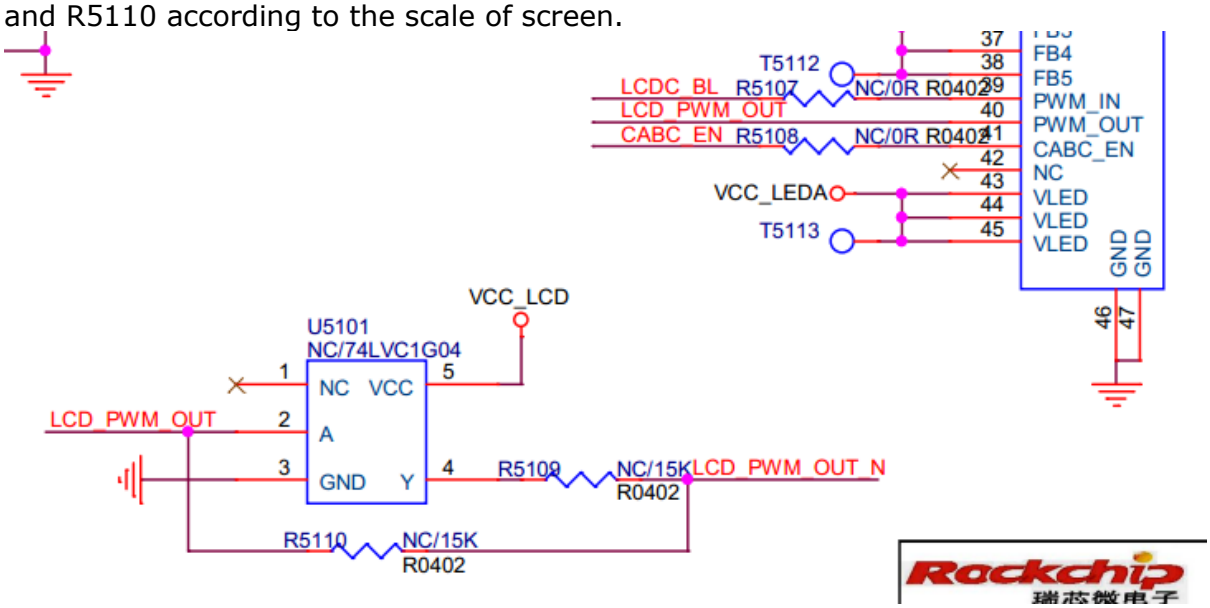


Figure 15-6

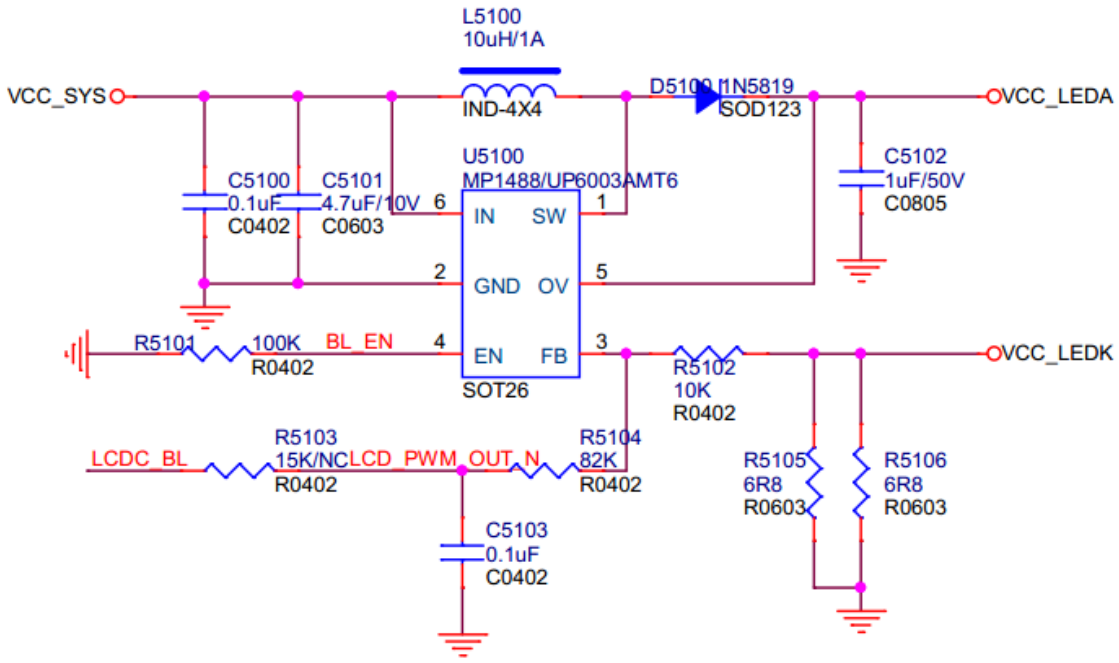


Figure 15-7

Please keep IO level match with the chip when designing LCM interface, double MIPI screen VDDIO shown as Figure 15-8 is 1.8V power supply, then the signal of LCD_EN and LCD_RST should be voltage divided.

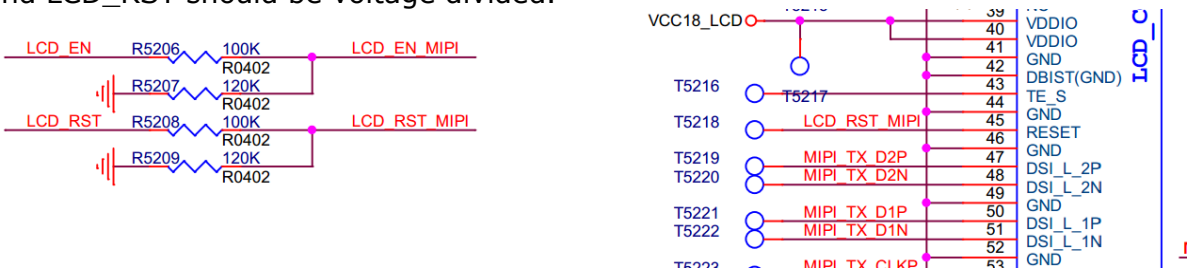


Figure 15-8

15.2 PCB Layout

High-speed signal layout please refer to the design requirements of PCB Layout in 12th chapter. Backlight current-limiting resistance R5006, R5007 and power supply capacitor C5004 should be placed close to screen socket, show as Figure 15-9 and Figure 15-10.

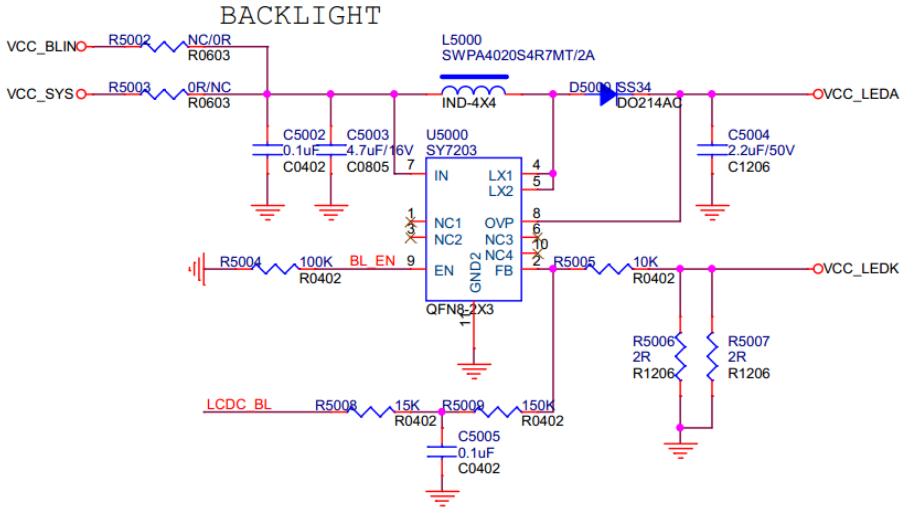


Figure 15-9

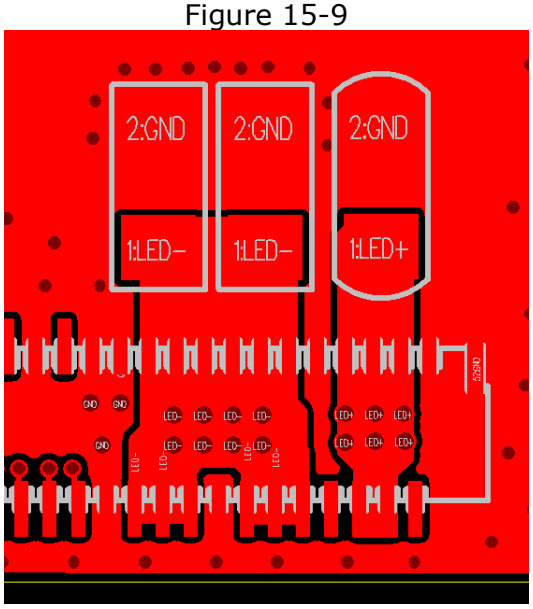


Figure 15-10

Chapter 16 Debug

16.1 Schematic

For convenience to debug the software on line, RK3288 specifically reserves an Uart interface (UART2) as Debug; In the practical product application, it is not recommended to use it in other way, and to design as Figure 16-1 can be easy to debug the product.

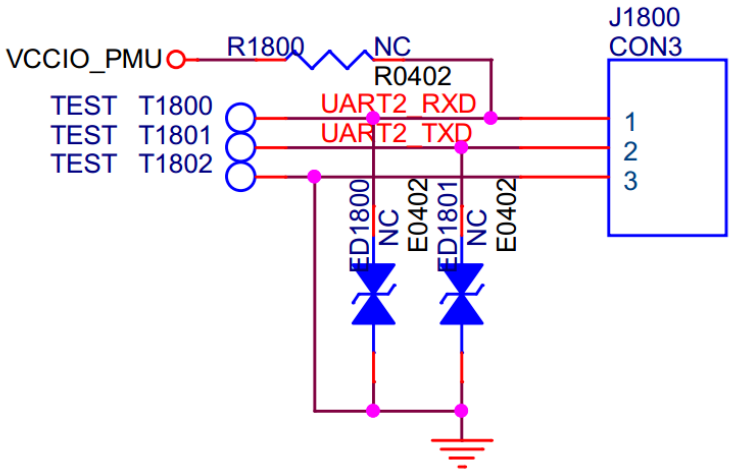


Figure 16-1

If using RS232 level conversion chip, please notice the direction of TXD and RXD.

16.2 PCB Layout

If using Debug function frequently (such as development board, SDK etc.), it is recommended to add ESD devices in the interface to protect the chip;

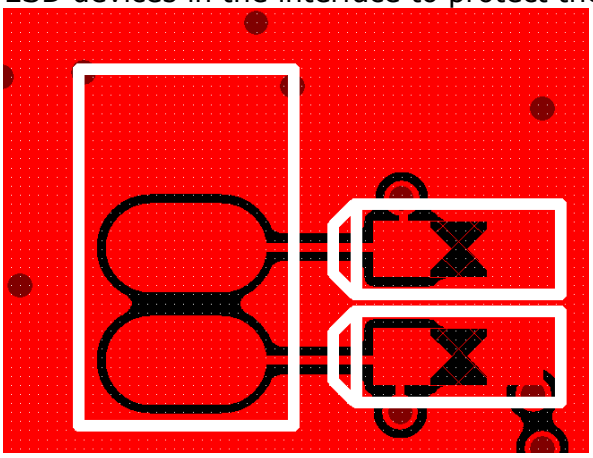


Figure 16-2

Chapter 17 Audio Codec & SPDIF

17.1 Schematic

CODEC I2S interface power domain is APIO4_VDD power supply, and in the actual product designs, according to the actual demands of IO power of Codec (1.8V or 2.8V) , choosing the corresponding power supply, meanwhile the I2C pull-up level must be correspondence with it, otherwise, the Codec would work abnormally or incapably, shown as Figure 17-1 and Figure 17-2.

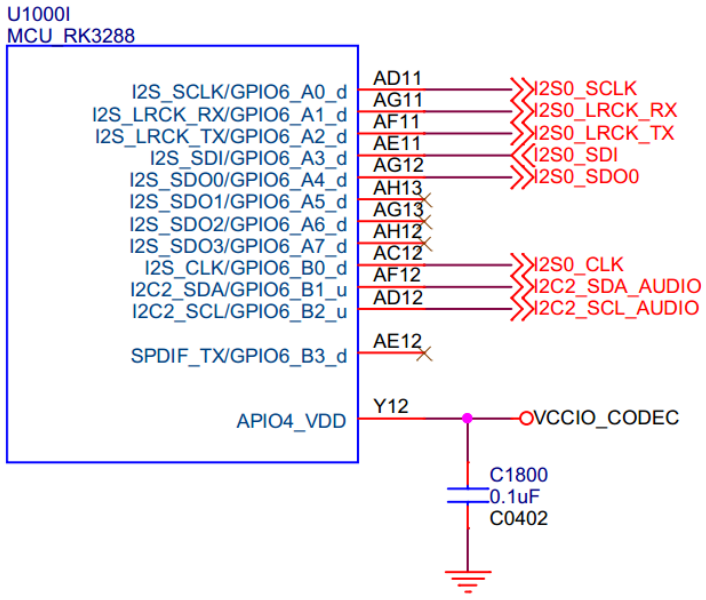


Figure 17-1

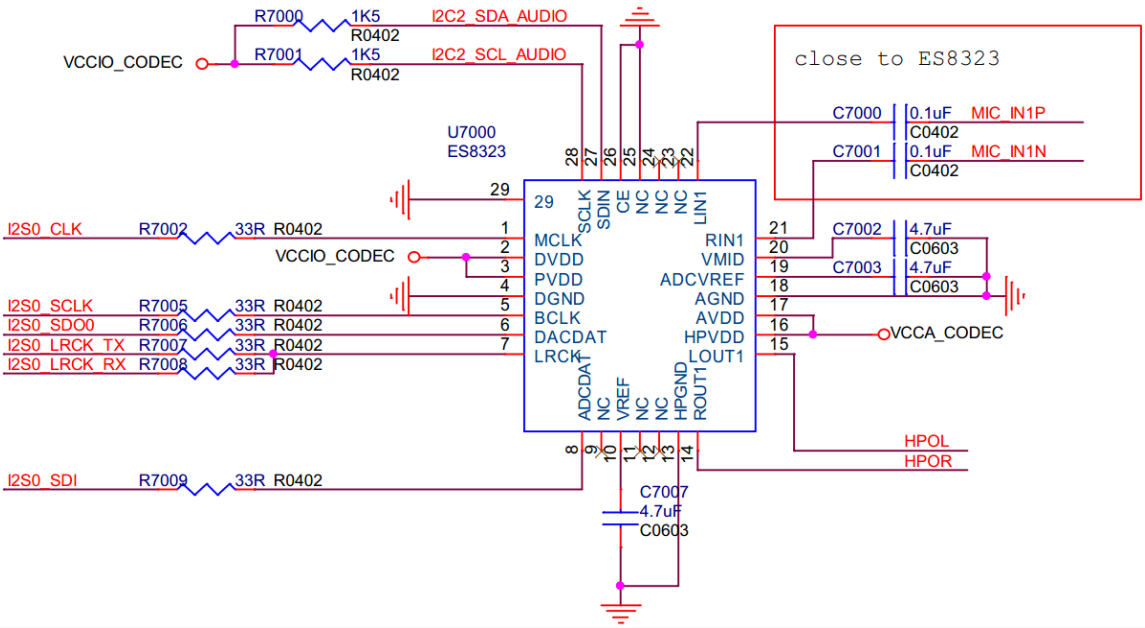


Figure 17-2

Please choose the appropriate MIC divider resistance R7010, R7016 according to electret microphone, shown as Figure 17-3.

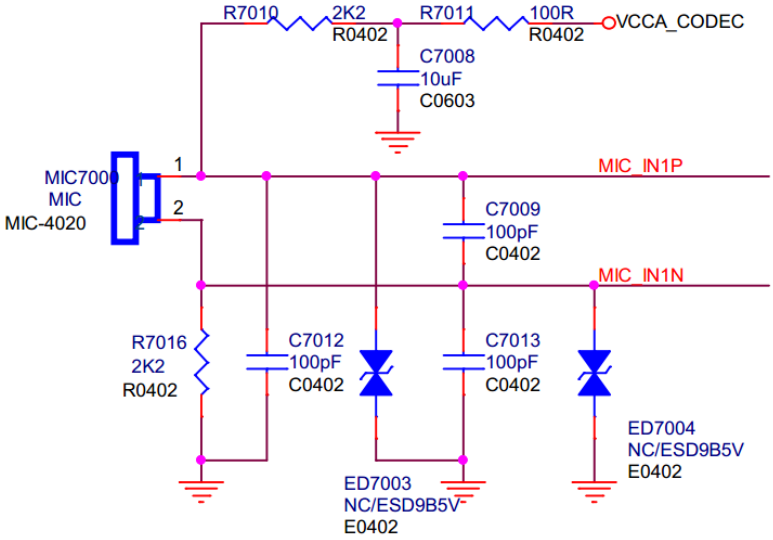


Figure 17-3

If using the output of capacitor coupling, 100uF capacitance can ensure the flatness of frequency response curve in the ideal situation, and if choosing smaller coupling capacitance wanted to reduce the cost would cause the deviation of low frequency, shown as EC7000, EC7001 in Figure 15-4;

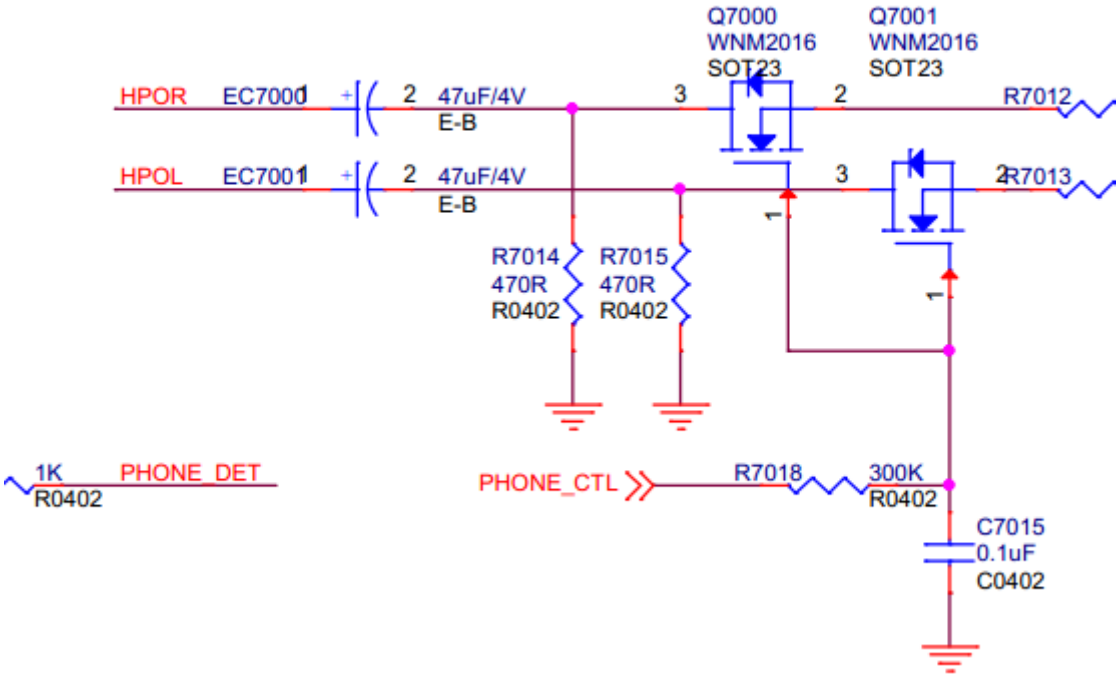


Figure 17-4

17.2 PCB Layout

- The width of power supply trace of Codec should over 15mils, and the width of VCC_SPK trace should over 30mils.
- Each IN/OUT signal of Codec, including HP OUT, LINE IN, LINE OUT, MIC IN, SPDIF, Speaker OUT and so on, are needed to shield by GND traces (shielding by GND traces includes in the same and adjacent layer) to avoid the crosstalk between signals to distorted and noise, and to isolated with other digital signals.
- The width of HP OUT trace is recommended to over 15mils.
- The width of LINE IN/OUT trace is recommended to over 10mils.
- MIC input signal is sensitive, the coupling capacitance of MIC should be placed close to Codec to avoid the noise, shown as Figure 17-5.

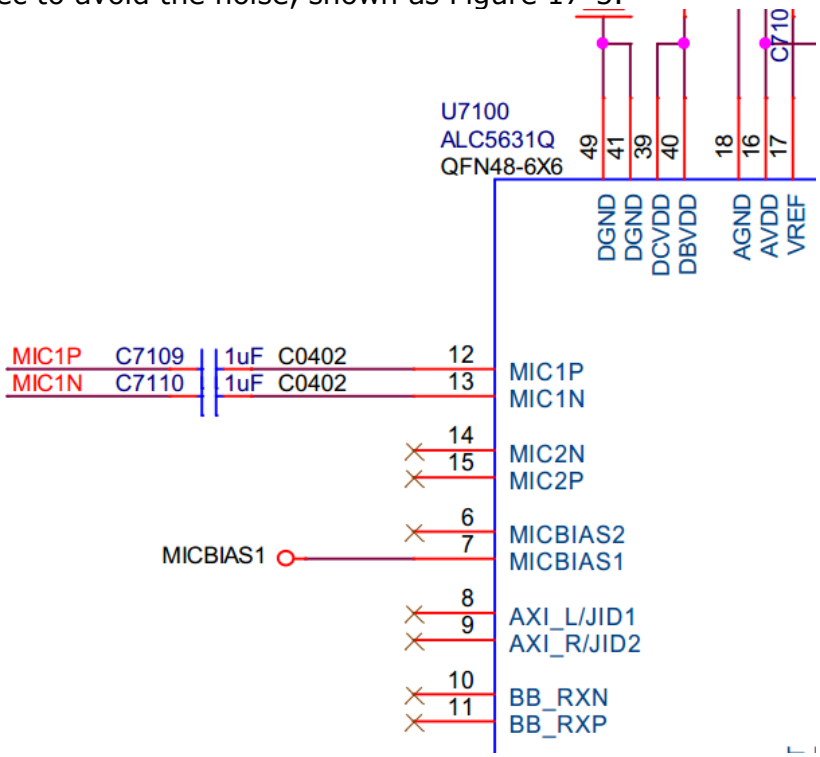


Figure 17-5

- Try to place Codec close to connecting in Layout, and the traces should be as short as possible.
- In order to suppress EMI, the traces of power amplifier to the loudspeaker need to be shorten, thicken and reduce the bend. To avoid the noise disturb, it is recommended to trace by differential pairs, the width of traces should larger than 20mils, the distance between traces should be smaller than 10mils, and to reserve LC filter nearby loudspeaker output.

Chapter 18 Touch Panel

18.1 Schematic

The pull-up resistance of Touch Panel I2C please connect to TP power supply VCC_TP to avoid leakage to TP screen through I2C bus so as to add extra power consumption in the case of dormancy.

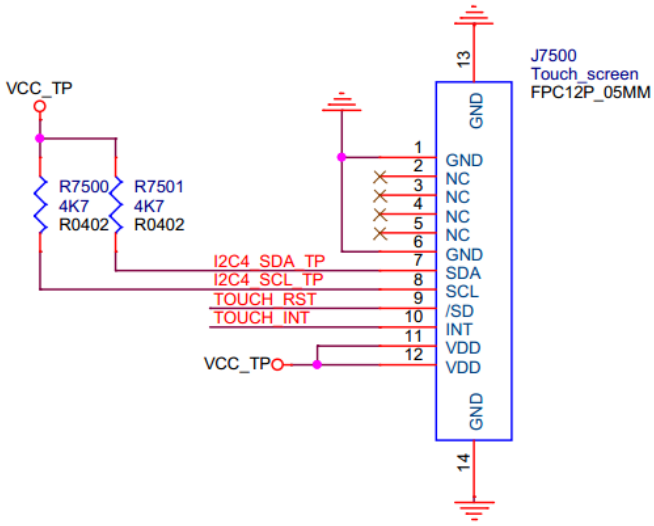


Figure 18-1

Charge Pump capacitor of TP IC should pay attention to the withstand voltage, shown as Figure 18-2, and is placed close to the chip pins.

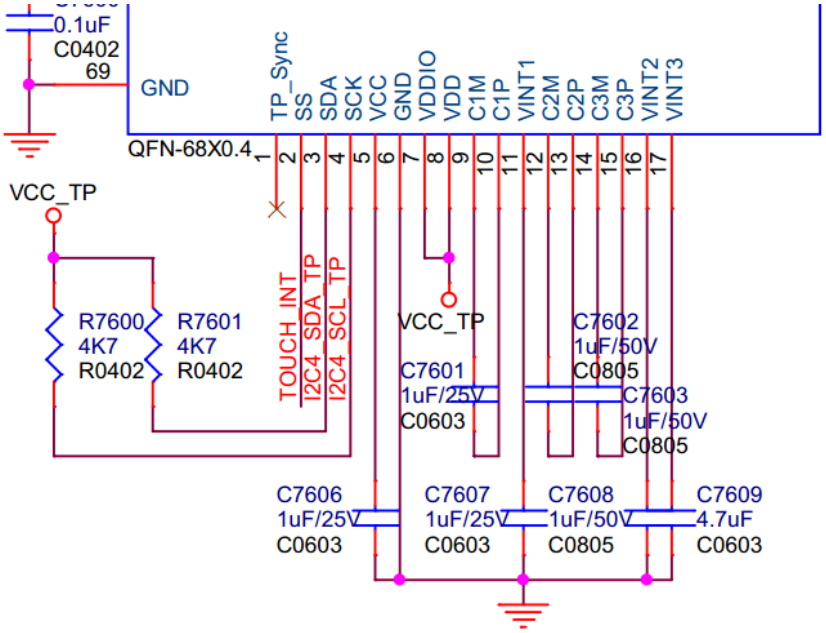


Figure 18-2

18.2 PCB Layout

ESD of big screen is easy to damage the data lines of SOC interface, and please note to protect the sensor signal lines .
The clearance between Sensor and Driver signals should be isolated by GND traces in the design of TP onboard.

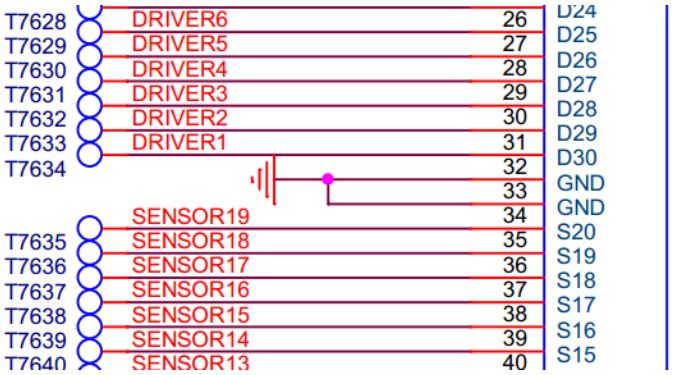


Figure 18-3

Chapter 19 Sensor

19.1 Schematic

VCC Supply of Sensor may be different from the power domain of VCCIO Supply. Please make sure the I2C1 signals are pulled-up to the power supply which is consistent with VCC Supply of Sensor, otherwise, the signal level needs to be matched.

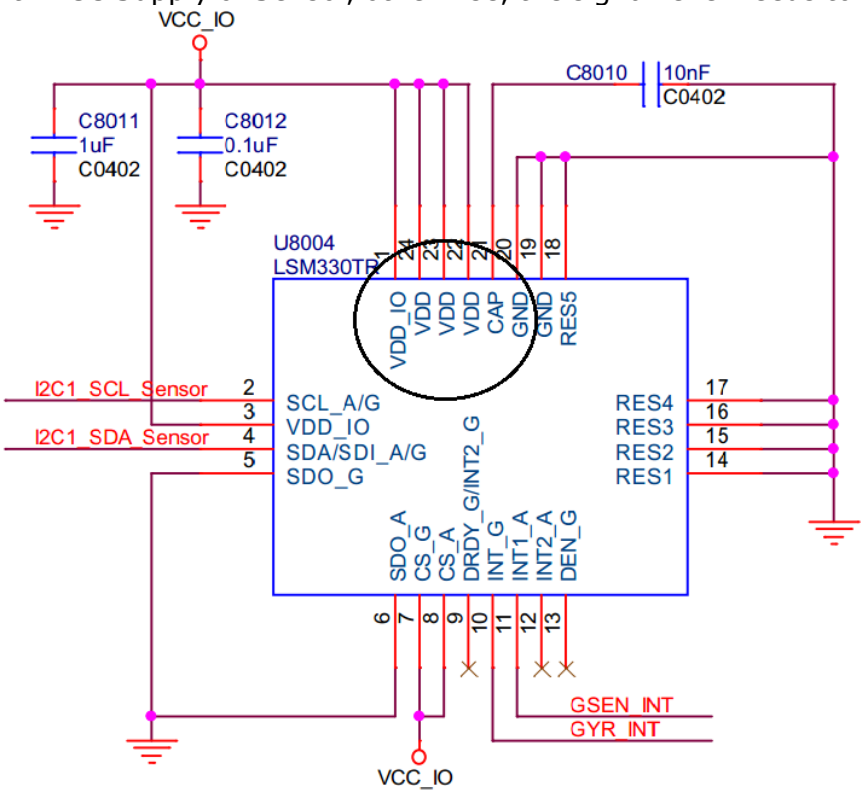


Figure 19-1

Hall Sensor has single-pole and omnipolar, choosing the appropriate model of device as needed.

The optical sensor can adjust the time of respond through the adjustment of the resistance value of R8000 in Figure 19-2, please refer to the device specification.

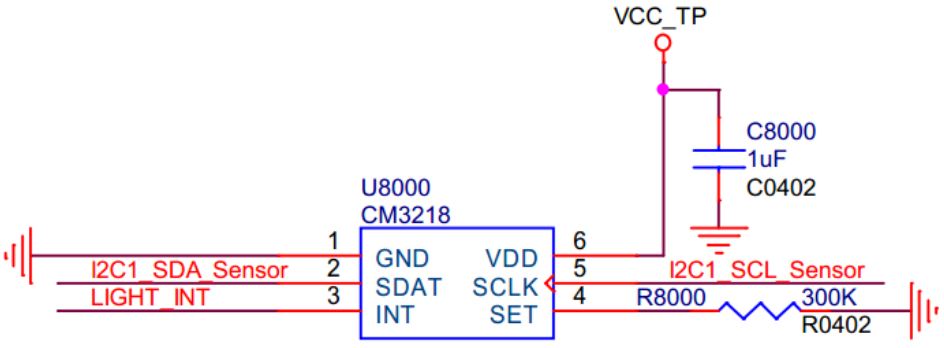


Figure 19-2

The motor is the inductive device that must add diode and please notice the direction of diode.

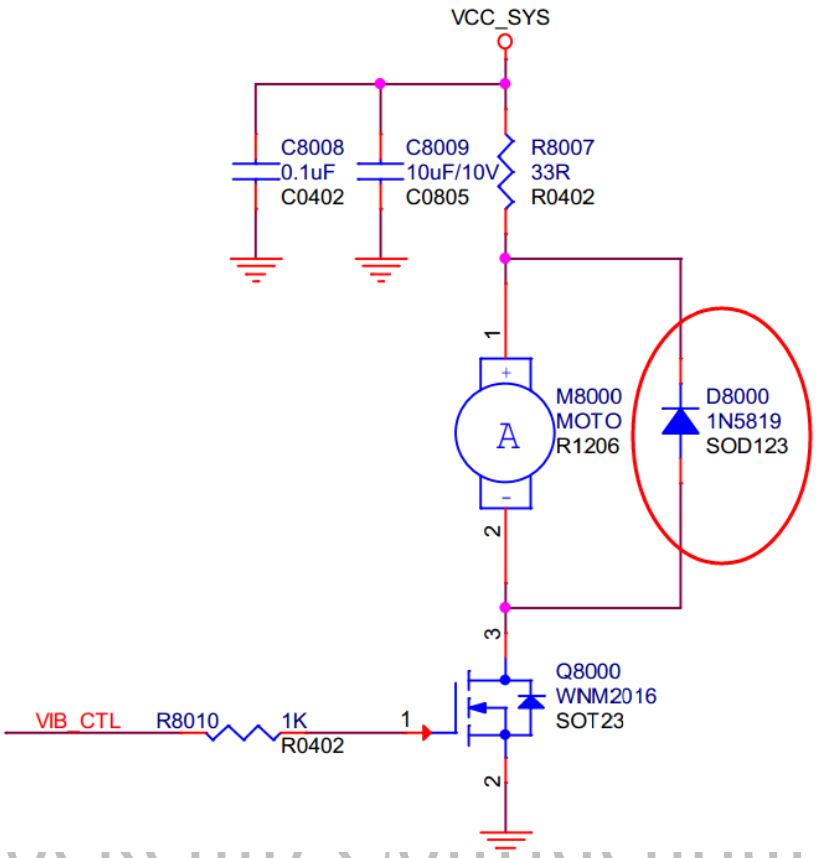


Figure 19-3

G-Sensor is compatible with LIS3DH, MMA8452Q and LSM303D and mounting according to the needs to meet the requirements of different compatibility.

I303D with 3D Gsensor and E-compass

	LIS3DH	MMA8452Q	LSM303D
C8004	NC	NC	4.7uF
R8003	0ohm	NC	NC
R8001	NC	0ohm	NC
C8001	NC	0.1uF	0.22uF
R8002	NC	NC	0R
R8004	NC	NC	0R

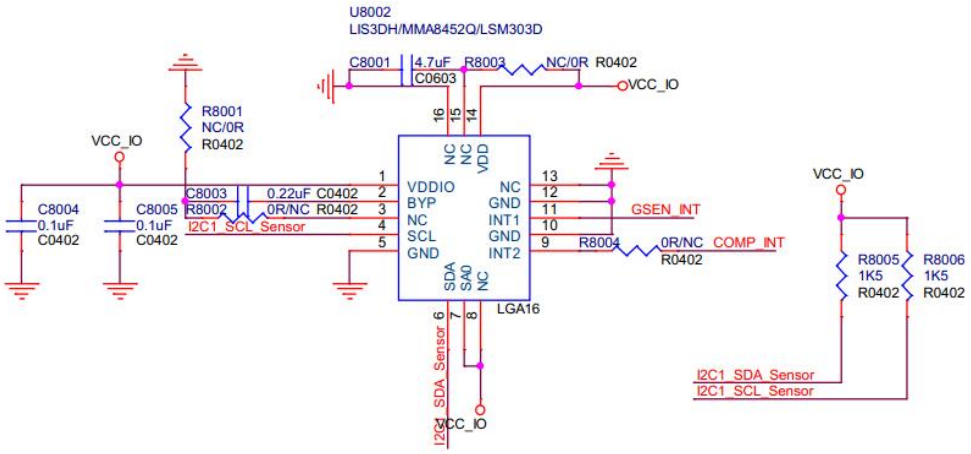


Figure 19-4

19.2 PCB Layout

- When the optical sensor is in Layout, the user experience must be considered. It is recommended to place nearby the front-facing camera, and try not to place other luminophor around the sensor, shown as Figure 19-5.

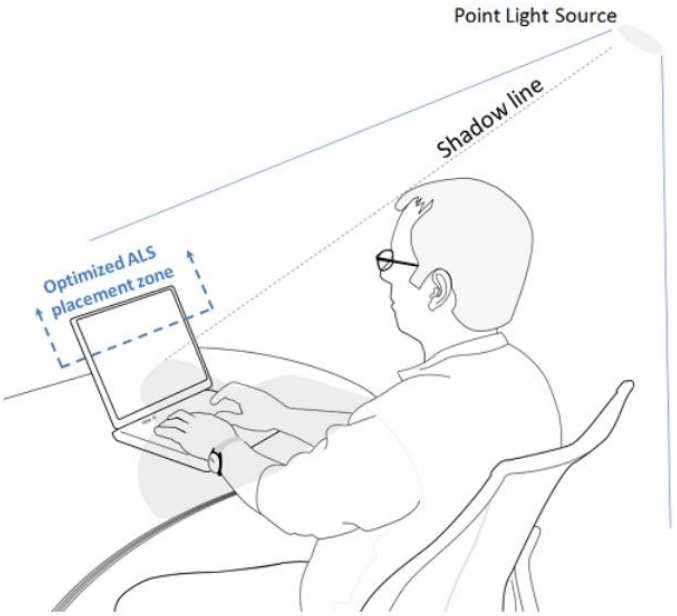


Figure 19-5

- The illumination value receiving from the surface of optical sensor depends on the size of silk screen hole and the ink luminousness, and the incidence angle should larger than ±30 degree, shown as Figure 19-6, and the specific calculation formula and the reference value please refer to *Capella_ALS Structure Design Guide.*

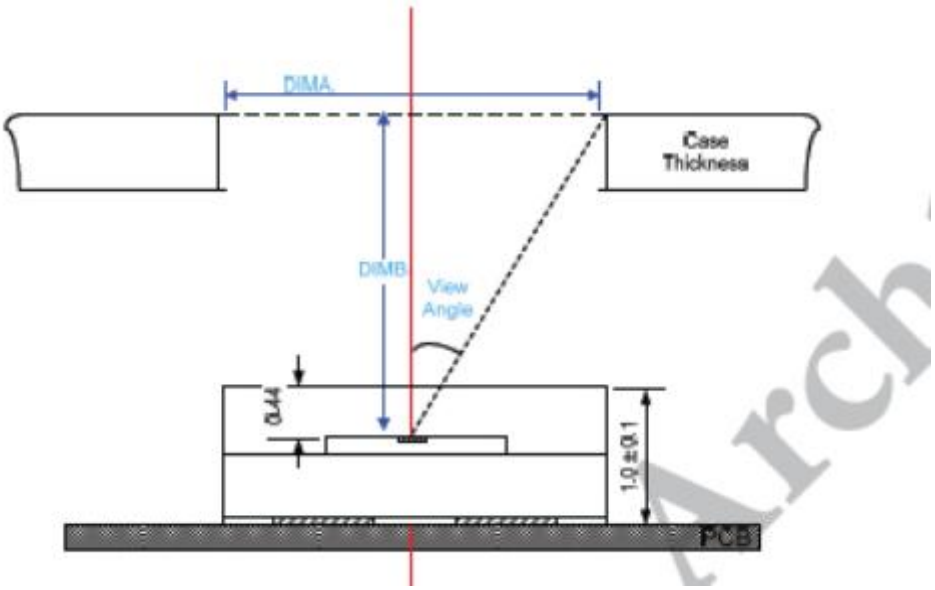


Figure 19-6

- Geomagnetic sensor and hall sensor in Layout should keep away from high magnetic fields, easy magnetization devices, and high-current devices and so on, such as receiver, loudspeaker, motor, camera, high-current inductance etc. Meanwhile they cannot be placed in shielding case.
- Notice the direction of G-Sensor in Layout, and the first pin is recommended to be placed on the top left corner of the product front view, and try to keep consistent with SDK to the debug.

Chapter 20 eFUSE

20.1 Schematic

If the customer need to programme the embedded eFUSE, the eFUSE power supply circuit needs to be added, shown as Figure 20-1. If not, this part of circuit can be deleted.
It is recommended the customer to reserve the test point in PCBA, and finish eFUSE programmer according to the power supply circuits reserved by fixture to reduce the cost.

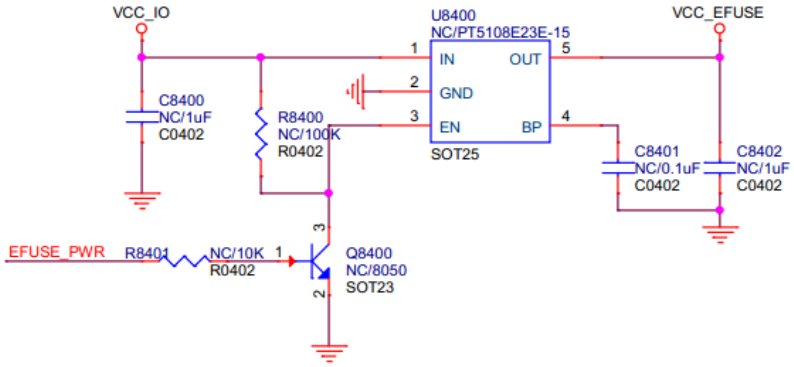


Figure 20-1

Chapter 21 MAC

21.1 Schematic

The Ethernet and FLASH1 are multiplexed together with RK3288, therefore if the Ethernet is needed, FLASH1 channel cannot be used.
MAC of RK3288 support RMII interface and RGMII interface. Figure 21-1 is RGMII, and Figure 21-2 is RMII.

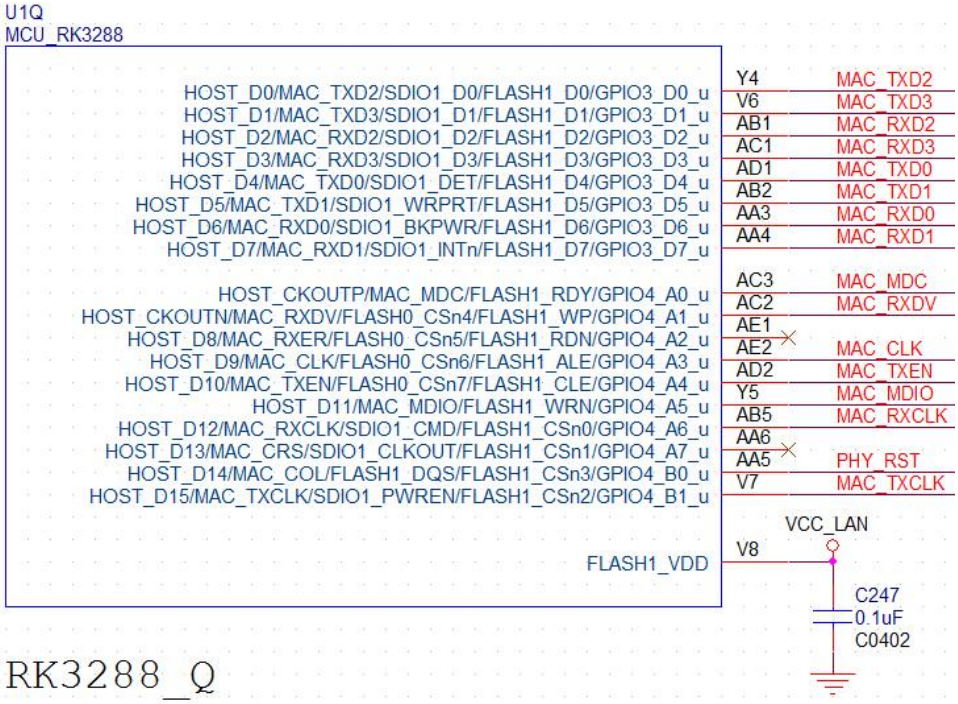


Figure 21-1

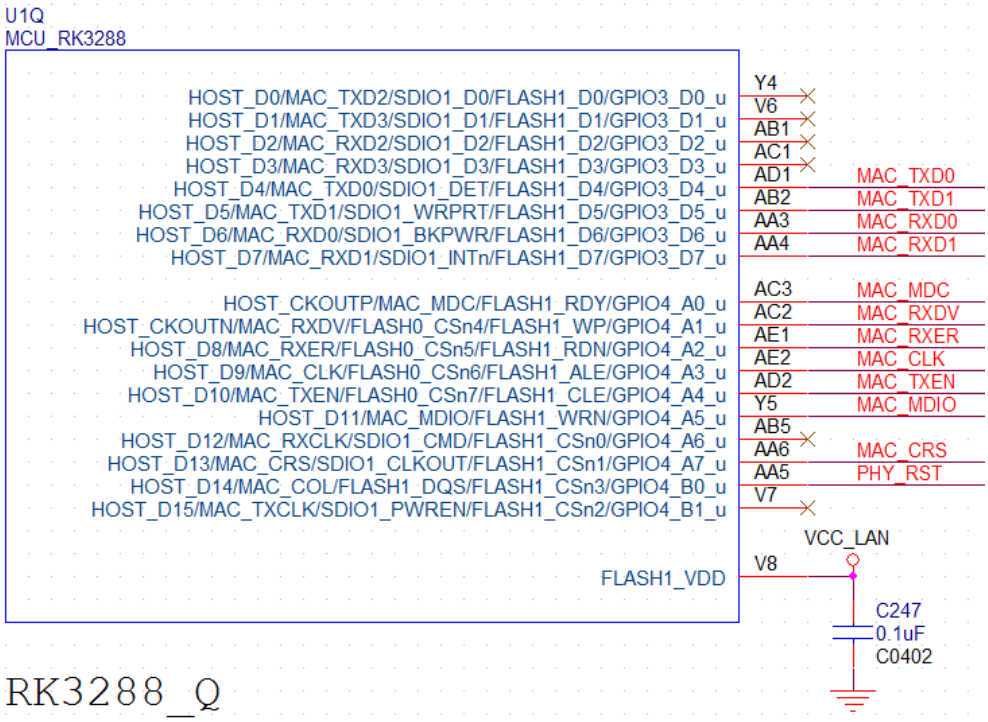


Figure 21-2

The value of load capacitors (C251, C252) of 25MHz crystal need to according to use nominal load-capacitance of crystal, and 12pF is chose by Rockchip as corresponding capacity value, not the universal value.

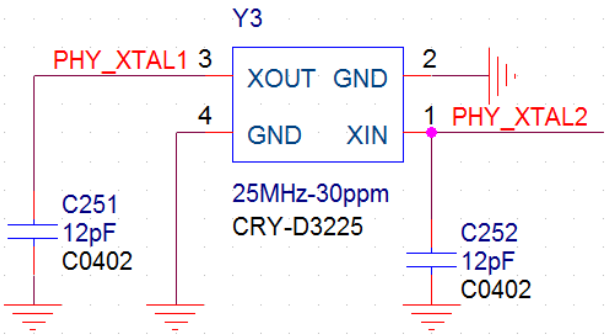


Figure 21-3

L9 inductance in Figure 21-4 should satisfy the following conditions: IDC>=600mA; Tolerance <= 20%; DCR <= 0.8ohms@1MHz; Measure Efficiency >= 75%@GbE link speed;

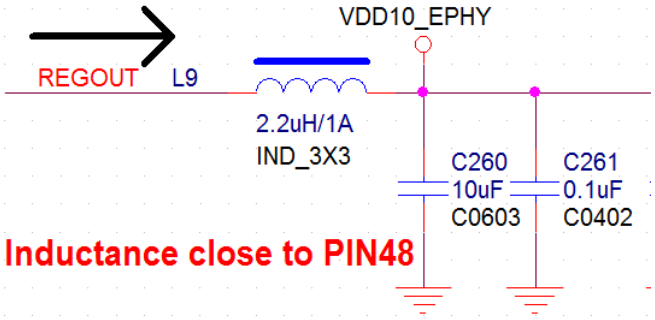


Figure 21-4

If want to pass the EMI test, 0R resistance of the differential signals should be changed into common mode choke (common mode choke is 90-120ohm).

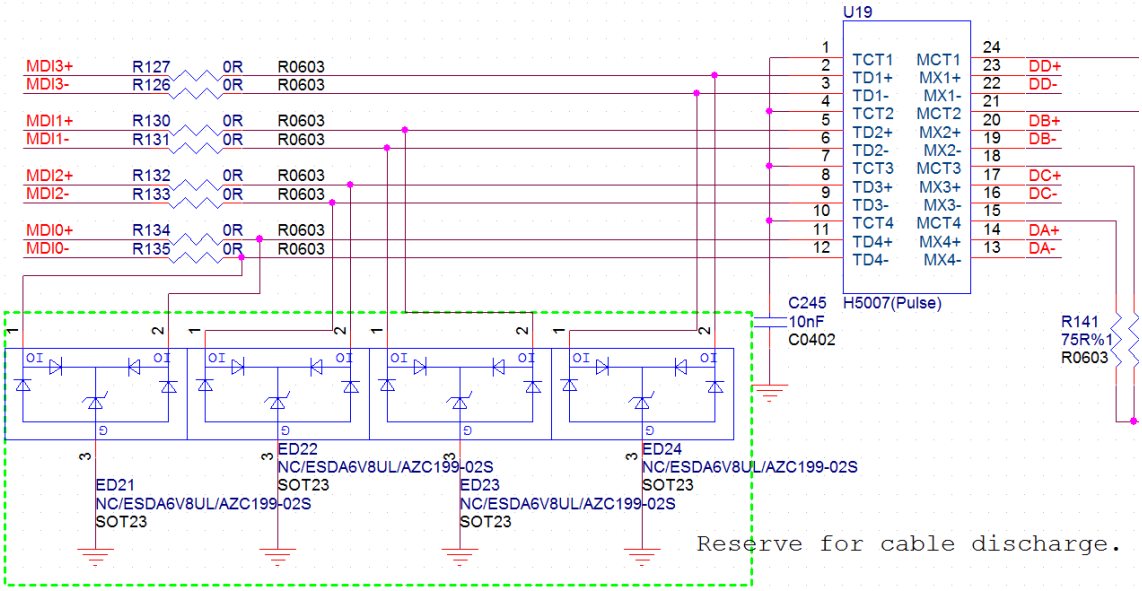


Figure 21-5

It is recommended to use RJ45 socket with metallic shield. If RJ45 has LED lights, then LED0-2 should reserve a 100pF capacitor to GND of to improve EMI, shown as Figure 21-6.

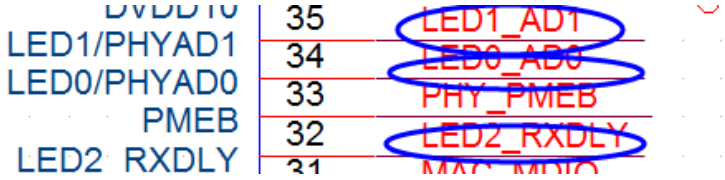


Figure 21-6

The ripple of 3.3V and 1.05V should less than 100mV. REST resistance must use 1% accuracy, shown as Figure 21-7.

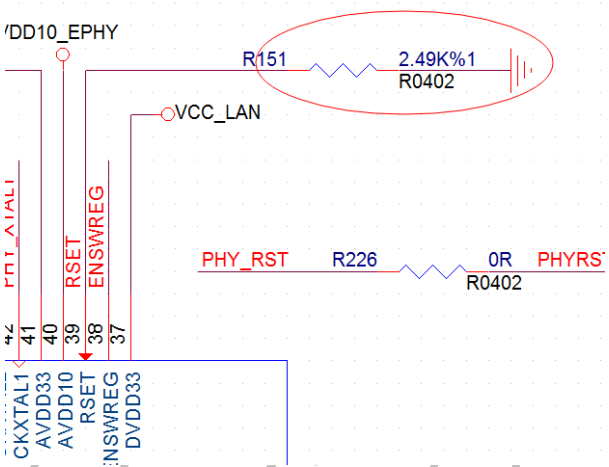


Figure 21-7

The network transformer should satisfy the conditions shown as Figure 21-8:

Turn Ratio TX/RX: 1:1

Primary Inductance: 350μH OCL with 8mA bias

Insertion Loss: -1.0 dB Max, 1 ~ 100MHz

Return Loss: -18dB Min @ 100Ω, 1 ~ 30MHz

-14dB Min @ 100Ω, 30 ~ 60MHz

-12dB Min @ 100Ω, 60 ~ 80MHz

Differential to Common Mode Rejection:

-40dB Min @ 1 ~ 60MHz

-30dB Min @ 60 ~ 100MHz

Hi-Pot: 1500Vrms @ 60sec

Operating Temperature: 0°C to 70°C

Recommended Magnetics: Pulse H5007 or similar

Figure 21-8

21.2 PCB Layout

Layout should obey the following rules:

- The more PHY close to RK3288, the better EMI could make, which RGMII signals traces should be as short as possible which must less than 15cm.
- RJ45 had better be placed close to PHY, which means MDI signals traces should be as short as possible which must less than 12cm, shown as Figure 21-9.

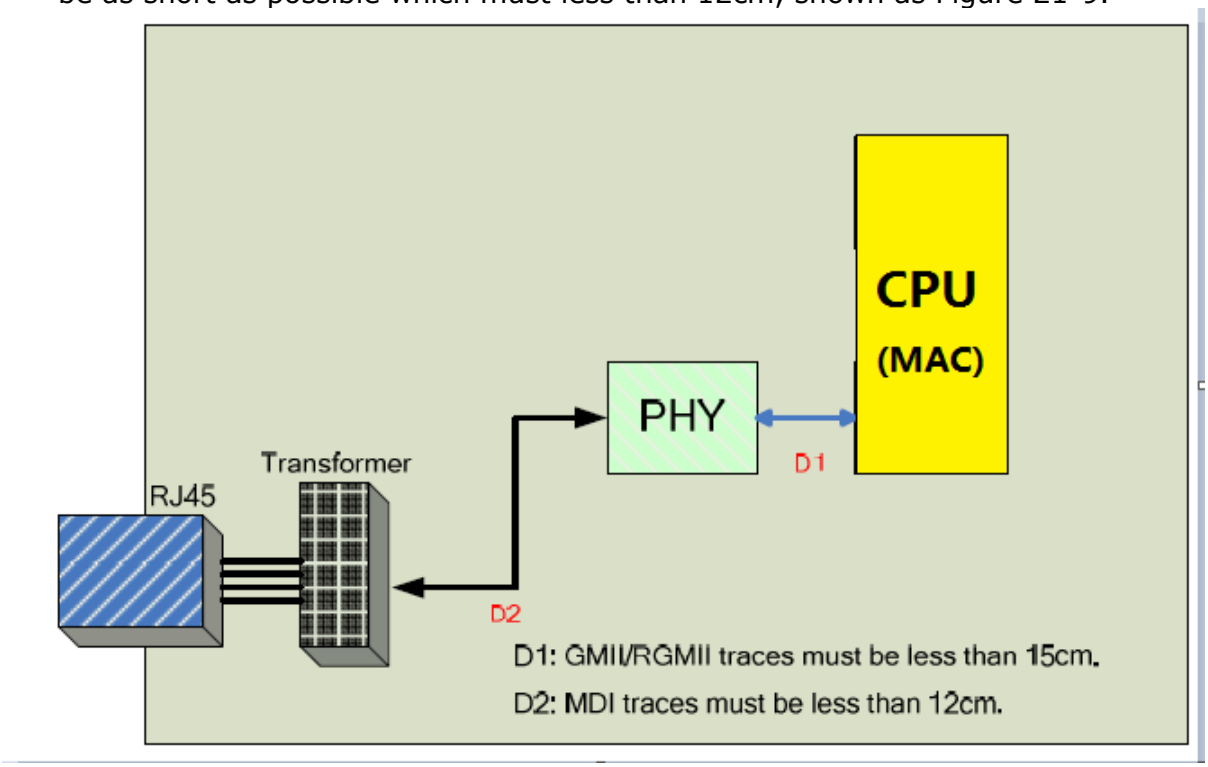


Figure 21-9

- If RJ45 and the transformer are separated, then 10/100/1000M network transformer should be placed close to RJ45, if having other transformers nearby, they had better keep far away from it and be placed at 90 degree.
- Four pairs of differential signals of MDI should be controlled length, the skew of the two differential internal signals are controlled within 10mil and the skew between differential external signals are controlled within 30mil. Use arc or obtuse angle at the corners of traces as much as possible, right-angle or acute angle is unallowable, and the impedance requirement Z=100±10ohm. The traces try to be as short as possible, the total length of differential signals should be shorter than 12cm, the reference plane should be continuous and complete (If not, the biggest EMI problem may occur), and try to reduce vias between different layers in layout.
- 25MHz crystal should be placed close to PHY, and the surrounding had better shield by GND traces, and other signals cannot pass crystal.
- 0.1uF coupling capacitor of power supply is placed respectively close to power supply pin, and the way of traces had better pass by the capacitor before power supply pin.

- ePAD of PHY should at least more than 9 GND vias, shown as Figure 21-10.

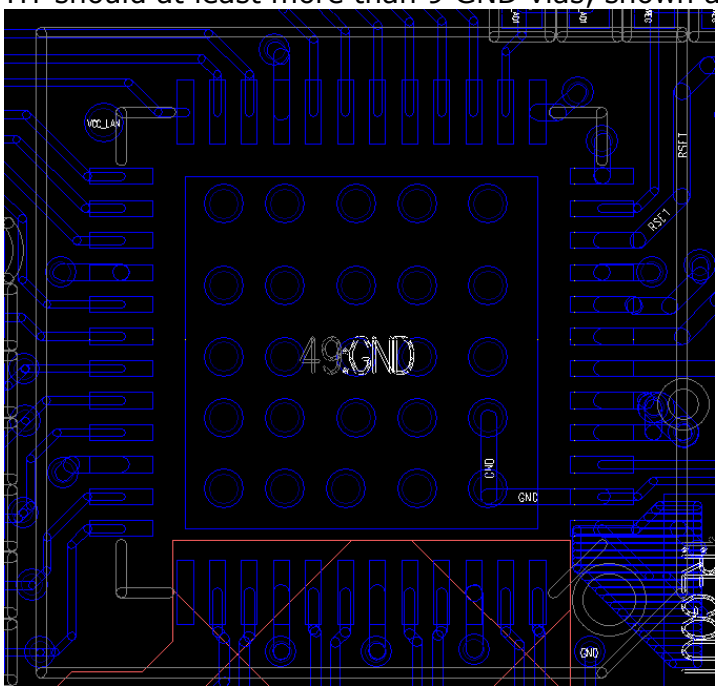


Figure 21-10

- R146 in Figure 21-11 should be placed close to PHY and shielded by GND traces, the traces are as short as possible, and make sure the reference plane is complete.

Figure 21-11

- RSET resistance R151 must close to PHY (less than 800mil), and keep far away from (VDDREG, REG_OUT, MDI0+/-,MDI1+/-etc.) and clock signals (the minimum distance is 50mils).

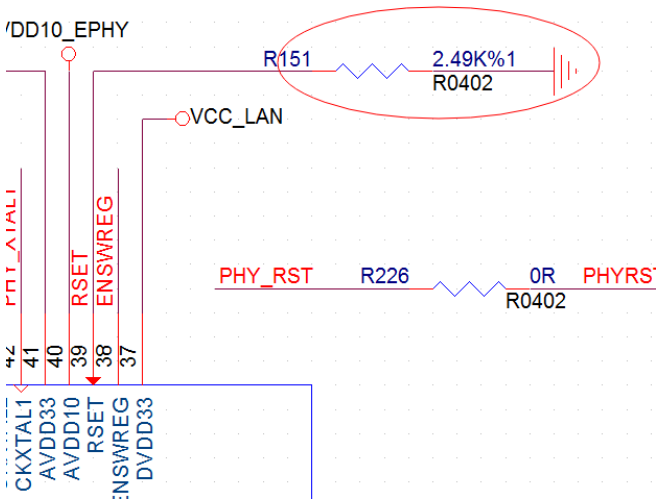


Figure 21-12

- The concatenation resistances in Figure 21-13 should be placed close to PHY to improve EMI.
  - MAC_RXCLK must be shielded by GND traces.
  - The distance between other signals in Figure 21-13 should meet the 3W layout rule.
  - RXD [0:3], RXCLK, RXDV traces should be controlled length, the skew of the whole signal trace should less than 100mil, the signal traces are as short as possible, the length of the whole trace should be shorter than 15cm.
  - Having the complete reference plane.

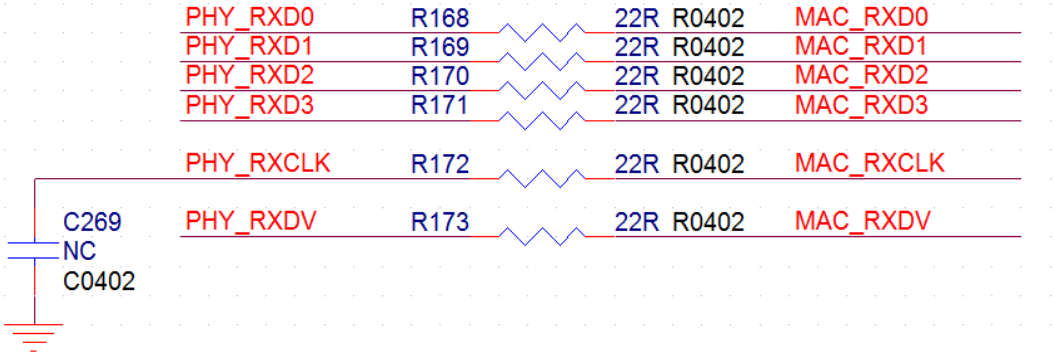


Figure 21-13

- The concatenation resistances in Figure 21-14 should be placed close to RK3288.
  - PHY_TXCLK must be shielded by GND traces to improve EMI.
  - The distance between other signals in Figure 21-13 should meet the 3W layout rule.
  - TXD [0:3], TXCLK, TXEN traces should be controlled length, the skew of the whole signal trace should less than 100mil, the signal traces are as short as possible, the length of the whole trace should be shorter than 15cm.
  - Having the complete reference plane.

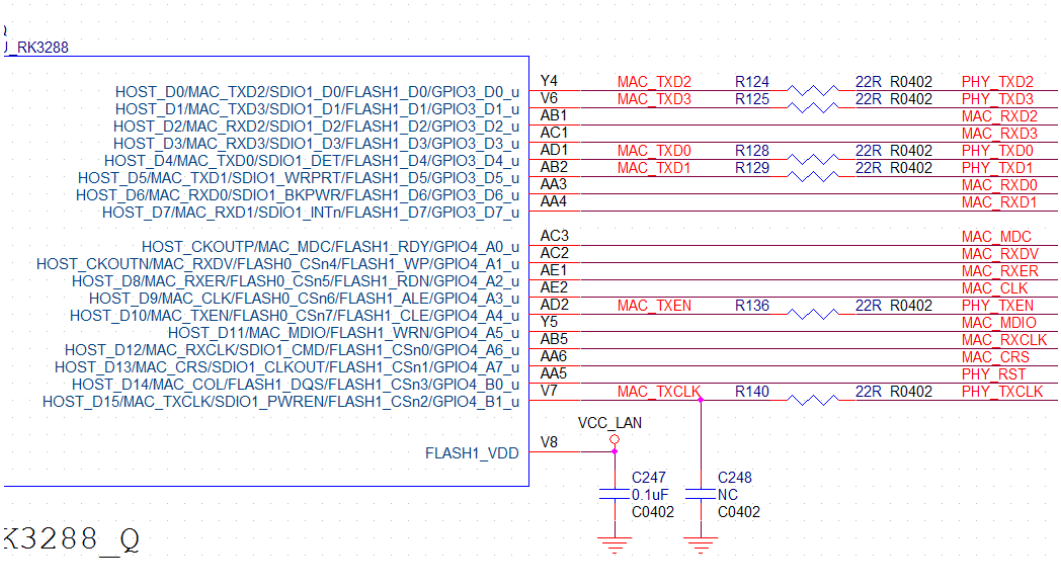


Figure 22-14

- Notices of internal Switching Regulator LAYOUT:
  - Place Capacitors C270, C271 of VDDREG power supply close to PIN44, 45, and the width of traces is not less than 40mil.
  - Place L9, C260 close to PIN48, and the width of traces is not less than 60mil.

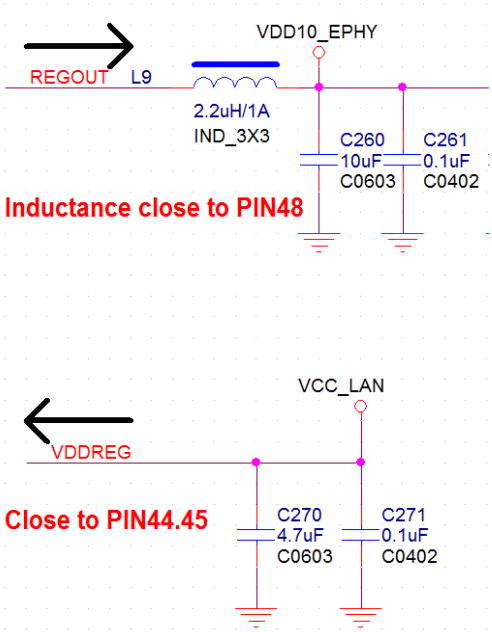


Figure 22-15

Chapter 22 2G/3G/4G

22.1 Schematic

GPIO interface power domain is APIO5_VDD power supply, and in the actual product designs, ensuring whether GPIO level is matching with 3G module, according to the actual demands of IO of 3G module, shown as Figure 21-1 and Figure 22-2.

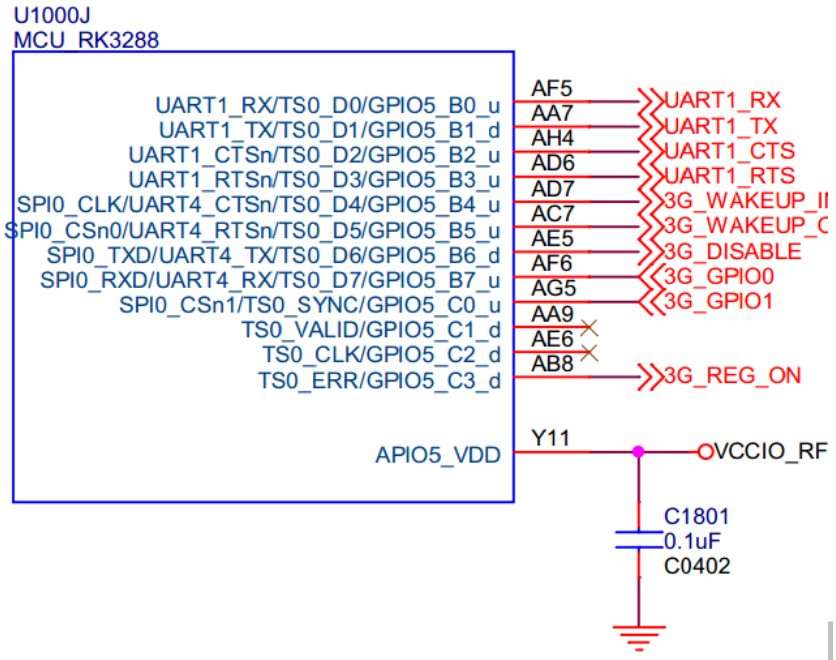


Figure 22-1

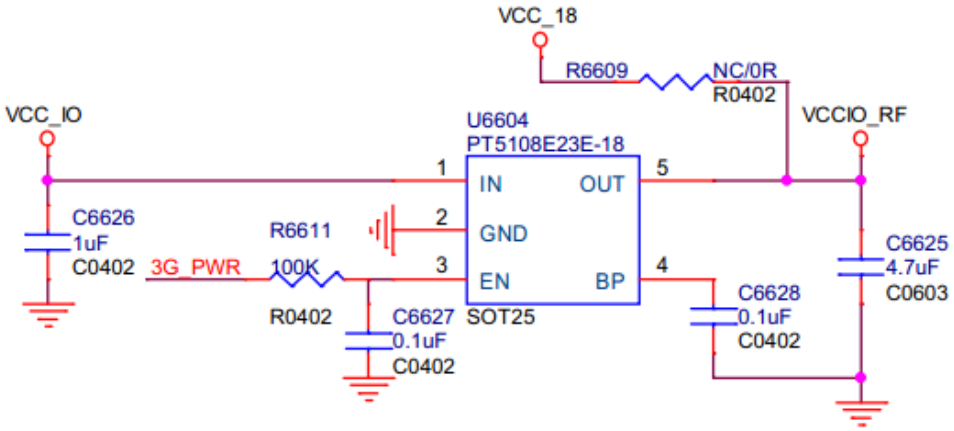


Figure 22-2

Reserve ESD devices for USIM socket to avoid the damage when the extracting the card, show as Figure 22-3.

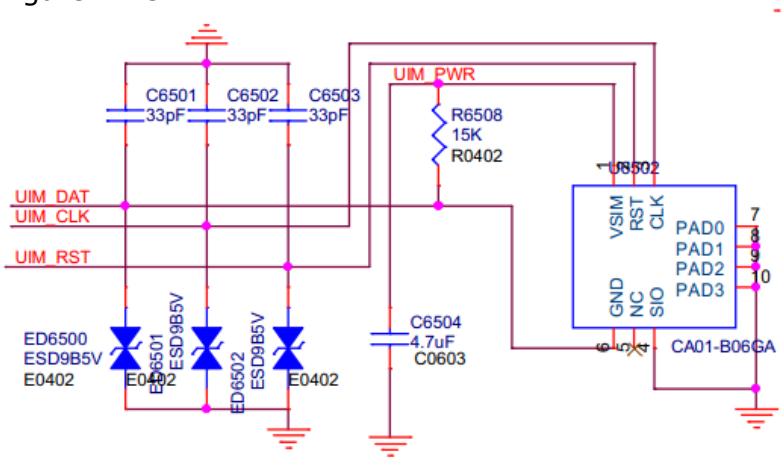


Figure 22-3

23.2 PCB Layout

- USIM socket should be close to 3G module in Layout, and the traces should be short and thick, and try to avoid the over-length. The traces of SCLK and SIO signals should be shielded by GND.
- The transient current of 3G module transmits at the maximum power will up to 1.8A, so the part of power supply is recommended to use DC/DC of high current or MOS of low ESR. And the reservoir capacitors of large capacity value (the circle in Figure 22-4) please be placed close to module pin. The traces try to use pour copper and the width is more than 100mil.

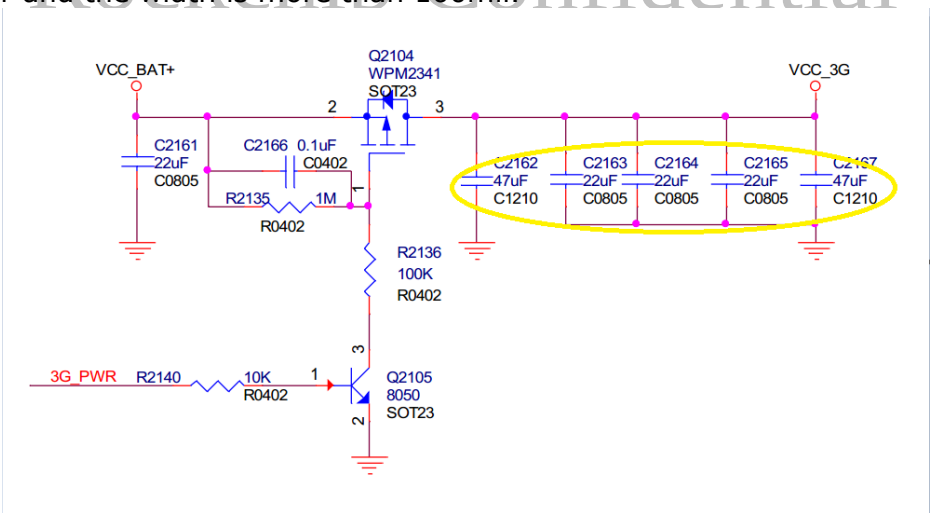


Figure 22-4

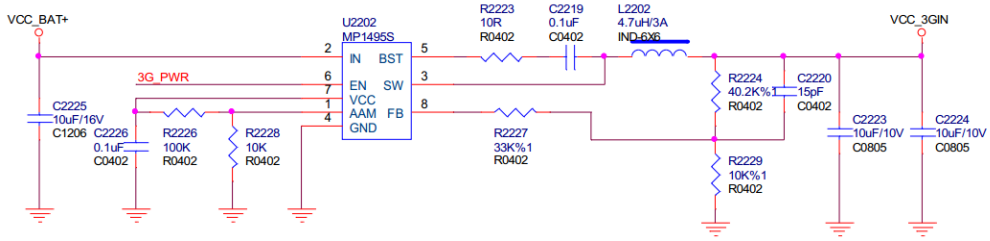


Figure 22-5

- Due to the high EMC interference of switching power, the power supply traces and other high-speed signals should not be close to the antenna.
- If the module itself is not shielded, the shielding must be added to the board and shielded completely by GND traces, shown as Figure 22-6.

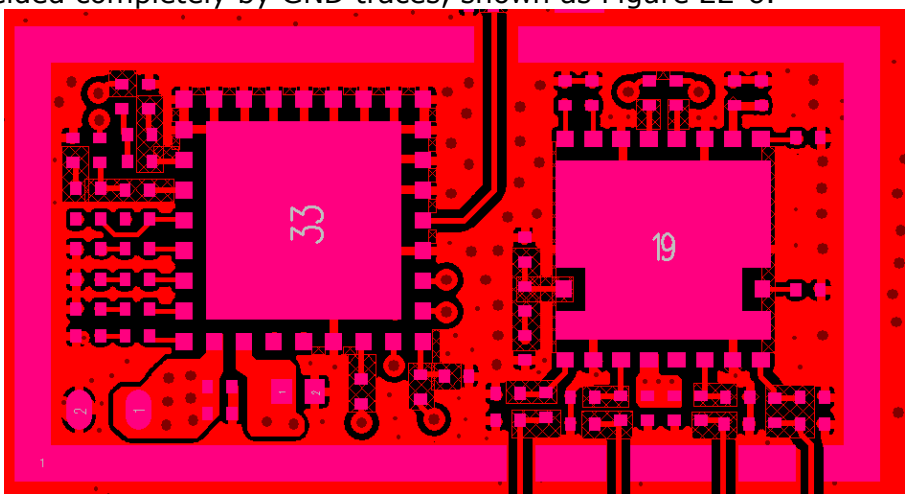


Figure 22-6

- The design of the 3G antenna and the width of microstrip should consider the impedance, which requires Z=50±10ohm. And the complete reference GND plane under the RF signal traces is needed.
- The longer the length of antenna path is in layout, the larger the energy loss, so in design, the path of the antenna is as short as possible and cannot have branches and vias, shown as Figure 22-7.
- The quantity of radiant energy of the antenna is large, so the antenna should not to disturb the sensitive detector and signals like DDR, FB of DC/DC.
- When the antenna needs to swerve, please trace with arc but not at corner, shown as Figure 22-7.

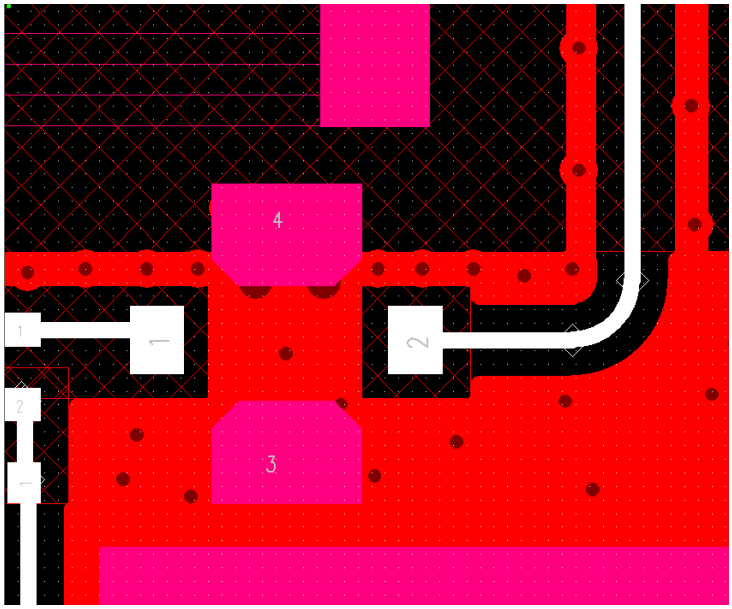


Figure 23-7

Chapter 23 WIFI & BT

23.1 Schematic

RK3288 supports WIFI/BT module of SDIO 3.0 interface. When using WIFI/BT module of SDIO, UART interface, power supply of UART controller APIO3_VDD should be consistent with VCCIO Supply module, shown as Figure 23-1, Figure 23-2.

Tip:

- **In SDIO 3.0, APIO3_VDD power supply must be 1.8V;**

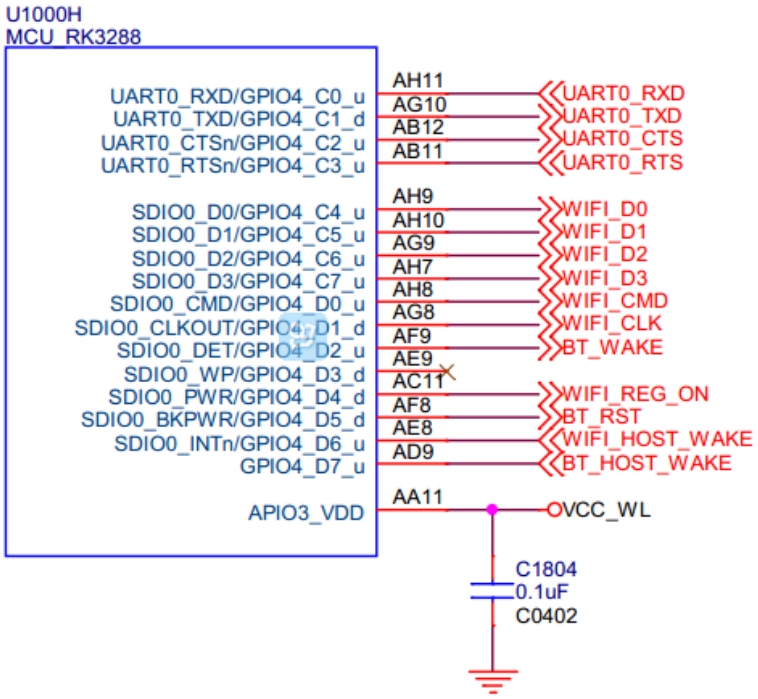


Figure 23-1

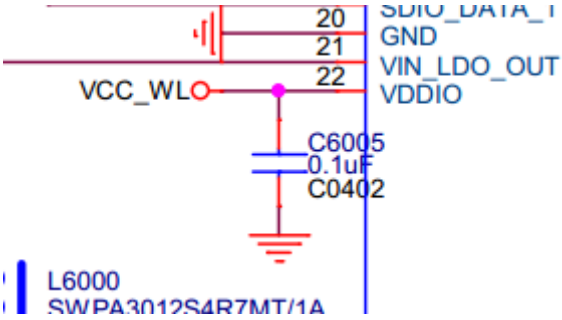


Figure 23-2

RTC_CLOCK of WIFI should pay attention to level match and choose the appropriate partial pressure ratio of the resistance to meet the WIFI input demands, otherwise WIFI could work abnormally, shown as Figure 23-3, Figure 23-4.

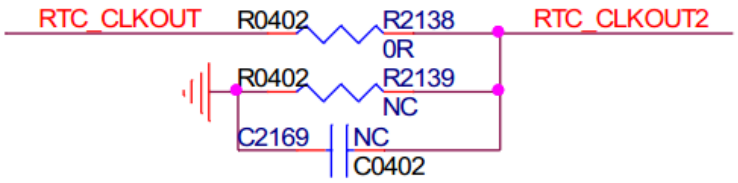


Figure 23-3

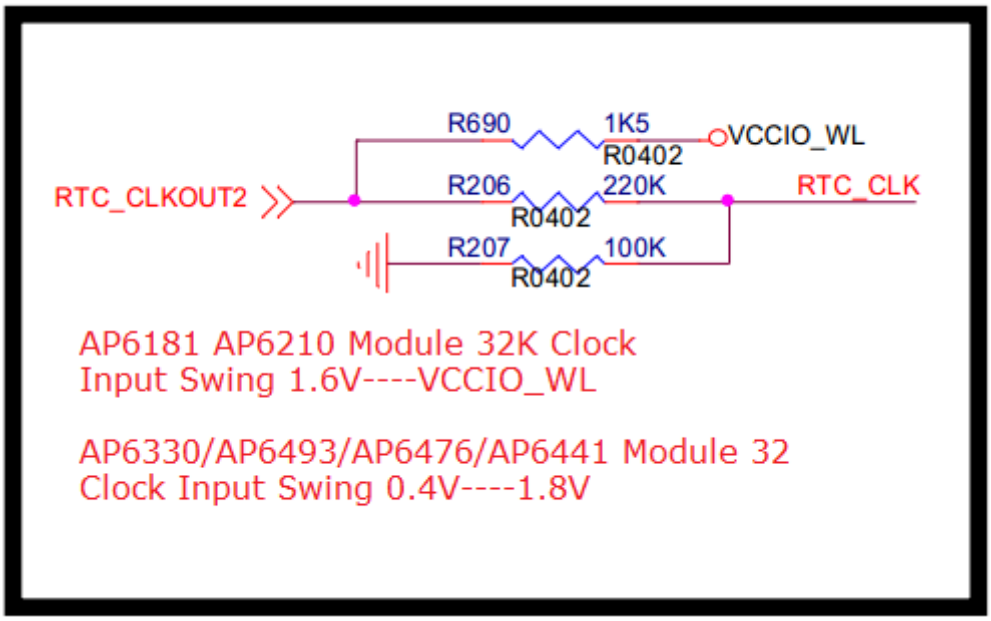


Figure 23-4

Please note that WIFI should choose the crystal whose ESR is less than 60ohm and whose frequency offset error is less than 20ppm. The matching capacitors of the crystal, please select the appropriate capacitance value according to the crystal specification to avoid frequency offset too large and resulting in abnormal working (for example the number of hot spots is less), show as Figure 23-5.

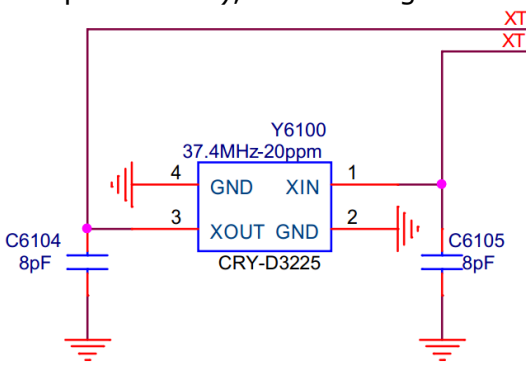


Figure 23-5

Reserve the pull-up resistances SDID (Figure 23-6), which is mounted to promote the quality of signal when WIFI is using SDIO 3.0.

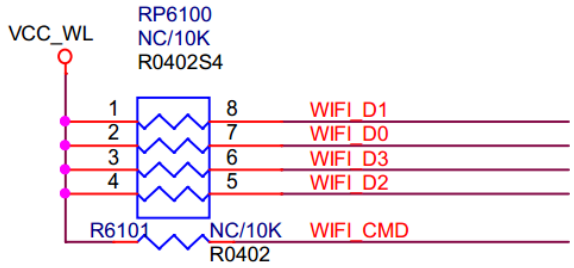


Figure 23-6

The voltage range of VBAT power supply of AP6XXX is 3.0V~4.8V, and the power supply current is at least 400mA.

Note:
VBAT Voltage Range 3.0V~4.8V
Supply Current At Least 400mA

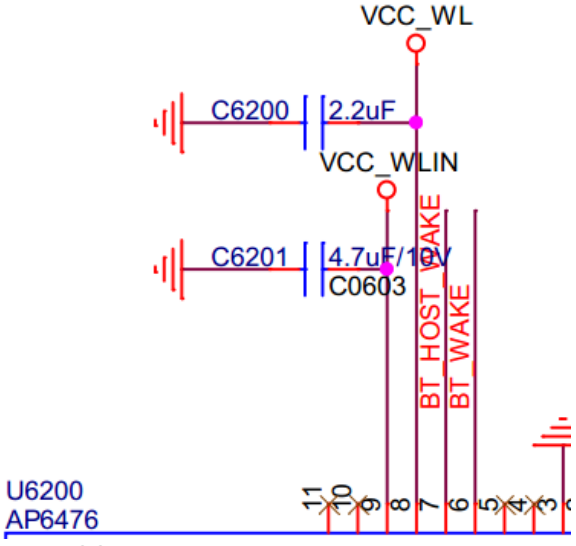


Figure 23-7

24.2 PCB Layout

- WIFI module please keep away from the high speed devices like DDR.
- SDIO signal traces try to be parallel and shielded in the group by GND traces, if having a rich space, CLK is recommended to be shielded separately by GND traces. Layout should avoid closing to power supply and high-speed signals. The skew of any two signals in the signal group should be controlled within 400mil, otherwise the frequency in high speed mode would not meet to the standard.
- The length of PCB Layout of TF Card try to limit within 12.4inch. It is recommended customers to use drive strength and Timing Tuning adaptive algorithms to promote the stability and compatibility of SDIO.
- Shown as Figure 23-8, the 4.7uF coupling capacitors C6100, C6111 of VBAT and VDDIO power supply of module should be placed close to the module and be placed in the same plane with the module.

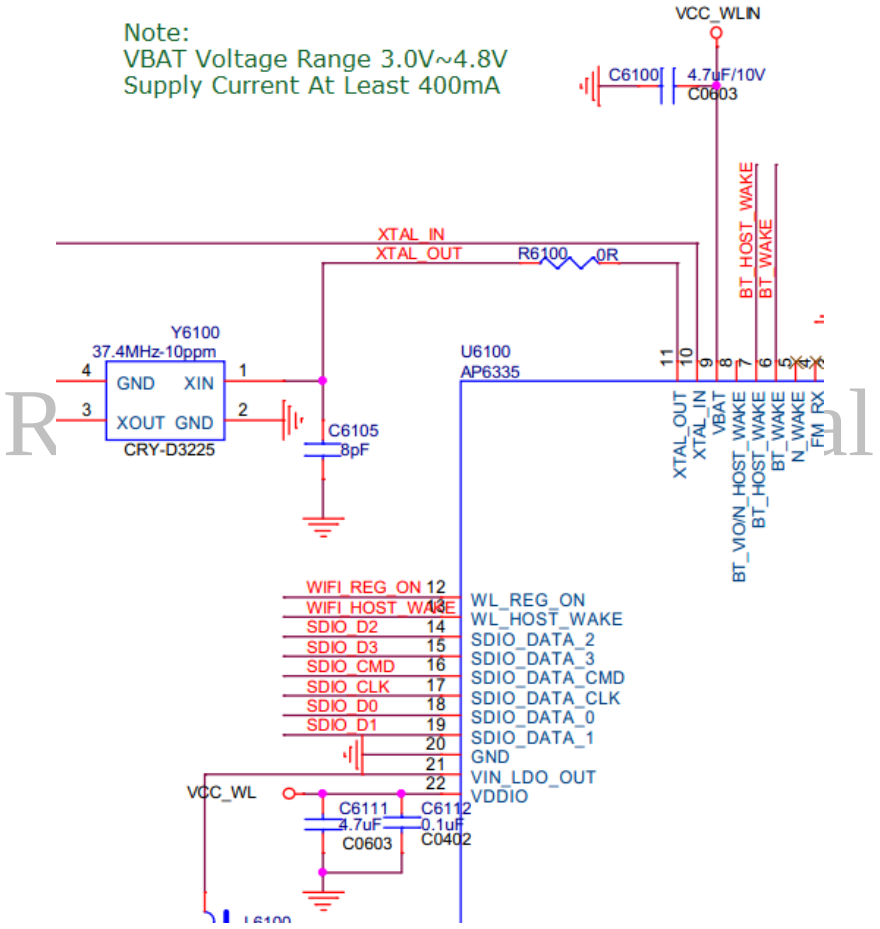


Figure 23-8

- Shown as Figure 23-9, Figure 23-10, the inductance L6100 of internal power supply in the module and the capacitor C6116 should be placed close to the module, and the width of the traces should be more than 15mil.

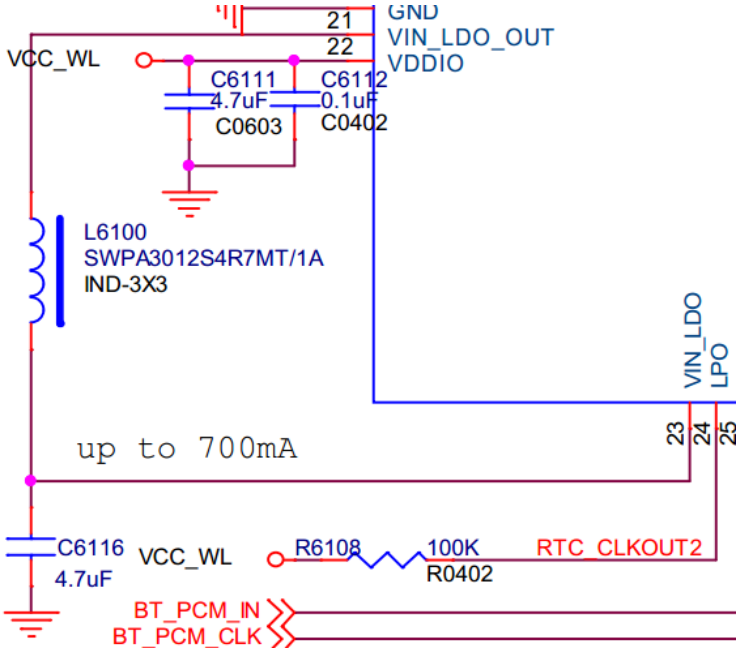


Figure 23-9

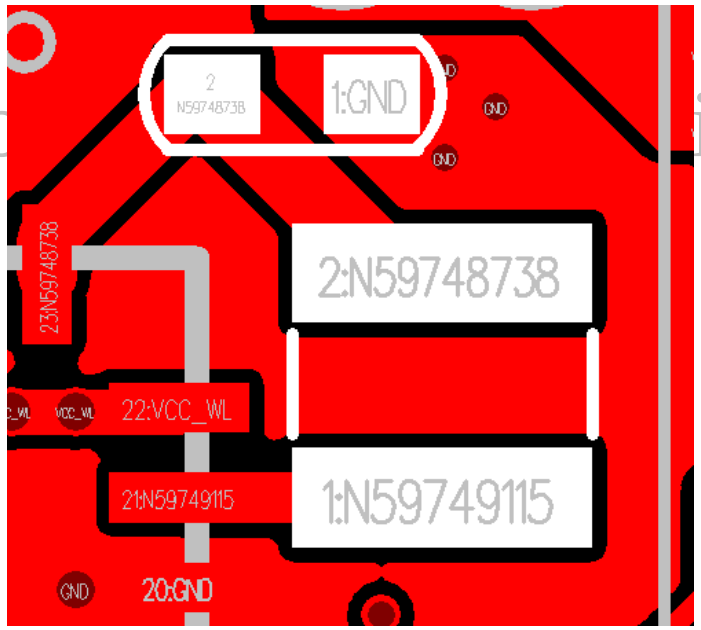


Figure 23-10

- Keep the complete GND reference plane on the first layer under the module, and other signal traces cannot pass the plane, shown as Figure 23-11.

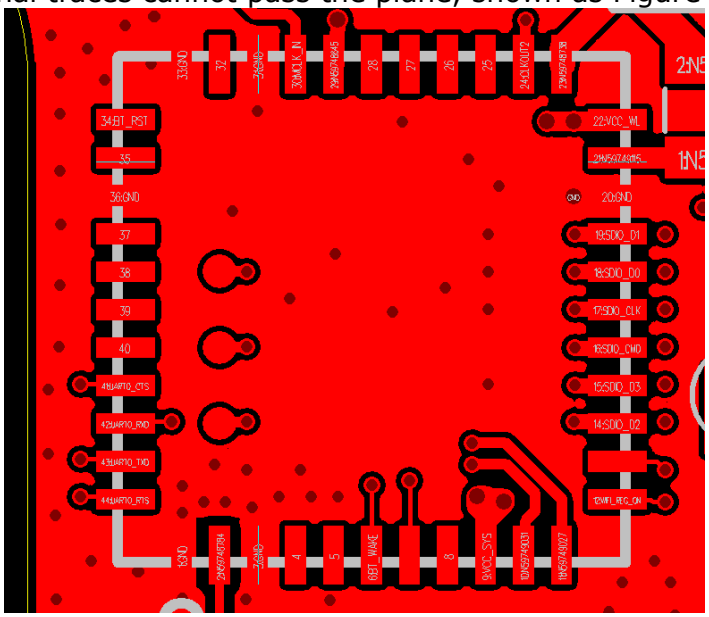


Figure 23-11

- Keep the complete GND reference plane under the Crystal, avoiding other signal traces, and having efficient GND vias in the crystal pins, shown as Figure 23-12.

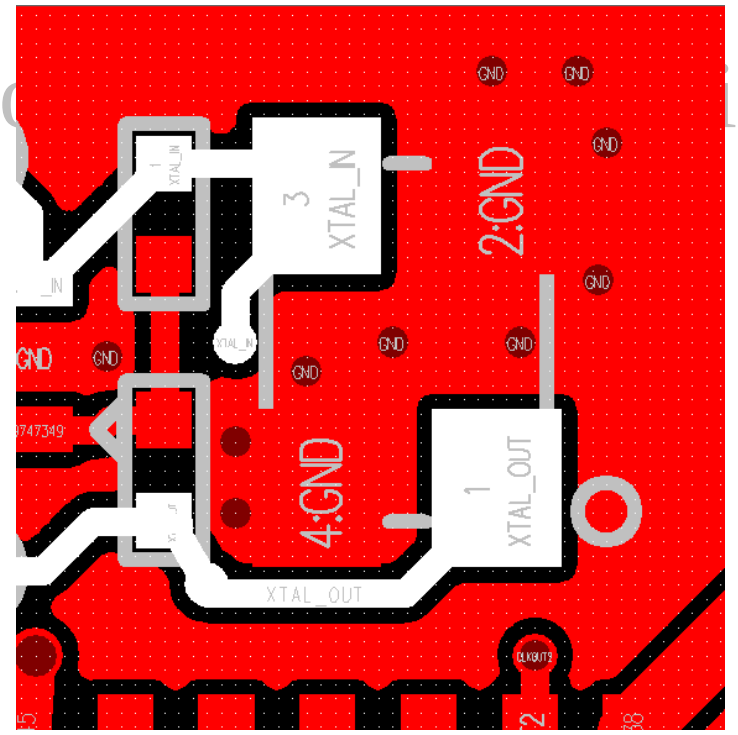


Figure 23-12

-

- The design of the antenna and the width of microstrip should consider the impedance, which requires Z=50±10ohm, and the complete GND reference plane under the RF signal traces is needed.
- The longer the antenna signal path is in layout, the larger the energy loss, so in design, the path of the antenna is as short as possible and cannot have branches and vias, shown as Figure 23-13, and Figure 23-14 is the wrong layout.
- When the antenna needs to swerve, please trace with arc but not at corner, shown as Figure 23-15, and Figure 23-14 is the wrong layout.

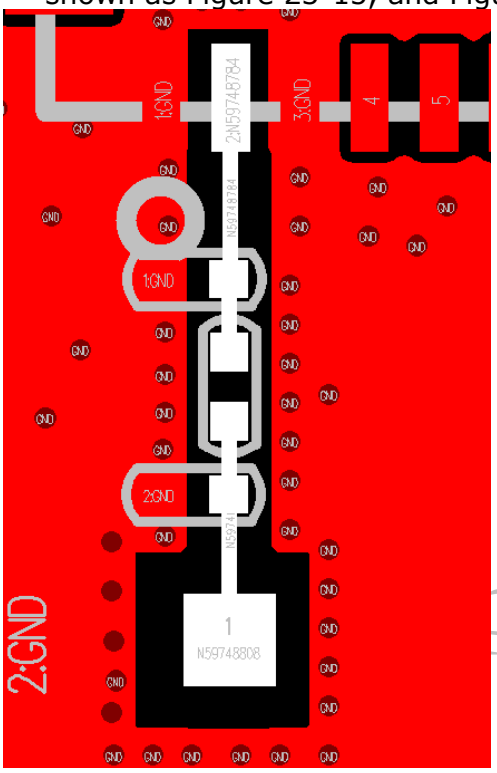


Figure 24-13

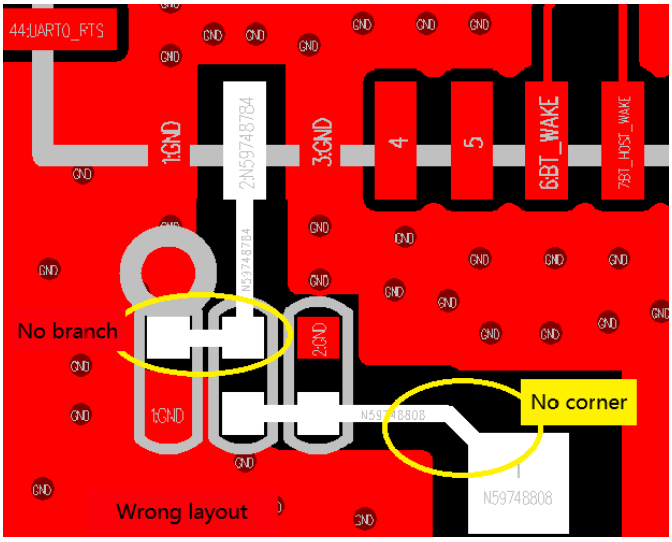


Figure 24-14

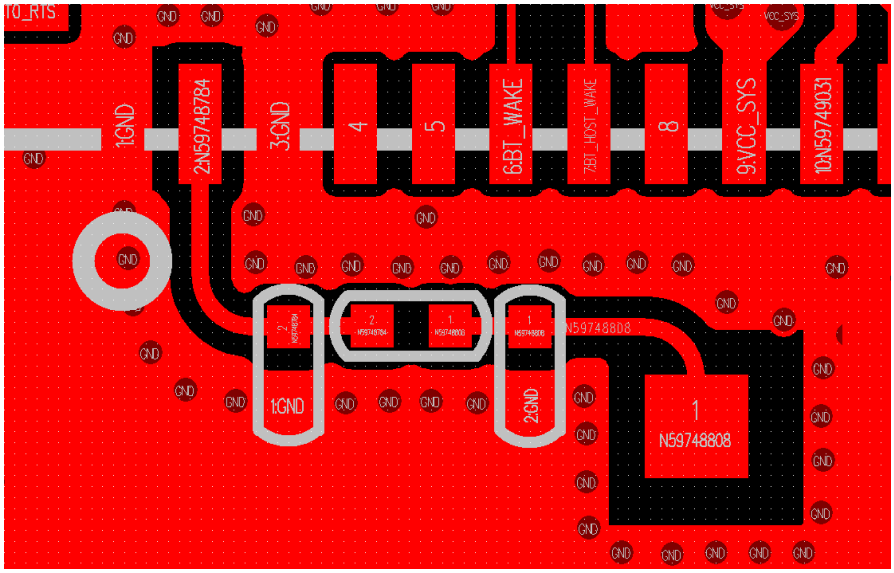


Figure 23-15

- The suggested placement of modules and antennas is shown as Figure 23-16, do not be placed in the place of hand and keep far away from the metal devices as far as possible.

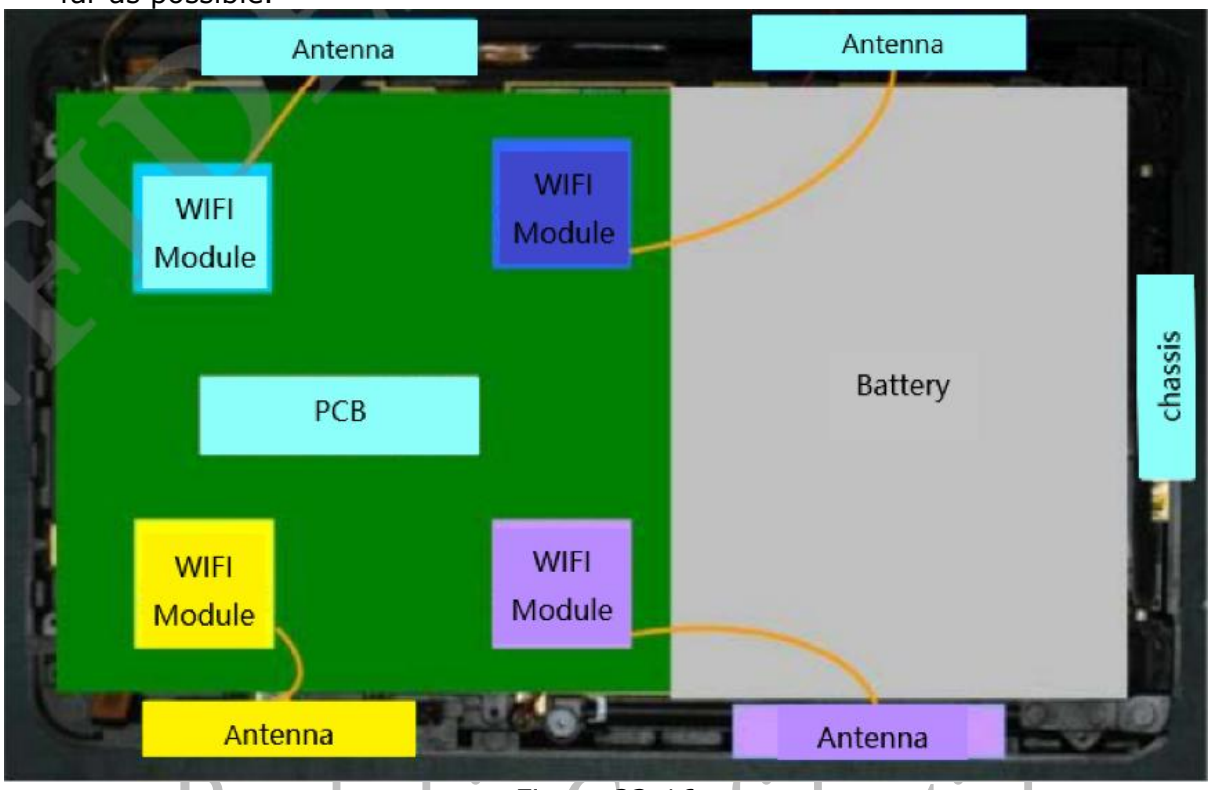


Figure 23-16

- The antenna should be matched and not be twisted with battery cables and speaker cables, and cannot pass the area of FPC and DDR.
- The feeder trace of the antenna cannot too long which would cause too much loss of RF energy, therefore the suitable length of the feeder is shorter than 7 centimeters. When stripping the feeders, please do not stripping the shielding net too much to cause the 50ohm impedance discontinuity, shown as Figure 23-17.

Figure 23-17

Chapter 24 GPS

24.1 PCB Layout

GPS is the sensitive part and is easily disturbed by magnetic field, therefor the inappropriate layout in space and structure may influence the GPS performance, such as loudspeaker, battery, metal materials, key, connector, LCD and touching FPC cable and a variety of longer flying lines. In structure, try to make GPS antenna away from the battery, speaker, connector, LCD and Camera socket, and try to place GPS antenna at the corner of having less EMI and noise, shown as Figure 24-1.

Figure 24-1

The working frequency of 2G, 3G module are not in the GPS frequency band, but when they and GPS are working at the same time, their peak power is large, and if their antennas is too close to GPS antennas (less than 10 centimeters), the input terminal of LNA is easy to saturate causing GPS work abnormally.

The product with GPS try to adopt the plastic shell but not the aluminum shell, otherwise GPS signal would be blocked completely and unable to work. If using the shell with aluminum alloy frame, the distance from the mullion to the antenna should be longer than 7mm. If must using the aluminum shell, then the area of louver should be at least lager than 3*3 centimeters and make sure the rear housing grounded well.

To ensure the GPS performance, it is necessary to have the shielding case, conductive fabric and conductive foam.

The internal layout in GPS, the related devices of the access of RF (LNA, SAW Filter, and matching circuit etc.) should be placed compactly, and the path from antenna feed to chip RF_IN should be as short as possible, which is less attenuation and less interference, shown as the highlight traces in yellow in Figure 24-2.

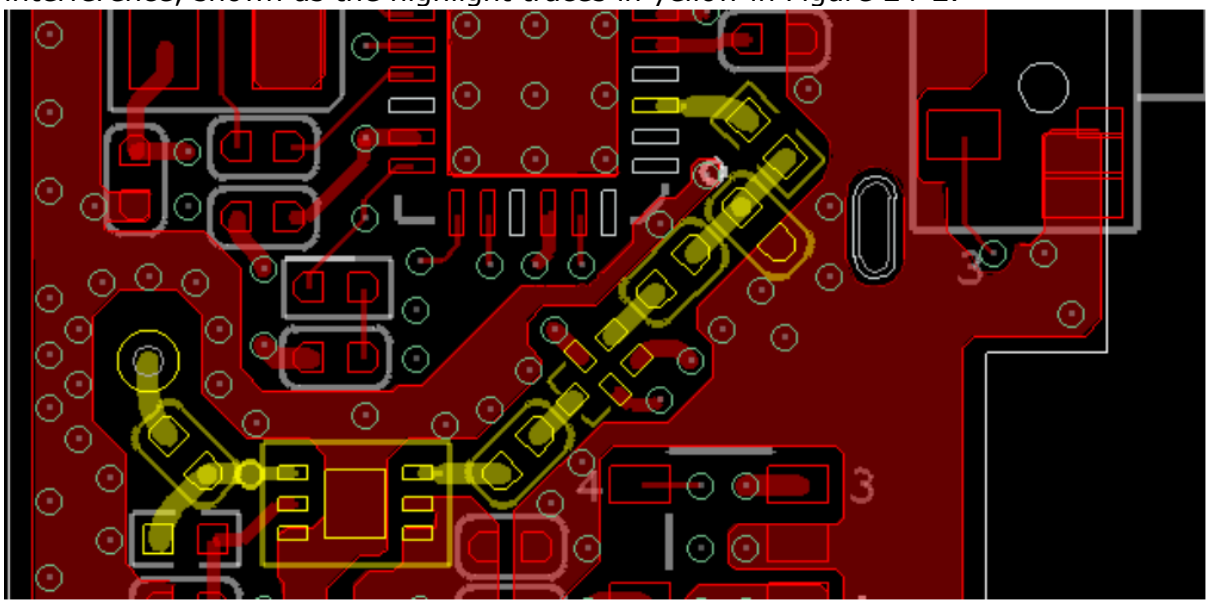


Figure 24-2

Because of the high receiving sensitivity of GPS (>-140dbm), the demand to control the Impedance is also comparatively high, if the Impedance cannot be controlled well, the standing wave and return loss would increase, which influence the GPS performance directly. The Impedance requirements Z=50±10ohm, and the complete GND reference plane under the RF signal trace is needed.

RF signal trace of GPS usually use the method of interlayer reference, which remove the copper on the second layer and regard the third layer as the reference plane for resistance traces, which can improve the accuracy of controlling the resistance, otherwise, the error of controlling the resistance would be large in the width of 4~5mil.

Chapter 25 NFC

25.1 Schematic

NFC technology uses loop antenna, the basic sensing distance is about 2 centimeters, and the current in work is up to about 200mA. RSM1, RSM2 please use the size of R0603, and the antenna traces cannot less than 12mil.

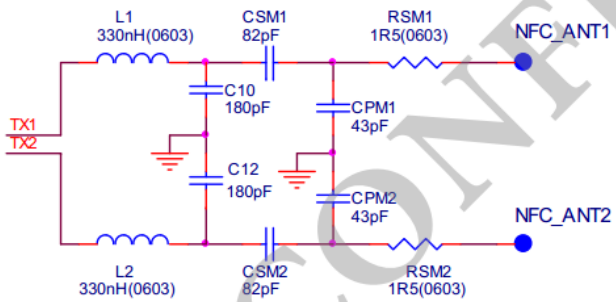


Figure 25-1

NFC antenna can be placed on the battery, and NFC absorbing material should be pasted between the antenna and the battery to avoid the antenna distance is decrease seriously.

Figure 25-2

25.2 PCB Layout

If using NFC technology, the product structure should not be used in metal shell.
NFC is communicated by magnetic induction, please place vertically to avoid the impedance discontinuity for mutual inductance between L1 and L2, shown as Figure 25-3.

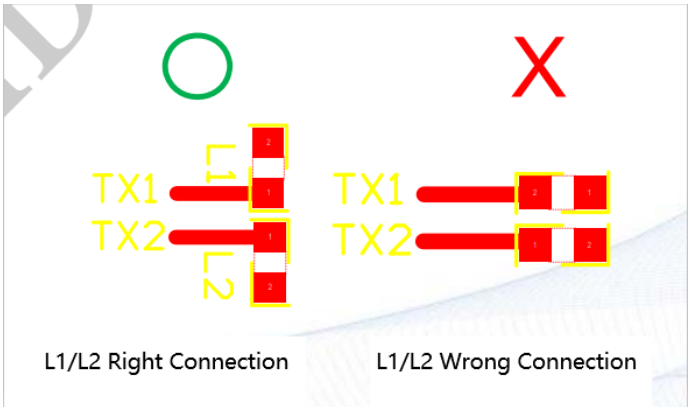


Figure 25-3